Introduction

Ideally, a programmable logic design environment satisfies a large variety of design requirements: it should support devices with different architectures, run on multiple platforms, provide an easy-to-use interface, and offer a broad range of features. Moreover, a design environment should give designers the freedom to use the design entry methods and tools of their choice. The Altera MAX+PLUS II development system is a fully integrated programmable logic design environment that meets all of these requirements.

The MAX+PLUS II design environment offers unmatched flexibility and performance. The rich graphical user interface is complemented by complete and instantly accessible on-line documentation, which makes learning and using MAX+PLUS II quick and easy.

MAX+PLUS II includes the following features:

- **Open Interfaces**—Altera works closely with EDA manufacturers to link MAX+PLUS II with other industry-standard design entry, synthesis, and verification tools. The interfaces to EDA tools comply with EDIF 2.00 and 3.00, library of parameterized modules (LPM), SDF, VITAL, Verilog HDL, VHDL, and other standards. The MAX+PLUS II interfaces allow users to create a logic design with Altera or standard EDA design entry tools, compile the design for an Altera device with the MAX+PLUS II Compiler, and perform device- or board-level simulation with Altera or other EDA verification tools. MAX+PLUS II currently has interfaces to tools from Cadence, Data I/O, Exemplar, Mentor Graphics, MINC, OrCAD, Synopsys, VeriBest, Viewlogic, and others.

- **Architecture-Independence**—MAX+PLUS II supports Altera’s FLEX 10K, FLEX 8000, MAX 9000, MAX 7000, FLASHlogic, MAX 5000, and Classic programmable logic device families, and offers the industry’s only truly architecture-independent programmable logic design environment. The MAX+PLUS II Compiler also provides powerful logic synthesis and minimization to efficiently fit designs with minimal user effort.
- **Multiple Platforms**—MAX+PLUS II runs under Microsoft Windows, Windows for Workgroups, Windows 95, or Windows NT on 486- or Pentium-based PCs, and under X Windows on Sun SPARCstation, HP 9000 Series 700, and IBM RISC System/6000 workstations.

- **Full Integration**—Together, MAX+PLUS II design entry, processing, and verification features offer the most fully integrated suite of programmable logic development tools available, allowing faster debugging and shorter development cycles.

- **Modular Tools**—Designers can customize their development environment by choosing from a variety of design entry, compilation, verification, and device programming options, all of which are described in this data sheet. Additional features can be added as needed, preserving the initial tools investment. Because MAX+PLUS II supports multiple device families, designers can add support for new architectures without having to learn new tools.

- **Hardware Description Languages (HDLs)**—MAX+PLUS II supports a variety of HDL design entry options, including VHDL, Verilog HDL, and the Altera Hardware Description Language (AHDL).

The MAX+PLUS II design process, shown in Figure 1, consists of four phases: design entry, design compilation, design verification, and device programming.
MAX+PLUS II can integrate multiple design files—generated with MAX+PLUS II design entry tools or with a variety of other industry-standard EDA design entry tools—into a single design hierarchy. The extensive integration between MAX+PLUS II applications allows information to flow freely to and from each application. For example, any errors identified during compilation, simulation, and timing analysis can be automatically located and highlighted in the original design file or in the Floorplan Editor. If a design (called a “project” in MAX+PLUS II) consists of two or more levels of hierarchy, the user can navigate from one design file directly to any other design file in the hierarchy, regardless of whether it is graphic-, text-, or waveform-based.
Industry-Standard LPM Support

Users can create their designs using functions from the industry-standard library of parameterized modules (LPM). The LPM offers scalable logic functions, such as RAM, counters, adders, and multiplexers, and preserves high-level design information for optimal implementation. The MAX+PLUS II Compiler automatically generates optimized, architecture-specific implementations of the LPM functions. LPM functions can be implemented with industry-standard design entry tools, or in schematic or text designs created with MAX+PLUS II.

Industry-Standard EDA Design Entry

The MAX+PLUS II Compiler interfaces with industry-standard EDA tools that generate EDIF 2.0.0 and 3.0.0 netlist files, including files that contain LPM functions. The Compiler uses Library Mapping Files (.lmf) to map proprietary symbol and pin names from other EDA tools to MAX+PLUS II logic functions. Altera provides LMFs for over 100 logic functions used with tools from companies such as Cadence, Mentor Graphics, MINC, OrCAD, Viewlogic, and others. VHDL and Verilog HDL design support is also available from Cadence, Exemplar, Mentor Graphics, Synopsys, VeriBest, Viewlogic, and others.

For more information on other industry-standard design entry tools, see EDA Software Support in this data book.

MAX+PLUS II can also read OrCAD Schematic Files (.sch) or Xilinx Netlist Files (.xnf) for compilation or integration into designs for Altera devices.

Schematic Capture & Symbol Editing

The MAX+PLUS II Graphic Editor, shown in Figure 2, makes schematic design entry fast and easy. Drag-and-drop editing allows the user to quickly move one or more objects or an entire area. During a move, a net can be preserved with the rubberbanding feature. The designer can also make a design more compact by connecting primitives with buses to create arrays of symbols. MAX+PLUS II provides symbols for over 300 74-series, LPM, and custom functions.

MAX+PLUS II can automatically create a symbol for any design file. With the Symbol Editor (also shown in Figure 2), the designer can modify a symbol to customize its appearance, or create an entirely new symbol.

The MAX+PLUS II Graphic Editor can also open and save OrCAD Schematic Files (.sch).
Hardware Description Language (HDL) Entry

The MAX+PLUS II Text Editor is ideal for entering and editing hardware description language (HDL) design files written in VHDL, Verilog HDL, or the Altera Hardware Description Language (AHDL). The MAX+PLUS II Compiler can synthesize logic from any of these languages and map it to any of Altera’s FLEX, MAX, and Classic device families.

Each of these HDLs can implement state machines, truth tables, conditional logic, Boolean equations, and arithmetic operations—including addition, subtraction, equality and magnitude comparison. (In addition, AHDL and VHDL also support the LPM.) Together, these features make it easy to implement complex projects in a concise, high-level description.
Waveform Design Entry

The MAX+PLUS II Waveform Editor (shown in Figure 3) is used to create and edit waveform design files, as well as input vectors for simulation and functional testing. The Waveform Editor also functions as a logic analyzer that allows the designer to view simulation results.

Waveform design entry is best suited for sequential and repeating functions. The Compiler’s advanced waveform synthesis algorithms automatically generate logic from user-defined input and output waveforms that represent registered, combinatorial, and state machine logic. The Compiler automatically assigns state bits and state variables for state machines.

Waveform Editor features allow the designer to copy, cut, paste, repeat, and stretch waveforms; to create design files with internal nodes, flipflops, state machines and memory words; to combine waveforms into groups that display binary, octal, decimal, or hexadecimal values; to compare two sets of simulation results by superimposing one set of waveforms on another; and to annotate files with comments.
Floorplan Editing

The MAX+PLUS II Floorplan Editor (shown in Figure 4) simplifies the process of assigning logic to device pins and logic cells. A graphical image of each device used in a project allows easy logic placement. Both high-level and detailed device views are available. The designer can assign pins and logic cells before compiling a design, and can view and modify the results after compilation.

Floorplan Editor features allow the designer to view all assigned and unassigned logic in a device. The Floorplan Editor provides a color-coded view of all logic resources in the device, as well as user assignments, fan-in and fan-out information, and architecture-specific features. Any node or pin can be dragged to a new location. Logic can be assigned to specific pins and logic cells, or to more general regions within a device. Assignments can also be made with menu commands in any MAX+PLUS II application. All assignments are stored in the text-based Assignment & Configuration File (.acf), which can be edited in the MAX+PLUS II Text Editor.

Figure 4. MAX+PLUS II Floorplan Editor
Hierarchical Design Entry

Hierarchical designs can consist of design files created using several different methods, including schematic capture, HDL design entry, waveform design entry, and industry-standard netlist files. MAX+PLUS II supports multiple levels of hierarchy in a single design. This flexibility allows designers to use the design entry method best suited to each portion of the design. The MAX+PLUS II Hierarchy Display, which displays the hierarchical structure of a project, allows designers to easily traverse the hierarchy, automatically opening the appropriate editor for each design file. See Figure 5.

Figure 5. MAX+PLUS II Hierarchy Display

Design Compilation

When MAX+PLUS II processes a design, the Compiler reads in design files and produces output files for programming, simulation, and timing analysis. The Message Processor can automatically locate errors detected during compilation and take users to the source design files. MAX+PLUS II supports FLEX 10K, FLEX 8000, MAX 9000, MAX 7000, MAX 5000, and Classic devices. (Compilation support for FLASHlogic devices is provided by Altera’s PLDshell Plus software.)

The MAX+PLUS II Message Processor communicates with all MAX+PLUS II applications, reporting error, information, and warning messages for design problems such as connection and syntax errors, as well as simulation, timing analysis and programming information. Designers can use the Message Processor to automatically open the design file that contains the source of an error and highlight its location. In addition, the Message Processor can locate errors in the floorplan for the current project in the Floorplan Editor. See Figure 6.
Logic Synthesis & Fitting

The MAX+PLUS II Compiler’s Logic Synthesizer module supports both synthesized and what-you-see-is-what-you-get (WYSIWYG) design implementation. It selects appropriate logic reduction algorithms to minimize and remove redundant logic, ensuring that the device logic resources are used as efficiently as possible for the target device architecture. It also removes unused logic from the project.

Logic synthesis options help the designer guide the outcome of logic synthesis. Altera provides three “ready-made” synthesis styles, which specify the settings for multiple logic synthesis options. The designer can choose a default style to set default synthesis options, create custom styles, and specify individual synthesis options on selected logic functions. Synthesis options can be tailored for a specific device family to take advantage of its architecture. A number of advanced logic options further expand the designer’s ability to control logic synthesis.
The Compiler’s Fitter module applies heuristic rules to select the best possible implementation for the synthesized project in one or more devices. This automatic fitting relieves the designer of tedious place-and-route tasks. The Fitter generates a Report File (.rpt) that shows project implementation as well as any unused resources in the device(s). Fitting results can also be displayed in the MAX+PLUS II Floorplan Editor.

**Timing-Driven Compilation**

The Compiler can implement user-specified timing requirements for propagation delays (t_{PD}), clock-to-output delays (t_{CO}), setup times (t_{SU}), and clock frequency (f_{MAX}). Designers can specify timing requirements on selected logic functions and for a project as a whole. The Report File and Compiler messages provide detailed information on how the timing requirements have been implemented in the project.

**Design-Rule Checking**

The MAX+PLUS II Compiler includes the Design Doctor, a design-rule checker. The Design Doctor checks each design file for logic that may cause system-level reliability problems that are usually discovered only after a design has entered production. The user can choose one of three predefined sets of design rules, or create a custom set of rules.

Design rules are based on reliability guidelines that cover potential design problems such as asynchronous inputs, ripple clocks, multi-level logic on clocks, preset and clear configurations, and race conditions. Rule violations are explained to help the designer determine which edits are needed in the design files.

**Multi-Device Partitioning**

If a project is too large to fit in a single device, the Compiler’s Partitioner module divides it into multiple devices from the same device family. The Partitioner attempts to split the project into the fewest possible number of devices while minimizing the number of pins used for inter-device communication. The Fitter automatically fits the logic into the specified devices.

Partitioning can be totally automatic, partially user-controlled, or fully user-controlled. If a project is too large to fit into the target device, the designer can specify the type and number of additional devices.
Industry-Standard Simulation Formats

The MAX+PLUS II Compiler can create netlist files for use in a variety of simulation environments. These netlist files contain post-synthesis functional and timing information that can be used with standard design verification tools for device- or board-level simulation.

The following interfaces are available:

**Interface:** MAX+PLUS II Support:

- **EDIF**
  - Creates EDIF 2.0.0 and 3.0.0 netlist files that provide functionality and timing for third-party simulators.

- **Verilog HDL**
  - Creates Verilog HDL netlist files that can be used with Verilog-XL simulators.

- **VHDL**
  - Creates VHDL netlist files that can be used with VHDL simulators.

For each interface, the Compiler can optionally generate a Standard Delay Output Format File (.sdo) that includes timing information for simulators that require timing and functional information in separate files.

Programming File Generation

The Assembler module creates one or more Programmer Object Files (.pof), SRAM Object Files (.sof), JEDEC Files (.jed), Hexadecimal (Intel-format) Files (.hex), and Tabular Text Files (.ttf) for a compiled project. The MAX+PLUS II Programmer uses POFs, SOFs, and JEDEC Files together with standard Altera hardware to program devices. Device programming is also available with other industry-standard programming equipment. In addition, MAX+PLUS II can generate Raw Binary Files (.rbf) and Serial Bitstream Files (.sbf). These files, as well as Hex files and TTFs, can be used for configuring FLEX 10K and FLEX 8000 devices in-system. MAX+PLUS II POFs and Serial Vector Format (.svf) files can be used for in-system programming of MAX 9000 and MAX 7000S devices.

Design Verification

MAX+PLUS II offers design verification capabilities, including design simulation and timing analysis, that test the logical operation and internal timing of a design. Design verification tools for Altera devices are also available from a variety of EDA vendors.
Simulation

The MAX+PLUS II Simulator provides flexibility and control for modeling single- or multi-device projects. The Simulator uses simulation netlist files that are generated during compilation to perform functional, timing, or multi-device simulation for a project. Figure 7 shows the MAX+PLUS II Simulator.

Figure 7. MAX+PLUS II Simulator

The designer either defines input stimuli with a straightforward vector input language or draws waveforms directly with the MAX+PLUS II Waveform Editor. Simulation results can be viewed in the Waveform Editor or Text Editor and printed as waveform or text files.

The designer specifies commands either interactively or in a text-based command file to perform a variety of tasks, such as monitoring the project for glitches, oscillation, and register setup and hold time violations; halting the simulation when user-defined conditions are met; forcing flipflops high or low; performing functional testing; and defining initial memory contents for RAM or ROM blocks. If a setup or hold time, minimum pulse width, or oscillation period is violated, the Message Processor reports the problem. The designer can then use the Message Processor to locate the time at which the problem occurred in the Waveform Editor and to locate the error in the original design file.

For easy comparison, the designer can superimpose the results of two simulations in the Waveform Editor.
**Functional Simulation**

The MAX+PLUS II Simulator supports functional simulation to test the logical operation of a project before it is synthesized, thereby allowing the designer to quickly identify and correct logical errors. The MAX+PLUS II Waveform Editor displays the results of functional simulation and provides easy access to all nodes in the project, including combinatorial functions.

**Timing Simulation**

In a timing simulation, the MAX+PLUS II Simulator tests the project after it has been fully synthesized and optimized. Timing simulation is performed at 0.1-ns resolution.

**Multi-Device Simulation**

MAX+PLUS II can combine the timing and/or functional information from multiple Altera devices, allowing the designer to simulate several devices operating together. Devices from different Altera device families can be used in the same project.

**Timing Analysis**

The MAX+PLUS II Timing Analyzer can calculate a matrix of point-to-point device delays, determine setup and hold time requirements at device pins, and calculate maximum clock frequency. MAX+PLUS II design entry tools are integrated with the Timing Analyzer, allowing the designer to simply tag start and end points in the design files or the Floorplan Editor to determine the shortest and longest propagation delays. In addition, the Message Processor can locate and display critical paths identified by the Timing Analyzer in the source design files or in the Floorplan Editor. See Figure 8.
**Device Programming**

The MAX+PLUS II Programmer, shown in Figure 9, uses programming files generated by the MAX+PLUS II Compiler or PLDshell Plus compiler to program Altera devices. The Programmer allows the designer to program, verify, examine, blank-check, and functionally test devices.

Altera provides all hardware and software necessary for programming and verifying devices, including a Logic Programmer Card and Master Programming Unit (MPU). The add-on Logic Programmer card (for PC-AT or compatible computers) drives the MPU. The MPU performs continuity checking to ensure adequate electrical contact between the programming adapter and the device. With the appropriate programming adapter, the MPU also supports functional testing, so that vectors created for simulation can be applied to a programmed device to verify its functionality.
Altera also provides the FLEX Download Cable and the BitBlaster for device programming and configuration. The FLEX Download Cable can connect any Configuration EPROM programming adapter, which is installed on the MPU, to a single target FLEX 10K or FLEX 8000 device in a prototype system. The BitBlaster serial download cable is a hardware interface to a standard PC or UNIX workstation RS-232 port that provides configuration/programming data to FLEX 10K, FLEX 8000, MAX 9000, MAX 7000S, and FLASHlogic devices on system boards. The BitBlaster also allows users to configure a FLEX 10K or FLEX 8000 device independent of the MAX+PLUS II Programmer.

With the BitBlaster, designers can also configure/program multiple FLEX 10K, FLASHlogic, MAX 9000, and MAX 7000S devices using the multi-device JTAG chain mode and the MAX+PLUS II Programmer.

For more information on the BitBlaster, Altera programming hardware and software, other programming hardware manufacturers, or multi-device JTAG chain programming and configuration, refer to the following sources:

- **BitBlaster Serial Download Cable Data Sheet** in this data sheet
- **Altera Programming Hardware Data Sheet** in this data sheet
- **Programming Hardware Manufacturers** in this data sheet
- “Setting Up Multi-Device JTAG Chains” in MAX+PLUS II Help
On-Line Help

On-line help provides access to all information on MAX+PLUS II. It includes complete, up-to-date documentation on all MAX+PLUS II applications, causes and suggested actions for messages, references to related Altera documentation, text file formats (e.g., AHDL), and information on Altera devices and adapters.

On-line help is only a keystroke or a mouse click away. The F1 key provides instant access to information on a dialog box, highlighted menu command, or pop-up message. Typing Shift+F1 or choosing the context-sensitive help button on the toolbar turns the mouse pointer into a question mark pointer that allows the designer to click on any item on the screen—including logic functions and AHDL keywords—for context-sensitive help on that item.

Software Maintenance Agreement

To guarantee timely upgrades for software and documentation, Altera offers a Software Maintenance Agreement that entitles the customer to software updates, discounts on selected software products, and Applications Engineering support.

Recommended System Configurations

To run MAX+PLUS II software with optimum results, Altera recommends the following system configurations:

PC System Configuration

- Pentium-based PC-AT or compatible computer
- The following shows the available memory requirements (i.e., combined RAM and virtual memory) for Altera device families:
  - FLEX 10K devices, 128 Mbytes of available memory, including 64 Mbytes of RAM
  - FLEX 8000 devices, 64 Mbytes of available memory, including 32 Mbytes of RAM
  - MAX 9000 devices, 64 Mbytes of available memory, including 32 Mbytes of RAM
  - All other devices, 32 Mbytes of available memory, including 16 Mbytes of RAM
- Microsoft Windows NT version 3.51 or higher, Windows 95, Windows version 3.1, or Windows for Workgroups version 3.11
- Microsoft Windows-compatible graphics card and monitor
- CD-ROM drive
- Microsoft Windows-compatible 2- or 3-button mouse
- Full-length 8-bit ISA slot for a Logic Programmer card
- Parallel port
- RS-232 serial port for the BitBlaster
Sun SPARCstation System Configuration

- Sun SPARCstation with color monitor
- 32 Mbytes of RAM (for FLEX 10K and large FLEX 8000 device projects, 64 Mbytes of RAM)
- Sun OS 4.1.2 or higher
- Sun OpenWindows 3.0 or higher
- Solaris 2.4 or higher
- ISO 9660-compatible CD-ROM drive
- RS-232 serial port for the BitBlaster

HP 9000 Series 700 Workstation System Configuration

- HP 9000 Series 700 workstation with color monitor
- 32 Mbytes of RAM (for FLEX 10K and large FLEX 8000 device projects, 64 Mbytes of RAM)
- HP-UX version 9.03 or higher
- HP-VUE
- ISO 9660-compatible CD-ROM drive
- RS-232 serial port for the BitBlaster

IBM RISC System/6000 Workstation System Configuration

- IBM RISC System/6000 workstation with color monitor
- 32 Mbytes of RAM (for FLEX 10K and large FLEX 8000 device projects, 64 Mbytes of RAM)
- AIX version 3.2.5 or higher
- AIX Windows version 1.2.5 or higher
- ISO 9660-compatible CD-ROM drive
- RS-232 serial port for the BitBlaster

Go to the MAX+PLUS II read.me file for the most-up-to-date information regarding system requirements.

Software Package Options

Altera offers a variety of tool configurations and add-on migration products for PC- and UNIX workstation-based versions of MAX+PLUS II. In addition, any customer who purchases a PC-based MAX+PLUS II software product receives a site license to install an unlimited number of copies of the PLS-ES feature set for the MAX+PLUS II development software.

For up-to-date information on MAX+PLUS II software packages and development systems, contact your local sales representative or Altera Literature Services.
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