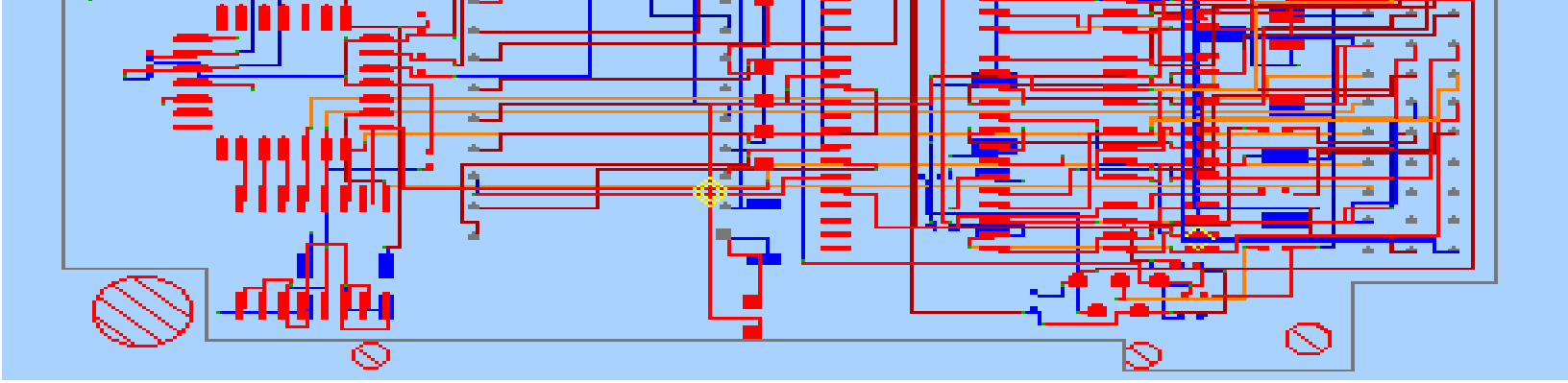

MicroSim PCBoards Autorouter

User's Guide

Index

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How to Use This Online Manual

Use this icon or toolbar button...	To do this...
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	Go back and forth between views.
Previous Chapter	Go back to the previous chapter.
Next Chapter	Go to the next chapter.
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Next Chapter

Welcome to MicroSim

Welcome to the MicroSim family of products. Whichever programs you have purchased, we are confident that you will find they meet your circuit design needs.

The MicroSim family of products is fully integrated, giving you the flexibility to work through your circuit design in a consistent environment. They provide an easy-to-use environment for creating, simulating, and analyzing your circuit designs from start to finish.

Overview

PCBoards provides an integrated interface to Cooper & Chyan Technology's (CCT) SPECCTRA autorouter. You can run an autorouting session directly from the PCBoards Layout Editor without additional setup. Or, through PCBoards' dialog interface, you can define layout rules that constrain SPECCTRA's operation. Rules can apply to the entire board, to individual nets, and/or to specific routing layers.

The number of board layers and autorouting features available to you depends on the package you have purchased. MicroSim PCBoards with Autorouter is available in four configurations:

- 2 layer/1000 pins
- 4 layer/4000 pins
- 6 layer/unlimited pins
- unlimited layers/unlimited pins

In addition, the autorouter can be purchased with any of the four options listed below:

Autorouter Option		Capabilities
ADV	Advanced	Considers per-layer trace properties and custom via-net associations
DFM	DFM	Establishes test points, miters corners, and spreads traces after routing
HYB	Hybrid	Supports custom blind/buried vias and via placement under SMT pads
FST	Fast Circuit	Supports rules to prevent coupled noise and timing problems

The symbols shown to the left of each option appear throughout the autorouting chapters in conjunction with features that are only available with the identified option.

The EditRoute option

EditRoute, Cooper & Chyan Technology's shape-based tool for interactive routing, is also available as an option to PCBoards. EditRoute can be used either stand-alone or in conjunction with the SPECCTRA autorouter. EditRoute uses many of the autorouting features of SPECCTRA to push blocking traces and vias out of the way as routes are interactively added or moved.

Typographical Conventions

This guide is designed so you can quickly find the information you need to use the PCBoards Autorouter. This guide assumes that you are familiar with Microsoft Windows (95 or NT), including how to use icons, menus and dialog boxes. It also assumes you have a basic understanding about how Windows manages applications and files to perform routine tasks, such as starting applications and opening and saving your work. If you are new to Windows, please review your Microsoft Windows User's Guide.

This guide generally follows the conventions used in the Microsoft Windows User's Guide. Procedures for performing an operation are generally numbered with the following typographical conventions.

Notation	Examples	Description
`monospace font`	`analog.slb` or `clipper.sch`	Library files and file names.
Ctrl+R	Press Ctrl+R	A specific key or key stroke on the keyboard.
`monospace font`	Type `VAC`...	Commands/text entered from the keyboard.

Online Help

Pressing F1 or selecting Contents from the Help menu brings up an extensive online help system.

The online help includes:

- Step-by-step instructions on how to use the PCBoards Autorouter features.
- Reference information about the PCBoards Autorouter.
- Technical Support information.

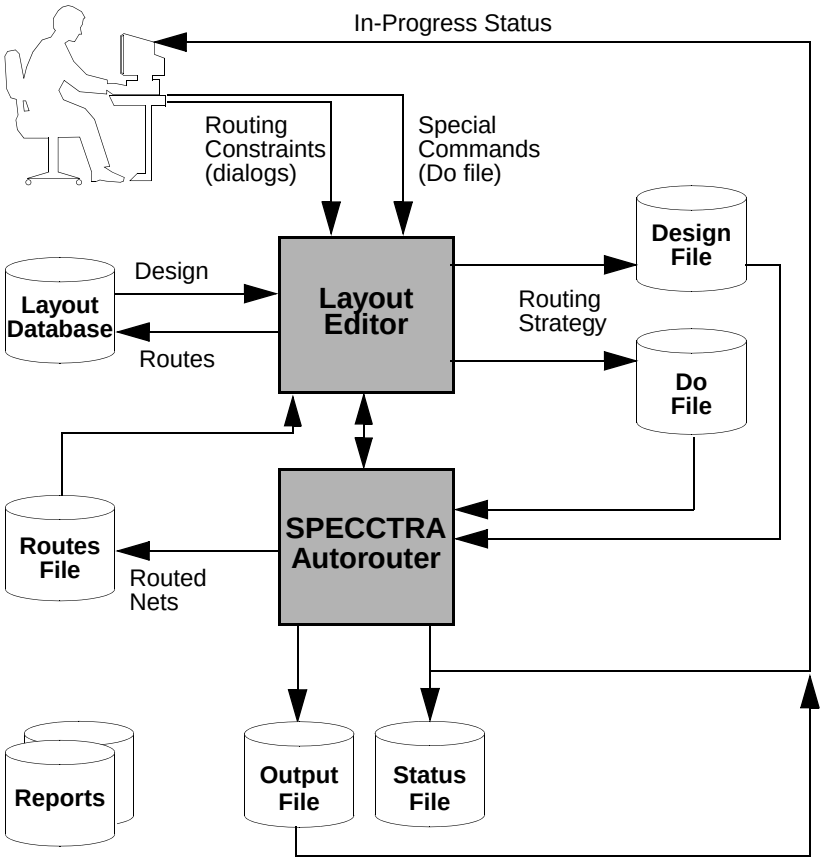
If you are not familiar with Windows (95 or NT) Help System, select How to Use Help from the Help menu.

Understanding Autorouting Basics

Introduction

Using shape-based technology, SPECCTRA models SMT pads, through-pins, traces, and other layout objects as geometric shapes. Each shape has corresponding rules for clearances, trace widths, and other constraints to which the routed design must ultimately adhere. On the first pass, SPECCTRA attempts to route all connections by allowing routing conflicts. Each subsequent pass modifies existing routes using rip-up and retry techniques that continuously reduce the number of conflicts until they have all been eliminated.

The figure illustrates the relationship between the user, the Layout Editor, the SPECCTRA autorouter, and the various files involved with autorouting.



Design File

Contains board structure (layers, boundary, via-padstack associations, rules, and grid definitions), component placement (locations and reference designators), component footprint and padstack definitions, connections, and preroutes (interactively drawn traces and trace segments). Default file name is `<layout database name>`.CCT.

Do File

Contains strategy and control commands. PCBoards creates a default Do file. For special cases, this file can be edited. See **Custom Setup and Strategies—Using the Do File** for a more detailed description of the Do file and how to use it. Default file name is `<layout database name>`.DO.

Status File

Contains summary information reflecting routing progress per pass: conflicts, successful routes, failures (for rip-up and reroute), remaining connections, number of vias, crosstalk rules violations, length violations, and percentage reduction in conflicts. Default file name is `<layout database name>`.STS.

Output File

Contains an audit trail of applied design rules, invoked SPECCTRA commands, and routing progress. This file is dynamically updated by the autorouter. Default file name is `<layout database name>`.CCO.

Reports

Reports can be optionally generated on a variety of subjects. Output can be either to a file or to the monitor. This requires adding `report` commands to the Do file. Refer to **Generating Reports (Do File)** for more information.

Routes File

Reflects the currently routed connections. This file is dynamically updated by the autorouter. Default file name is `<layout database name>`.RTE.

Before autorouting can begin, PCBoards translates the Layout Database into the Design file. PCBoards then takes the design constraints entered into the Tools/CCT: Setup and Tools/CCT: Net Rules dialogs (and subdialogs) and generates appropriate commands and rules which are saved to the Design file and Do file.

For typical designs, setup through the dialogs is sufficient and the autorouter can be invoked. By default, PCBoards uses the smart-route technique (**Default Setup and Smart-Route Strategy**) which permits SPECCTRA to examine the design with each pass and adapt routing to the layout's current state.

As initialization and autorouting proceed, audit trail and status information is displayed in the SPECCTRA window for immediate evaluation. All of SPECCTRA's responses are logged to the Output file providing a complete history of the autorouting run; the on-screen information can be reviewed at any time by scrolling up and down within the Output subwindow. An up-to-date autorouting summary is logged to the Status file and can also be viewed while routing is in progress.

Routed nets are saved to the Routes file. Once routing is complete, the final routing information can be read from the Routes file and written to the Layout Database.

Adaptive Autorouting

SPECCTRA uses a routing algorithm that attempts to route all connections in the first pass by allowing clearance and crossover violations. Conflicts are eliminated in subsequent routing passes using rip-up and retry techniques.

The number of conflicts after the first pass is typically three to four times the total number of connections. Conflicts are graphically marked with a conflict box or diamond as shown below.

Clearance Conflict **Crossover Conflict**

During passes two through five, conflict costs increase while SPECCTRA rips up and reroutes *every* connection. After the fifth pass, only connections involved in conflicts and connections in the area of conflicts are ripped up and rerouted. With the sixth and subsequent passes, SPECCTRA attempts to eliminate all remaining conflicts and achieve 100% completion.

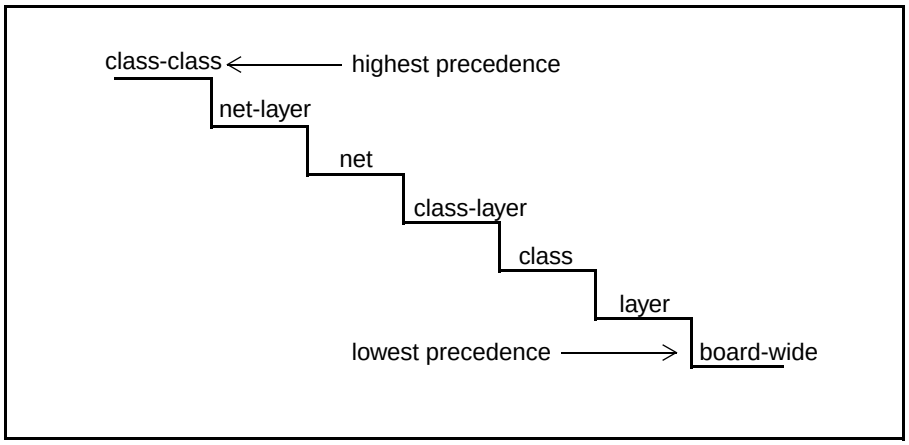
If SPECCTRA cannot find a path for a connection, a failure occurs. Failures are monitored and recorded in the Status file. For pass one, failures are left unrouted. For subsequent passes, failures may consist of unrouted connections and traces that cannot be rerouted. If SPECCTRA encounters a situation where the number of conflicts reduces very slowly and there are more than 50 failures, it automatically removes the gridlocked traces and continues.

When autorouting difficult designs, as many as 100 (or more) routing passes may be required to eliminate conflicts.

Electrical Rules Handling

The PCBoards interface to SPECCTRA supports electrical rules for individual nets, classes of nets, layers, and board-wide. When rules are defined at these various levels, SPECCTRA automatically determines which rules have precedence as illustrated below. Board-wide rules have the lowest precedence in the event of contention; rules at all other levels override the board-wide rules. Rules between net classes have highest precedence.

Electrical Rules Hierarchy



Default Setup and Smart-Route Strategy

By default, PCBoards uses SPECCTRA's built-in smart-route strategy to route the design using the settings specified in the Tools/CCT: Setup dialog and Tools/CCT: Net Rules dialog and subdialogs.

Setup Through Dialogs

When invoking the Tools/CCT: Setup and Net Rules dialogs for the first time, initial values are determined by the current trace style used for interactive routing (as set using the Styles drop-down list in the toolbar). Layer and padstack definitions created using the appropriate Configure menu selection also compose the selection lists provided in these dialogs.

However, the settings for autorouting are managed separately from those for interactive routing. The latest autorouting strategy is saved with the design and can be refined for future autorouting runs. Any changes made within the CCT dialogs have no effect on settings made within the Configure menu or toolbar drop-down lists.

Board-wide setup

Board-wide routing controls are defined in the Tools/CCT: Setup dialog. These include: default trace properties (width, clearance, via padstack), grid size for routing and vias, routing

style, connection rules, layer pairs, and trace topology constraints. These rules apply to nets that do not have existing layout rules as defined in the Layout Database (trace segment attributes) or in the Tools/CCT: Net Rules dialogs.

Net-, layer-, and function-specific setup

Routing controls can be specified per net, per net-class, per-layer, and to meet special requirements such as manufacturability, test, hybrid circuit, and high-speed design. These relationships are defined in the Tools/CCT: Net Rules dialog and subdialogs. Settings made in these dialogs override the default settings specified in the Tools/CCT: Setup dialog.

The option-specific dialogs are summarized here:

ADV
- Per-layer trace properties and net-via associations are set in the Tools/CCT:Net Rules/Adv dialog (Advanced option required).

DFM
- Manufacturability and test requirements are specified in the Tools/CCT: Net Rules/DFM dialog (DFM option required). These settings are used to adjust the layout after routing is complete. Includes rules for establishing test points, mitering corners, and spreading traces.

HYB
- Special via controls are specified in the Tools/CCT: Net Rules/Hyb dialog (Hybrid option required). These settings define rules for via placement under SMT pads, and blind and buried vias.

FST
- Rules affecting signal integrity in high speed designs are specified in the Tools/CCT: Net Rules/Fst dialog (Fast Circuit option required). These settings are used to control coupled noise and control timing.

How Does Smart-Route Work?

When in smart-route mode, SPECCTRA evaluates the design, then chooses and runs the appropriate SPECCTRA autorouting commands to produce the best possible completion rate. Strategy determination is dynamic based on the conflict reduction rate, the routing completion rate, the failure rate, and the number of layers.

Smart-route does the following:

- Sets the trace and via grids to the spacings specified in Tools/CCT: Setup dialog
- Performs fanout if there are enough signal layers, or if the [Top] and [Bottom] signal layers are excluded from routing
- Changes the grid to achieve optimum fanout
- Applies bus routing
- Runs standard routing passes
- Provides warning and error messages to help analyze difficult board designs
- Runs four clean passes
- Stops autorouting if the board design will not converge

Custom Setup and Strategies—Using the Do File

When the smart-route strategy isn't sufficient to fully route the design, it is necessary to edit the Do file and insert appropriate SPECCTRA commands. Refer to **Setting Up Autorouter Runs** for discussions on specific cases where Do file commands must be used. Refer to the **CCT Design Language Online Reference Manual** for a comprehensive description (including syntax) of all available Do file commands.

What Is the Do File?

The Do file is an ASCII file that contains a sequence of SPECCTRA autorouter commands. The selection and ordering of these commands is very important. The figure below shows an example of the default Do file generated by PCBoards.

Default Do File

```
# Do file produced by MicroSim PCBoards
# for Board Layout -- C:\CIRCUITS\PCBEX2 --
# on Fri Jun 30 06:45:43 1995

# Initial commands

# Routing commands
bestsave on C:\CIRCUIT\PCBEX2.wre
status_file C:\CIRCUIT\PCBEX2.sts
bus diagonal
smart_route

#DFM commands

#Final commands
write routes C:\CIRCUIT\PCBEX2.rte
```

Adding Commands to the Do File

The Do file is opened for editing by selecting Tools/CCT: Edit Do File. Setup commands, (like unit and grid_smart) should be inserted into the #Initial `commands` section. Alternative routing strategy commands (`route` and `clean`) should be inserted into the `#Routing commands` section. Output commands (like `report`) belong in the `#Final commands` section.

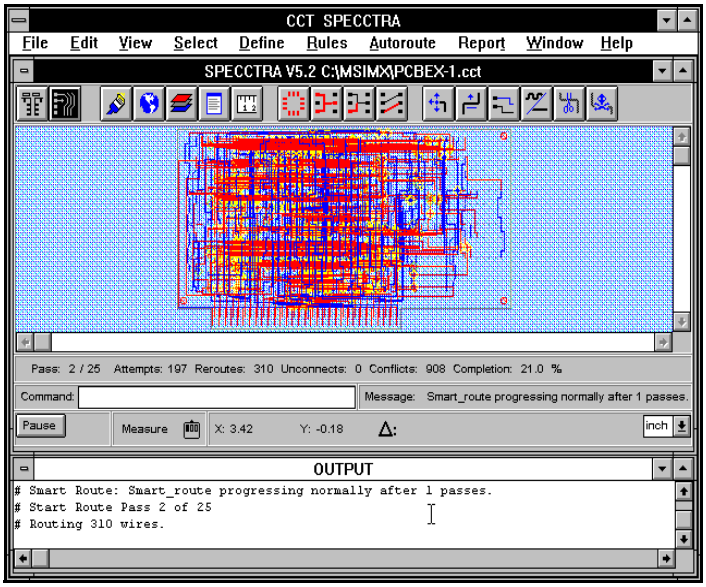
In the case of an alternative routing strategy, the `smart_route` command must be commented out. For example, the following sample Do file replaces the `smart_route` command with a sequence of `route` and `clean` commands. A `report` command is added after routing is completed to generate a summary of the design rules.

Custom Do File

```
# Do file produced by MicroSim PCBoards
# for Board Layout -- C:\CIRCUITS\PCBEX2 --
# on Fri Jun 30 06:45:43 1995

# Initial commands

# Routing commands
bestsave on C:\CIRCUIT\PCBEX2.wre
status_file C:\CIRCUIT\PCBEX2.sts
bus diagonal
# smart_route
route 25
clean 2
route 50 16
clean 4

#DFM commands

#Final commands
write routes C:\CIRCUIT\PCBEX2.rte
report rules
```

The SPECCTRA Window

When autorouting commences, the SPECCTRA window displays on the monitor similar to the screen shown below.



The main window is comprised of two internal windows

- The SPECCTRA subwindow with in-progress graphical display of the current autorouting run. Controls are provided to pause and abort the run when it is deemed necessary to change the design and/or routing constraints to achieve 100% completion.
- The Output subwindow providing a text audit trail of the currently executing SPECCTRA commands and autorouting status. Text written to this window is logged to the Output file.

Most of the autorouting rules defined using PCBoards dialog controls are saved to the Design file (.cct), not the Do file (.do). Rules entered directly into the Do file override corresponding rules, if any, that were previously established in the Design file using PCBoards.

Setting Up Autorouter Runs

Steps to Set Up Autorouting

These steps are required to set up and run the SPECCTRA autorouter:

1. If not already specified, define the region where routing is allowed using Draw/Board Signal Keepin. (Refer to the MicroSim PCBoards User's Guide.)
2. If not already specified, draw power and ground planes using Draw/Areafill (Refer to the MicroSim PCBoards User's Guide.).
3. Define board-wide routing controls (e.g., default trace width and clearance, trace and via grids, routing styles, connection control, layer pairs, etc.) in the Tools/CCT: Setup dialog.
4. Define basic electrical rules (per net and/or net class), and, depending on the installed options, electrical rules for layers, DFM, hybrid circuits, and fast circuits (signal integrity) in the Tools/CCT: Net Rules dialog and sub-dialogs.
5. If required, update the Do file through Tools/CCT: Edit Do File for special functions like protecting nets/traces, redefining the number of routing passes, and redefining the number of clean-up passes.
6. Start the autorouter by selecting Tools/CCT: Autoroute.
7. Evaluate status information displayed on screen. If unsatisfactory, abort run by clicking Pause followed by Stop within the SPECCTRA window, and repeat steps 2-5 to refine the strategy. (See **Evaluating/ Troubleshooting Autorouting Results**.)
8. If Auto-complete CCT (in the Tools/Options dialog) is disabled, then, when autorouting successfully completes, select Tools/CCT: Read Routes to add the routed nets to the Layout Database. If Auto-complete CCT is enabled (the installed default), and SPECCTRA has finished, PCBoards automatically reads in the completed routes.

Defining the Trace and Via Grids

So that board space is used efficiently, the trace and via grids should be set to values that are compatible with component pin spacing, trace width, and clearance. The trace grid should be set to the smallest value consistent with the layout. Via grid size is sometimes set proportionally larger than routing grid size to create less dense placement of vias and thus, save space.

Defining Trace Grids

A single trace grid can be used for the entire board. Or, for more complex designs, different grid spacings can be assigned to different layers. These are specified in the Trace Grid frame. The same grid(s) is/are used for all routing passes.

To use a single trace grid

1. Select Tools/CCT: Setup.
2. Enter the spacing between grid points in the Spacing text box.
3. Click OK.

To use a different trace grid for different signal layers

1. Select Tools/CCT: Setup.
2. Enter the spacing between grid points in the Spacing text box.
3. Select one or more layers in the Apply to Layer list box.
4. Click Apply to Layer.
5. Click OK.

Defining Via Grids

A single via grid can be used for the entire board. Or, for more complex designs, different via-padstack combinations can utilize different grid spacings. The latter case applies to installations with the Advanced and Hybrid options.

Note that the choice of a smart via grid versus a constant via grid depends on the routing strategy that is employed. See the next section for details.

To use a single via grid

1. Select Tools/CCT: Setup.
2. Enter the spacing between grid points in the Spacing text box.
3. Click OK.

HYB To use a different via grid for a given via-padstack combination

ADV
1. Select Tools/CCT: Setup.
2. Enter the spacing between grid points in the Spacing text box.
3. Select a padstack definition in the Apply to Via list box.
4. Click Apply to Via.
5. Click OK.

If additional padstack definitions are required, use Configure/ Padstacks to create new definitions.

Defining a “Smart” Via Grid versus “Constant” Via Grid (Do File)

To avoid creating via barriers, help distribute vias, and leave space for placing vias in later routing passes, SPECCTRA provides a smart via grid feature that varies the grid spacing between passes to improve routing efficiency. SPECCTRA computes a larger initial grid for the first three passes, then reverts to the specified minimum grid spacing for subsequent passes.

Alternatively, SPECCTRA can enforce a constant via grid. The choice depends on the routing strategy. When using the default smart-route strategy, a smart via grid is automatically employed. When using custom strategies (with `route` commands in the Do file), a constant via grid is employed; in this case, the constant via grid can be overridden by inserting the `grid smart` command in the Do file.

To use a constant via grid

1. Select Tools/CCT: Edit Do File.
2. Change the `smart_route` command that appears in the `#Routing commands` section of the Do file to a combination of `fanout`, `route`, and `clean` commands.
3. The grid spacing specified in the Tools/CCT: Setup dialog applies to all routing passes.
4. Select File/Save then File/Exit to save and close the file.

To use a smart via grid when using a custom routing strategy

1. Select Tools/CCT: Edit Do File.
2. Verify that one or more `route` commands appear in the `#Routing commands` section of the Do file.
3. Insert the `grid smart (via <dimension>)` command into the `#Initial Commands` section setting `<dimension>` to the minimum grid spacing that should be used after the third pass.
4. This `grid smart` command overrides the `grid` command PCBoards saved to the Design file.
5. Select File/Save then File/Exit to save and close the file.

Setting Net Rules

The board-wide settings specified in the Tools / CCT: Setup dialog and rules specified using net attributes in the Layout Editor, can be overridden per net and per net class in the Tools / CCT: Net Rules dialog and subdialogs.

Defining Net Classes

When identical rules are to be assigned to multiple nets, it is convenient to group the nets into a class. Later, the class name can be selected for rule assignment in the Apply Rules To frame available in many of the dialogs.

To create a net class

1. Select Tools/CCT: Net Rules.
2. Choose Edit Classes in the Apply Rules To frame. A subdialog is displayed.
3. Type a name for the class in the Class Name text box.
4. Click two or more net names in the nets list box on the left. If most of the nets are to be included, click Select All, then click off the entries to be excluded from the set.
5. Click Add.

Assigning Rules to Nets or a Net Class

Rules can be assigned to multiple nets or to one net class.

To assign a rule to one or more nets

1. Invoke the Tools/CCT: Net Rules dialog, or, from within the CCT Net Rules dialog, choose ADV, DFM, or FST.
2. In the Apply Rules To frame, either:
   - Click on one or more entries in the Net(s) list box. The Net(s) option button is automatically selected. If most of the nets are to be included, click Select All, then click on the entries to be excluded.
   - Or, click on an entry in the Net Class list box. The Net Class option button is automatically selected.
3. Enter net properties and click the appropriate Set <xxx> button within the dialog. Each time the Set <xxx> button is chosen, a new rule is added for the currently selected net(s) or net class. The rule applies to all nets selected or contained in the net class.

Enabling/disabling routing on nets

PCBoards provides controls to fix nets (routed or unrouted) so that they are ignored during autorouting. There is also a way to protect existing routes from rerouting. The main difference between the two is that the autorouter will route to protected traces, but not to fixed traces. These are described in the following sections.

Fixing nets

It is sometimes useful to autoroute specific nets in the design, while excluding all others. For example, when routing a multi-layer SMT board without ground and power planes, it is recommended to first route the VCC and GND nets before anything else. The autorouter can be run once with selected nets enabled while all others are disabled. Then, a follow-on run can be invoked with the remaining nets enabled.To prevent fully or partially routed nets from rerouting and connecting to new routes, do either of the following:

To prevent fully or partially routed nets from rerouting and connecting to new routes, do either of the following

From within the Layout Editor work area

1. Double-click on a trace segment, or highlight multiple trace segments and click  Edit/Attributes.
2. Click on the NET_FIXED attribute.
3. Set the Value control to YES.
4. Click Change.
5. Click OK.

To exclude routing on unrouted nets

Select Tools/CCT: Net Rules.

6. Select the net name(s) or net class name in the Apply Rules To list box.
7. Choose the On option button in the Net Attributes frame.
8. Click Set Fixed.
9. Repeat steps 2-4 until all nets to be excluded have been set.

Protecting routed nets (Do File)

SPECCTRA can be prevented from disturbing existing trace segments (routing barriers) while still being able to complete any unrouted portions of a net. This requires using the protect command in the Do file.

To prevent rerouting existing trace segments but still allow connection with new routes

1. Select Tools/CCT: Edit Do File.
2. Add the required commands to the #Initial Commands section as follows:
   a. To prevent all routed nets from rerouting:

   Insert a protect all wires command.

   b. To prevent selected routed nets from rerouting:
   c. Insert one or more protect net <net name> commands and/or protect class <net class name>.
   d. To prevent rerouting fanout vias and traces:
   e. Insert a protect all wires (attr fanout) command.
   f. To prevent rerouting bus vias and traces:
   g. Insert a protect all wires (attr bus) command.
   h. To prevent rerouting test point vias and traces:
   i. Do nothing. Testpoints, by default, are protected.
3. Select File/Save then File/Exit to save and close the file.

Use the unprotect command to reverse these effects. See the protect/unprotect command description in the **CCT Design Language Online Reference Manual** for more variations.

Defining Trace Properties

Controls defining the physical properties, geometry limits, and pin/via limits for traces can be defined globally for all nets on the board. Net-specific values can also be defined which override the global settings. In addition, a given net can be assigned different width and clearance values depending on the layer used for routing.

To set global trace properties

1. Select Tools/CCT: Setup.
2. In the Default Settings frame, enter values for Width and Clearance.
3. In the Net Control frame, enter values for the controls as needed.
4. In the Pin/Via Control frame, enter values for the controls as needed.

To set trace properties for a net or net class routed to any layer

1. Select Tools/CCT: Net Rules.
2. In the Apply Rules To frame, select the relevant net(s) or net class.
3. In the Set Width edit control, enter a width value and click Set Width.
4. In the Set Clearance edit control, enter a clearance value and click Set Clearance.
5. In the Net Control frame, enter values for the controls as needed and click Set Rules.
6. In the Pin/Via Control frame, enter values for the controls as needed and click Set Rules.

ADV To set trace properties for a net or net class routed to a specific layer

1. Select Tools/CCT: Net Rules.
2. Choose ADV.
3. In the Apply Rules To frame, select the net(s) or net class to which the override properties are to be assigned.
4. In the Layer Width Control frame, enter values for Width and Clearance, select one or more layers in the list box, and click Set for Layer(s).

Enabling/Disabling Routing of Nets on Layers

For one or more nets, controls are provided which govern whether or not a layer is available for routing.

ADV To use fewer routing layers than configured

1. Select Tools/CCT: Net Rules.
2. Choose ADV.
3. In the Apply Rules To frame, click Select All. Subsequent rule settings will be assigned to all nets in the design.
4. In the Layer Routing Control frame, select the layer names on which routing is allowed. Consecutive clicks on an entry will toggle between selected (highlighted) and unselected (unhighlighted).
5. For example, to prevent routing on the surface layers, highlight all of the layer names in the list except the [Top] layer (named Component by default) and the [Bottom] layer (named Solder by default).
6. Click Set Layer(s) for Net(s).

If SMT components are mounted on a layer that has been disabled for routing, SPECCTRA automatically generates escapes from the pins to access internal layers.

ADV To route a net or net class on specific layers

1. Select Tools/CCT: Net Rules.
2. Choose ADV.
3. In the Apply Rules To frame, select the net(s) or net class to be routed on a specific layer.
4. In the Layer Routing Control frame, select the layer name(s) on which routing is allowed.
5. Click Set Layer(s) for Net(s).

Controlling Via Use

PCBoards provides controls governing whether SPECCTRA can use vias to route connections, or to limit the total number of vias used.

To limit the maximum number of vias for any connection and any net

1. Select Tools/CCT: Setup.
2. Enter the via limit value for a pin-to-pin connection in the Max Vias per Connection text box.
3. Enter the via limit value for any net in the Max Vias per Net text box.

To disallow vias for a net or net class

1. Select Tools/CCT: Net Rules.
2. In the Apply Rules To frame, select the relevant net(s) or net class.
3. Enter 0 in the Max Vias per Net text box.

To disallow vias for the entire design

1. Select Tools/CCT: Net Rules.
2. In the Apply Rules To frame, click Select All.
3. Enter 0 in the Max Vias per Net text box.

ADV To set specific vias for a net or net class

1. Select Tools/CCT: Net Rules.
2. Choose ADV.
3. In the Apply Rules To frame, select the relevant net(s) or net class.
4. In the Via Control frame, choose the appropriate padstack definition and click Set Via Padstack.
5. New padstack definitions can be added to this list using Configure/Padstacks.

HYB To set the padstack style used for blind and buried vias

1. Select Tools/CCT:Net Rules.
2. Choose HYB.
3. Enable the Use Blind and Buried Vias check box.
4. In the Use Padstack(s) list box, select the padstack style from which all blind/buried via padstacks should be derived.
5. If required, enter a value for the Buried Via Gap.
6. Click OK.

Refer to **Autorouting SMT Designs** for more on via use in SMT designs.

Improving Manufacturability

PCB manufacturability can be improved by (1) increasing trace clearances, and (2) eliminating 90-degree corners (mitering). PCBoards with the DFM option provides controls permitting the autorouter to make these cleanup attempts after routing has been completed.

Increasing Trace Clearances

SPECCTRA attempts to incrementally increase the designated trace clearances using the specified values. If spreading a trace would result in a conflict, it is *not* repositioned. Also, vias are not moved or removed.

DFM To spread out traces

1. Select Tools/CCT: Net Rules.
2. Choose DFM.
3. Define delta values to use when incrementing clearance values (by default, half the via/pin clearance value defined in the CCT Setup dialog)

   To attempt a single increment that is one-half the current clearance value:

   a. Enter 0 in the Try Amount text box.

   b. Enter 0 in the Smallest Amount text box.

   To attempt a single specific increment:

   a. Enter the increment value in the Try Amount text box.

   b. Enter 0 in the Smallest Amount text box.

   Or, to attempt progressive increments within a range:

   a. Enter the starting increment in the Try Amount text box.

   b. Enter the smallest increment in the Smallest Amount text box.

   The autorouter will successively divide the last used increment (starting with Try Amount) by two and attempt to spread out the traces. When the increment value is less than Smallest Amount or five passes have been made, the autorouter will stop making attempts.
4. Identify which traces should be attempted by checking the appropriate Wire-Pin, Wire-SMT, and/or Wire-Via boxes. If none of the boxes are checked, all traces are attempted.
5. Click Spread Out Traces.
6. If different increment values are to be used for the different Wire-Pin, Wire-SMT, or Wire-Via combinations, repeat steps 3-5, checking the appropriate box each time.

Mitering Corners

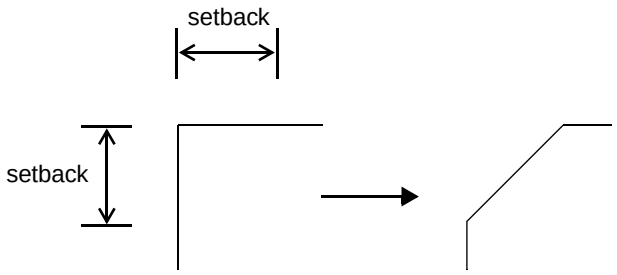
SPECCTRA attempts to replace 90-degree corners with 135-degree bends while adhering to the setback values (X and Y dimension of the 135-degree trace segment) specified in the dialog. Setback constraints can be defined board-wide or for specific layers.

Miter types and setback

SPECCTRA distinguishes between four types of 90-degree corners as described below. All or any subset of these geometries can be the target of a mitering attempt.

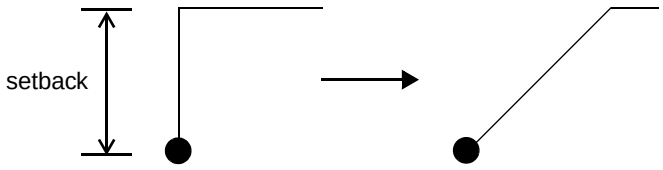
Bends

refer to any two orthogonally joined trace segments. Mitering is performed incrementally. On the first pass, the maximum allowable setback value is attempted on all candidate 90-degree corners. Another attempt is made using half the value of the previous setback value on all remaining 90-degree corners that did not satisfy the first pass. This process continues until the calculated setback value is less than the minimum setback value allowed. The default minimum setback is the trace width; the default maximum setback is one-half inch.



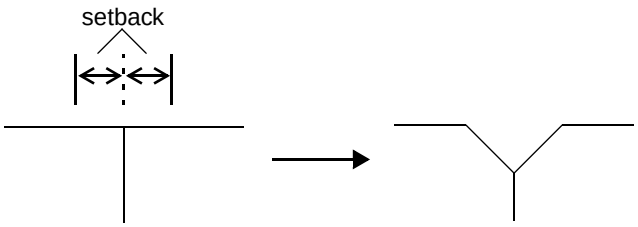
Pin Exits

refer to the pin-to-corner trace segments. Mitering takes place if the trace segment leading from the pin is greater than or equal to the setback value. The pin setback distance is measured from the center of the pin to the turn. The default setback is one inch.



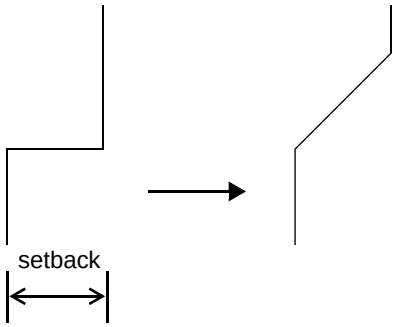
Tjunctions

refer to the three trace segments joined in a T. When mitered, the 135-degree cut begins at a distance away from the junction equal to the setback value. The default setback is one inch.



Slants

refer to wrong-way segments. Mitering takes place when the wrong-way length is equal to or greater than the setback value. The default setback is one inch.



Mitering

DFM

To miter all corner types using default setback values

1. Select Tools/CCT: Net Rules.
2. Choose DFM.
3. Establish mitering constraints as either board-wide or per layer.

   To set board-wide rules:

   a. Click Set Default Miters.

   Or, to set per-layer rules:

   a. In the Cleanup after Routing frame, select one or more applicable layer names in the list box at the bottom of the frame.

   b. Click Set Layer Miters.
4. If setting mitering rules per layer, repeat steps 3-4 for as many layer combinations as required.

DFM To miter selected corner types, or to use setback values other than the defaults

1. Select Tools/CCT: Net Rules.
2. Choose DFM.
3. For each corner type to be mitered:
   a. Check the box for the corner type
   b. Enter the corresponding setback value(s).
4. Establish mitering constraints as either board-wide or per layer.

   To set board-wide rules:

   a. Click Set Default Miters.

   Or, to set per-layer rules:

   a. In the Cleanup after Routing frame, select one or more applicable layer names in the list box at the bottom of the frame.
   b. Click Set Layer Miters.
5. If setting mitering rules per layer, repeat steps 3-4 for as many layer combinations as required.

Unmitering bends when applying ECOs (Do File)

When applying ECOs, it is best to replace all mitered corners with 90-degree corners. SPECCTRA can reroute orthogonal traces more efficiently.

DFM To unmiter corners

1. Select Tools/CCT: Edit Do File.
2. Insert the `unmiter` command in the `#Initial Commands` section.
3. Select File/Save.

   Refer to **Evaluating/ Troubleshooting Autorouting Results** for more on ECO handling when autorouting.

Setting Up Test Points

Test points can be established in two ways:

- Using SPECCTRA to establish an optimal set of test points according to specified constraints (described in this section). This technique requires the DFM option.
- Using the PCBoards Layout Editor to define test point attributes on existing pins and vias using Edit/Attributes (Refer to the MicroSim PCBoards User's Guide.).

Using SPECCTRA, test points can be established for the entire design or for a net class while minimizing the total number of required vias. First, SPECCTRA establishes only one test point per net. Second, existing through-hole pins can optionally be used. Third, test points are established after autorouting is complete. So existing vias are used where possible. Finally, SPECCTRA runs two clean passes after having established the test points to further reduce the number of vias (if possible).

DFM To establish test points using SPECCTRA

1. Select Tools/CCT: Net Rules.
2. Choose DFM.
3. Set whether test points are to be established for all nets or for selected nets. Set the Only for Netclass control as follows:

   To add test points to all nets:

   a. Uncheck the Only for Netclass box.

   Or, to add test points to specific nets:

   a. Check the Only for Netclass box.

   b. Select one net class name shown in the list box.
4. Set the remaining test point rules as required:

   By default, SPECCTRA sets the [Bottom] layer (named Solder by default) as the layer through which the test point is exposed (probing layer). Alternatively, the [Top] layer (named Component by default) or both layers can be specified as probing layers.
5. To change the probing layer to the [Top] only, uncheck the Solder box and check the Component box.

   The Use Padstack(s) list box displays padstack definitions that are currently available to the layout. If additional padstacks are required for test points, use Configure / Padstacks to create the new definitions.
6. To change the test via-padstacks, select a padstack definition in the Use Padstack(s) list box.

   Besides vias, existing through-hole pins can optionally be used as test points.
7. To allow through-hole pins as test points, check the Use Thru Pins box.
8. To use a grid different from the via grid for test point placement, check the Use Grid box.
9. Enter the test point grid spacing in the text box.

   Establish the test point rule as defined.

10 Click Add Testpoints.

11 If test points are defined per net class, repeat steps 3-9 as required.

Pre-existing test vias (manually defined using attribute settings or established in a previous autorouting run) are protected such that SPECCTRA cannot disturb them when autorouting.

DFM To allow SPECCTRA to adjust test vias

1 Select Tools/CCT: Edit Do File.

2 Insert an `unprotect all testpoints` command in the `#Initial Commands` section.

3 Select File/Save then File/Exit to save and close the file.

Generating Reports (Do File)

Autorouter data acquired during a run can be saved to ASCII text files or displayed in the Report window by using the appropriate `report` command in the Do file.

To output reports

1. Select Tools/CCT: Edit Do File.
2. Enter the appropriate report commands in the `#Final Commands` section of the Do file. The table below lists a useful subset of report commands using syntax that directs the report to a default file. Refer to the **CCT Design Language Online Reference Manual** for more detail and other report types.
3. Select File/Save and File/Exit to save and close the file

Report Command	Description
report class	Information on all defined net classes. (CLASS.RPT)
report component <reference designator>	Information on a single specified component. (COMP.RPT)
report conflict	Current routing conflicts in the design. (CONFLICT.RPT)
report corners	Number of corners and their angles. (CORNERS.RPT)
FST report crosstalk	Parallel (same layer) and tandem (adjacent layers) crosstalk rules and violations. (XTALK.RPT)
report length	Nets that have length and delay rules. (LENGTH.RPT)
report net <net name>	Information on a single specified net. (NET.RPT)
report network	Sorted statistics on all nets in the design. (NETWORK.RPT)
report no_fanout	SMT pads without escape vias after the last fanout attempt. (NOFANOUT.RPT)
report padstack	Padstacks in the design. (PADSTACK.RPT)
report rules	Current design rules in effect. (RULES.RPT)
report status	Routing summary and selected statistics. (STATUS.RPT) The output from this command is more detailed than that written to the default status file, <*layout database name*>.STS.
DFM report testpoint	Test vias and through-pin test points in the design. (TSTPT.RPT)
report unconnect	Unrouted connections. (UNCONN.RPT)
report vias	Vias in the design. (VIAS.RPT)

Autorouting High-Speed Designs

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Routing Differential (Balanced) Pairs

The autorouter can route any two nets in parallel. A specified gap is maintained except when avoiding obstacles or connecting to pins.

FST To route two nets in parallel

1. Select Tools/CCT: Net Rules.
2. Choose Fst.
3. In the Apply Rules To frame, select two net names in the Net(s) list box.
4. In the Paired Nets frame, enter the edge-to-edge spacing between the two nets in the Gap text box.
5. Click Set Differential Pair.

Controlling Impedance

PCBoards provides layer controls and trace width adjustments to control impedance.

ADV To assign high-speed nets to specific layers for routing

1. Select Tools/CCT: Net Rules.
2. In the Apply Rules To frame, select the net(s) or the net class for the rule.
3. Choose ADV.
4. In the Apply Rules To frame, select the net class created in step 2.
5. In the Layer Routing Control frame, select one or more applicable layers.
6. Click Set Layer(s) for Net(s).

ADV To control trace widths on a layer for all nets

1. Compute the trace width that satisfies the impedance requirement.
2. Select Tools/CCT: Net Rules.
3. Choose ADV.
4. In the Apply Rules To frame, choose Select All.
5. In the Layer Width Control frame:
   a. Enter the width computed in step 1 in the Width text box. (Enter a Clearance value if appropriate.)
   b. Select one or more layers in the Set for Layer(s) list box.
   c. Click Set for Layer(s).

ADV To control trace widths on a layer for a net class

1. Compute the trace width that satisfies the impedance requirement for the net class.
2. Select Tools/CCT: Net Rules.

3. If not already defined, create the net class with special width properties: in the Apply Rules To frame, choose Edit Classes, specify net class name and constituent nets, click Add, and click OK.
4. Choose ADV.
5. In the Apply Rules To frame, select the net class created in step 3.
6. In the Layer Width Control frame:
   a. Enter the width computed in step 1 in the Width text box. (Enter a Clearance value if appropriate.)
   b. Select one or more layers in the Set for Layer(s) list box.
   c. Click Set for Layer(s).

Preventing Coupled Noise

Coupled noise can be minimized in three ways:

- Limiting the lengths of parallel trace segments.
- Computing and responding to cumulative noise contributions between parallel trace segments.
- Shielding sensitive nets.

Defining Length Constraints (Non-Cumulative)

The simplest way to control coupled noise is to limit the lengths of parallel trace segments with a given gap value. SPECCTRA applies such rules to individual trace segments without considering noise contributions from parallel segments.

FST To limit length and constrain spacing between parallel nets

1. Select Tools/CCT: Net Rules.
2. Choose FST.
3. Choose Parallelism Rules.
4. In the Apply Rules To frame, select the net(s) or net class to which the parallel segment rules will apply.
5. Set the noise amount per unit length on same and adjacent layers

   For same-layer parallel segments

   a. Under the Set Max Parallel Run at Gap (on same layer) button, set Gap and Distance values.

   b. Click Set Max Parallel Run at Gap (on same layer).

   For adjacent-layer parallel segments

   a. Under the Set Max Parallel Run at Gap (on adjacent layer) button, set Gap and Distance values.

   b. Click Set Max Parallel Run at Gap (on adjacent layer).
6. If the length limits are to apply between net classes, and a net class has been selected in the Apply Rules To frame:

   a. Check the Limits Apply Between Net Classes box.

   b. Select a second net class from the list box on the right-hand side of the dialog.

Repeat steps 4-6 for as many length-gap combinations as required. A separate rule is created for each length-gap combination thus creating a table.Parallel segment rules can be applied board-wide by clicking Select All in the Apply Rules To frame. Care should be taken when doing this since applying parallel rules to all nets will adversely affect autorouting performance.

Defining Noise Contributions (Cumulative)

For more precise control, noise contributions can be specified per unit length and used to compute cumulative noise from all qualifying parallel trace segments along the entire length of a net. When the accumulated noise exceeds the allowable limit, the net is rerouted to comply with the coupled noise rules.

FST To consider cumulative coupled noise between parallel trace segments

1. Select Tools/CCT: Net Rules.
2. Choose FST.
3. Choose Noise Rules.
4. In the Apply Rules To frame, select the net(s) or net class to which the noise rules will apply.
5. Set the maximum noise amount allowed on the nets in the Set Max Noise text box (volts or mvolts) and click Set Max Noise.
6. Set the noise amount per unit length on same and adjacent layers:

   For same-layer noise contributions

   a. Calculate the amount of noise occurring in a trace segment that is one default unit long (mm or mils). Be sure to calculate the value in the same units (volts or mvolts) as specified for Max Noise in step.

   b. Under the Set Noise Amount per Unit Length (at gap, on same layer) button, set Noise Amt, Gap, and Threshold values. Threshold is the minimum required same-layer parallel length before coupled noise calculations are made.

   c. Click Set Noise Amount per Unit Length (at gap, on same layer).

   For adjacent-layer noise contributions

   a. Calculate the amount of noise occurring in a trace segment that is one default unit long (mm or mils). Be sure to calculate the value in the same units (volts or mvolts) as specified for Max Noise in step.

   b. Under the Set Noise Amount per Unit Length (at gap, on adjacent layer) button, set Noise Amt, Gap, and Threshold values. Threshold is the minimum required adjacent-layer parallel length before coupled noise calculations are made.

   c. Click Set Noise Amount per Unit Length (at gap, on adjacent layer).
7. If required, define layer-specific coupling effects as defined below.
8. Repeat steps 4-7 for as many net-noise combinations as required.

Coupled noise contributions are affected by the layer on which a net is routed and by the surrounding layers. When defined, SPECCTRA will apply layer-specific multiplication (weighting) factors to the noise coupling computations for a victim net.

To consider coupling effects between layers (step in the above procedure)

1. Enter the noise weighting factor in the Weight text box within the Noise Rules dialog.
2. Select the appropriate layer name in the left-hand list box under the Weight text box.
3. Select the coupled layer name in the right-hand list box. If the Weighting factor applies to parallel segments on a single layer, select the same layer name as that in step 1. Otherwise, select the layer name for an adjacent layer.
4. Click Set Noise Weighting Factor.
5. Repeat steps 1-4 for as many layer combinations as required.

Shielding

Ground shielding is a common method used to prevent noise coupling to sensitive nets.

ADV FST

To shield a net

1. Make sure that the net to be used to shield the critical net is connected to a plane layer.
2. Select Tools/CCT: Net Rules.
3. Choose FST.
4. Choose Noise Rules.
5. Enter Shield Width and Shield Gap values.
6. Select the shielding net from the Shield with drop-down list. (Only nets routed to the plane layer will appear in this list.)
7. Click Shield with.

For details on creating plane layers, refer to the MicroSim PCBoards User's Guide.

Controlling Timing Using Length Rules

Length rules can be used to control timing by

- Controlling the maximum and minimum routed lengths on nets (expressed in absolute dimension or as a ratio of the Manhattan length to the routed length).
- Matching the routed lengths among nets in a class or between all connections within a net.
- Controlling gap and maximum amplitude of trace segments comprising a connection; e.g., when routing using trombone or accordian patterns.

A net or net class cannot be assigned both a length rule and a comparable delay rule. Whichever rule is set last overrides all previously set rules.

FST To control the maximum and minimum routed lengths of nets

1. Select Tools/CCT: Net Rules.
2. Choose FST.
3. In the Apply Rules To frame, select the net(s) or net class to have length constraints.
4. Choose the units in which the length limits are to be expressed and enter the values:

To use actual dimensions

1. Choose the Actual Length option.
2. Enter physical length values in the Max and Min text boxes.
3. Click Set Length.

To use Manhatten ratios:

1. Choose the Ratio to Manhatten option.
2. Enter decimal multipliers equivalent to the percentage of Manhatten length (the sum of the X and Y distances between a pair of pins) in the Max and Min text boxes.

   For example, Max of 1.25 and Min of 1.1 means that the selected nets should route with a maximum wire length no greater than 125% and no less than 110% of its Manhattan length.

FST To match routed lengths

1. Select Tools/CCT: Net Rules.
2. Choose FST.
3. In the Apply Rules To frame, select nets to have matched length properties:
4. To match routed lengths among constituent nets in a class, select one net class in the Net Class list box.

If more than one net is specified, matched lengths do not apply between nets. Matched lengths are attempted only for connections of a given net. So, for example, two nets may have the “match length” rule and the same Tolerance value, but may have different Max and Min length settings defining the allowable length values.

To match routed lengths of all connections comprising a net

1. Select one or more nets in the Net(s) list box.
2. Enter the allowable deviation from matched lengths in the Tolerance text box.
3. Click Set Same Length.

FST To set length and spacing constraints for trombone and accordian routing patterns

1. Select Tools/CCT: Net Rules.
2. Choose FST.
3. In the Apply Rules To frame, select the net(s) or net class to have length and gap constraints.
4. In the Set Accordian/Trombone Gap text box, enter the allowed clearance between trace segments of a given route and click Set Accordian/Trombone Gap.
5. In the Set Accordian Amplitude text box, enter the allowed amplitude of a trace routed in an accordian pattern and click Set Accordian Amplitude.

Controlling Timing Using Delay Rules

For more precise control, delay contributions can be specified per unit length per layer and used to compute total delay on a net. When the accumulated delay exceeds the allowable limits, the net is rerouted to comply with the delay rules.

Timing can also be controlled by matching delays between nets in a class.

A net or net class cannot be assigned both a length rule and a comparable delay rule. Whichever rule is set last overrides all previously set rules.

FST To consider time delay

1. Select Tools/CCT: Net Rules.
2. Choose FST.
3. Choose Delay Rules.
4. In the Apply Rules To frame, select the net(s) or net class to have delay calculations.
5. Enter Max and Min delay values in nsec.
6. Click Set Delay.
7. For each signal layer, set delay per unit length:
   a. In the Delay/Length text box, enter delay per unit length—nsec/default units (mm or mils).
   b. Select one or more layers in the Layer list box at the bottom of the Delay Control frame.
   c. Click Set Delay per Unit Length on Layer(s).
   d. Repeat steps a-c for the remaining signal layers.

FST To match time delays among nets

1. Select Tools/CCT: Net Rules.
2. Choose FST.
3. Choose Delay Rules.
4. In the Apply Rules To frame, select the net class to have matched delay values.
5. In the Tolerance text box, enter the allowable deviation from matched delays.
6. Click Set Same Delay.

Autorouting SMT Designs

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Introduction

Component placement, design rules, and routing strategy should be evaluated to achieve optimal routing results when working with SMT designs. For example, the placement of components back-to-back on opposite sides of the board, the way vias are brought out from the SMT pins (fanout patterns), and whether traces can be routed on the surface layers are all considerations that significantly affect the ultimate success of the autorouting process.

Placing SMT Components Effectively

When autorouting high density SMT designs, the effective placement of components can prove critical to achieving 100% completion. This is especially true when parts are mounted on both sides of the circuit board. There are three important factors to consider when placing SMT components:

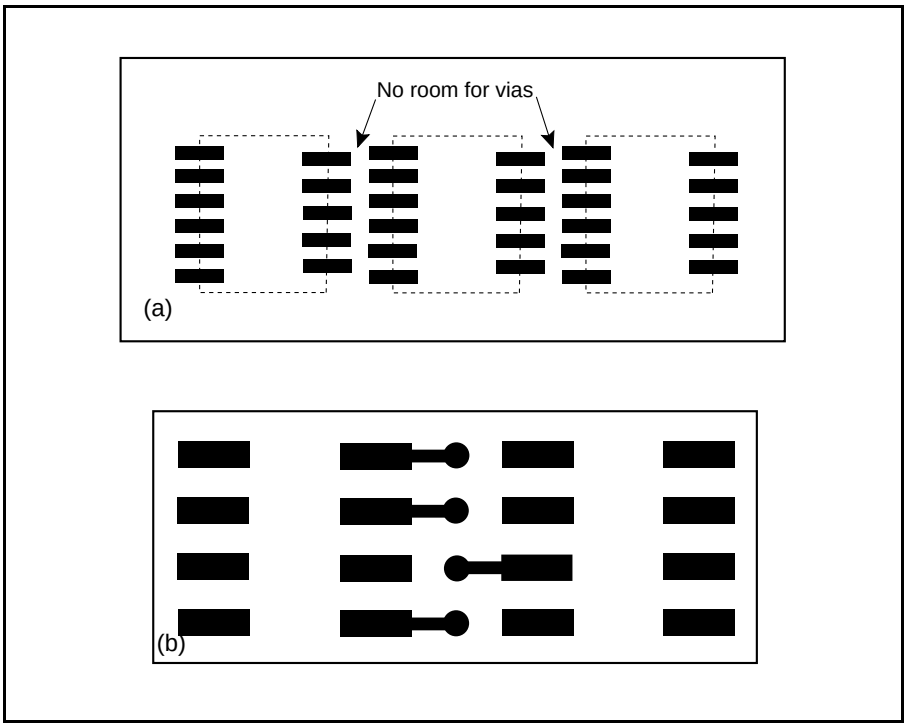
- Is enough space provided between components to allow for the placement of vias during routing? (See **Component-to-Component Placement on the Same Layer**.)
- Do the grid spacing, trace width, and via size facilitate the placement of vias and the routing of traces between component pins? (See **Grid and Routing Settings**.)
- Can traces be routed on the surface layers? (See page **Routing on Surface Layers with SMT Components**.)

Component-to-Component Placement on the Same Layer

Because of the high pin count and routing density inherent in SMT designs, most of these require multilayer circuit boards with internal routing layers. In order to connect traces using the internal layers, SPECCTRA must have enough area to place vias. If the component-to-component distance is too tight, there will not be enough room to place vias between the SMT pins, and SPECCTRA will be unable to hook up all of the traces.

Careful alignment of the components and provision for adequate space around the SMT pads will avoid this pitfall. Below is an example of poor back-to-back component placement (no room for vias and channels) and an example of preferred back-to-back placement (room for vias and open routing channels).

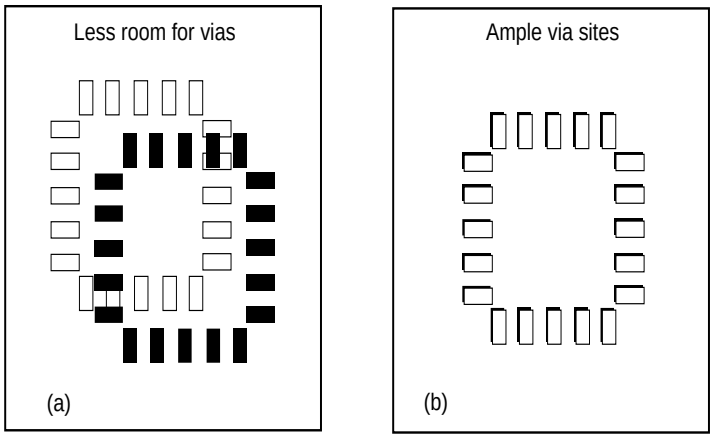
Component Placement



Component Placement on Both Surface Layers

Similar care should be given to the placement of SMT components back-to-back (or superimposed) on opposite layers. Always provide as much room as possible for vias. When components are placed back-to-back, the same surface area of the board must now provide enough space for many more via sites. Clever placement can optimize the use of this limited real estate. Below is an example of poor back-to-back placement of SMT parts (no room for vias and no open routing channels) and an example of preferred back-to-back placements (room for vias and open routing channels). As the figures illustrate, superimposing the pins preserves the greatest possible space for via placement during routing.

Back-to-Back



Grid and Routing Settings

As a general rule, the fewer constraints that are imposed on SPECCTRA, the more successful the autorouter will be in completing all of the connections. The grid spacing, trace width and clearance, and via size definitions combine to determine what routing channels can be used. Thus, these parameters have the most fundamental impact on the success of the autorouter. This can require experimentation with different combinations to gain the best understanding of what settings to use for particular types of board designs.

Grid spacing and the grid smart command

When defining grid spacings, choose a grid pattern that will allow for optimal placement of traces and vias between component pads. Although SPECCTRA is a shape-based autorouter (rather than grid-based), grid spacing may need to be defined to assure consistency with any interactive routing done within PCBoards.

If no grid setting is defined, SPECCTRA will have maximum flexibility when creating routing pathways—using the full power of SPECCTRA's shape-based routing algorithm. However, autorouted traces defined on a gridless system can prove difficult to edit later during the interactive design phases.

Here are some considerations when defining grid spacings:

- When using the default smart-route strategy, grid spacings of 1 mil tend to give SPECCTRA the greatest freedom for finding routing paths, and traces are placed on a grid matrix for easier interactive editing.
- When faced with special grided routing situations, consider using the `grid smart` command in conjunction with the `fanout`, `route`, and `clean` commands in place of `smart_route`. `grid smart` gives SPECCTRA greater freedom to adjust the via grid settings to different values at different stages of the routing effort. In most cases this is the most efficient way to establish trace and via grid spacings. Refer to **Setting Up Autorouter Runs** for details on the `grid smart` algorithm and inserting the command into the Do file.

Trace width, via size, and clearance settings

The smallest allowable via size, trace width, and clearance settings will achieve the greatest autorouting success. Consider the following when setting these values in the Tools/CCT: Setup and Tools/CCT: Net Rules dialogs:

- Choose minimum settings consistent with good manufacturing practices and tolerances.
- Avoid using needlessly large vias that may block routing channels.
- Choose a combination of trace width and clearance settings that will provide the maximum number of pathways for trace routing between component pins. This is especially true when routing between SMT pads on external layers.

Routing on Surface Layers with SMT Components

The placement of SMT components and their fine-pitch pin spacings often create areas on the surface layers that completely inhibit the routing of traces (the proverbial wall). In many cases, because of manufacturing or other design constraints, the routing of traces on the external layers is prohibited. These factors should be considered when setting up the initial routing conditions prior to starting the autorouting process:

- More internal signal layers may need to be added to compensate for the restrictions imposed on the external layers.
- A better combination of grid spacing, trace width, and clearance definitions may be necessary to allow for routing of traces between surface mount pads (see page 4-5).

By anticipating these potential areas of conflict at the outset and adjusting the routing parameters accordingly, SPECCTRA will have a greater chance of completing all of the routes on the first run.

To prevent routing on the external layers, it is necessary to edit the Do file and add restrictions by assigning *cost* factors to those layers. A cost factor is simply a means of controlling how restrictive autorouting will be on a given layer. Cost factors are normally adjusted by SPECCTRA throughout the autorouting process. By setting the cost factor to forbidden, the layer cannot be used for routing. The fanout of SMT pins, however, will still take place.

To inhibit routing on surface layers using “cost” factors

From within MicroSim PCBoards:

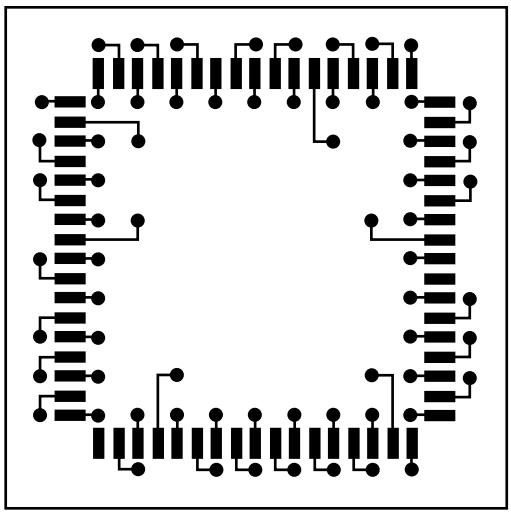
- Select Tools/CCT: Edit Do File.
- Insert the command cost layer Component forbidden before the bus diagonal command.
- Insert the command cost layer Solder forbidden.
- Click File/Save then File/Exit to save and exit the Do file.

Refer to the **CCT Design Language Online Reference Manual** for more on the `cost` command.

Fanout (Via Escape for SMT Pads)

Fanout is the method of connecting SMT pads to vias by short trace segments arranged in regular patterns. This facilitates routing on the inner layers. If fanout is done at the very beginning of the autorouting process, best use can be made of the limited via sites available. This is particularly important when parts are mounted on both sides of the board. Fanout can also be used to guarantee test-point locations for every SMT pad (refer to **Setting Up Test Points**).

Fanout Examples



There are three ways to create fanout patterns for SMT components.

- Automatically when SPECCTRA is allowed to run using the default smart-route strategy (no action on the part of the user).
- By inserting the `fanout` command in the Do file
- By interactively routing fanout patterns for specific components within the PCBoards work area.

Any one of these methods, or any combination of them may be used.

Creating Fanout Patterns Automatically

When SPECCTRA is run from PCBoards (Tools/CCT: Autoroute) without modifying the default smart-route strategy defined in the Do file, SPECCTRA automatically executes the fanout command. This should be adequate for all but the most complex designs.

For multilayer designs, this method generally yields the best results because the autorouter is offered the most flexibility—all SMT pin escapes are generated by the standard autorouting algorithm without forcing fanout at the very beginning. This is especially true for designs with two routing layers.

Using the fanout Command in the Do File

When a need exists to fanout all SMT pads (as in test point generation), then the `fanout` command should be inserted at the beginning of the Do file. The default `smart_route` command must also be replaced with a custom strategy.

To use the fanout command

From within MicroSim PCBoards:

1. Select Tools/CCT: Edit Do File.
2. Replace smart_route with fanout <# of rip-up and retry attempts>.
3. Add the commands route <# of passes> and clean <# of passes> after the fanout command.
4. Click File/Save then File/Exit to save and exit the Do file.

Avoid inserting the `fix` or `protect` commands after executing `fanout`. To work effectively, SPECCTRA must be free to reroute the fanouts during later phases of the routing effort. If the fanouts are fixed or protected, the autorouter will be greatly inhibited when trying to complete the connections.

Interactively Routing Fanout Segments

In special cases, fanout patterns can be interactively routed within PCBoards. Corresponding nets can optionally be fixed prior to autorouting by setting the NET_FIXED attribute to YES (refer to **Enabling/disabling routing on nets**).

Using Blind and Buried Vias

The Hybrid (HYB) option is required to autoroute with blind and buried vias. This option also supports assignment of a padstack style for blind/buried vias.

Blind and buried vias are different from the standard through-vias used for normal routing. A blind via has its starting layer on one surface layer, and its ending layer on an inner layer. A buried via has both its starting and ending layer set to inner layers.

For example, a blind via might begin on the component side (layer 1 of a six layer board) and connect to layer 2. A buried via, on the other hand, can begin on layer 2 and connect to layer 5. There can be many combinations of layers defined for blind and buried vias.

When the Use Blind and Buried Vias check box is enabled, PCBoards automatically creates all combinations of blind/buried vias based on the chosen through-hole padstack style and the number of signal layers in the design. Then, when autorouting, the appropriate via is applied each time a blind or buried via is generated.

HYB To allow blind and buried vias

1. Select Tools/CCT:Net Rules.
2. Choose HYB.
3. Enable the Use Blind and Buried Vias check box.
4. In the Use Padstack(s) list box, select the padstack style from which all blind/buried via padstacks should be derived.
5. If required, enter a value for the Buried Via Gap.
6. Click OK.

Using Vias under SMT Pads

The Hybrid (HYB) option is required to permit the autorouter to place vias under SMT pads, and thus, gain direct access to the inner layers without *escape* trace segments. This technique is useful when spacing between components is so tight that no via sites remain and the autorouter cannot otherwise complete connections.

Several caveats should be considered when allowing vias under SMT pads:

- The majority of SMT pads will not be large enough, or spaced far enough apart from each other, to accommodate the placement of a via without violating DRC rules. The advantages sought with this technique may prove to be minimal in actual practice when very few vias can actually be placed under SMT pads.
- If vias are placed under SMT pads, these components then become virtual through-hole parts when standard through-vias are used. This will inhibit the placement of parts back-to-back on opposite sides of the board. Conversely, if parts are placed back-to-back and through-vias are used, there may be little advantage to allowing vias under the SMT pads since most will short to other pads on the opposite side. In this case, the use of blind vias will provide the only routing advantage (see **Using Blind and Buried Vias**).
- Finally, the use of vias under SMT pads may have significant adverse effects on the fabrication and assembly processes. Plating and soldering can be severely degraded when holes exist under SMT pads. Check with the fabrication and assembly houses that will be used for manufacturing the finished circuit boards to be sure that they can accommodate through-holes under SMT pads.

Options can be enabled to control how SPECCTRA places vias. These options include either on or off the normal via grid, or inside or outside the SMT pad diameter.

HYB To allow vias under SMT pads

1. Select Tools/CCT:Net Rules.
2. Choose HYB.
3. Enable Allow Vias Under SMT Pads.
4. If needed, enable Via Must Fit Within Pad Diameter and/or Via Must Stay on Grid.
5. Click OK.

Evaluating/ Troubleshooting Autorouting Results

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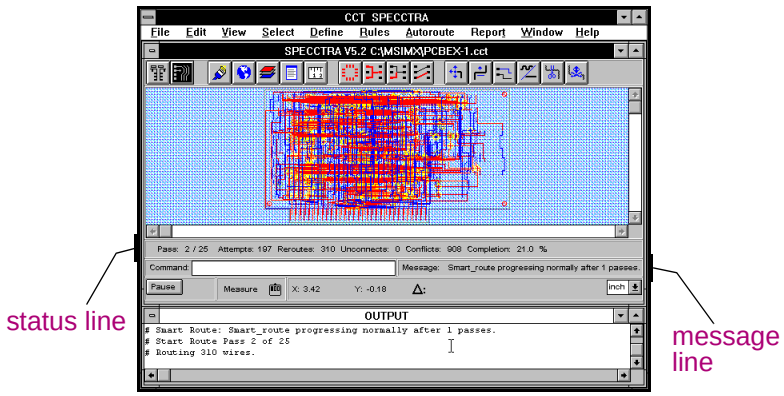
Introduction

Autorouter progress is determined by the continued reduction of routing conflicts over a given number of passes. Progress is monitored throughout the autorouting process by means of: (1) in-progress status and message lines in the SPECCTRA window and (2) records in the Status file.

Status and Message Lines

The status and message lines in the SPECCTRA subwindow provide real-time reports on autorouter progress. The status line reports the current routing pass, the number of attempts and reroutes being executed, the number of remaining conflicts and unconnects, and a completion percentage. The message line reports whether or not smart-route is progressing normally; that is, whether it is achieving the anticipated number of conflict reductions on each pass. This message is updated at the end of each pass.

SPECCTRA Window: Status and Message Lines



If SPECCTRA determines that insufficient progress is being made, a warning is issued and routing is automatically halted. In this situation, the routing constraints (number of layers, grid spacing, via size, placement, etc.) are too restrictive. To ensure 100% completion, the routing parameters should be modified in PCBoards before continuing to autoroute the design.

Status File

The second way that SPECCTRA provides information about the progress of the routing effort is using a Status file. This report can be viewed in two different ways.

To view the Status file from the SPECCTRA window

1. Click on  in the SPECCTRA toolbar or, select Report/Route Status in the SPECCTRA menu.

Viewing the Status file does not halt the autorouting process; the router continues to run in the background. The report is updated automatically after every 100 connections are routed and is saved as a text file called `<layout database name>`.STS. Also, a final Status file is always saved when the autorouting process is completed. Intermediate reports can be saved at specified intervals during routing by using the `set update_interval` command in the Do file.

To save intermediate Status files from PCBoards

1. Select Tools/CCT: Edit Do File.
2. Insert the command

```
set update_interval <# of completed connections
```

in the #Initial Commands section. The default value is 100 connections; a lower value will require more frequent saves and may slow the autorouter.

3. Click File/Save then File/Exit to save and close the file.

Interpreting the Status File

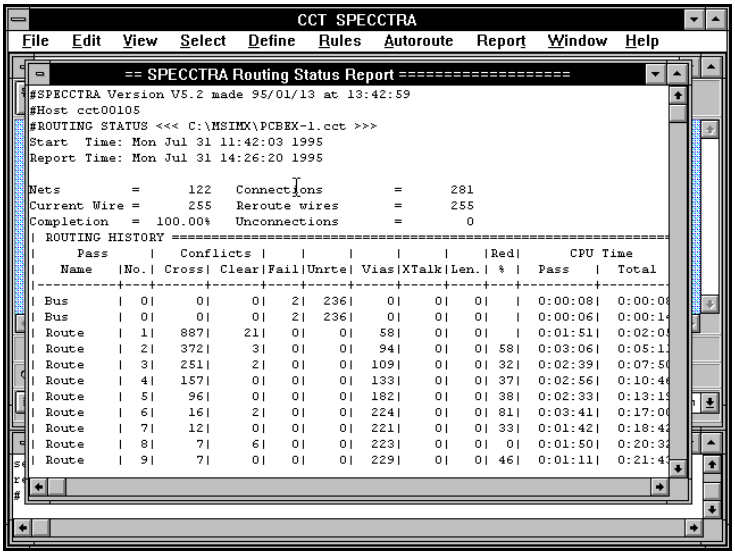
The Status file contains detailed statistics about the progress of the SPECCTRA router. The header of the file shows information about the number of nets, traces, connections, unconnections, and the completion rate. The body of the file shows statistics based on each pass of the router for the following items

.

Header	Description
Conflicts, Cross	crossover conflicts (trace-to-trace shorts on a given layer)
Conflicts, Clear	clearance conflicts (violation of DRC clearance for pad, via, or trace)
Fail	failed connections (no pathway found; unable to reroute)
Unrte	unrouted connections
Vias	vias used
XTalk	violations of crosstalk rules
Length	violations of maximum and minimum length rules
Red %	reduction percentage (percentage of conflicts eliminated since previous pass)

In addition, the amount of CPU time used for each pass and for the total job is reported.

SPECCTRA Status File



The information in the Status file is used to judge whether SPECCTRA can successfully complete all of the required connections given the specified constraints of the design. Progress

in autorouting means a steady reduction in the number of remaining conflicts and unrouted traces. For a typical board:

- The number of unroutes should be zero after the first two passes.
- The Reduction % should be greater than 30% for the first five passes.
- With each subsequent pass, the number of crossover and clearance conflicts should be decreasing.

Larger and more complex designs require more routing passes to complete the connections successfully. As long as the statistics in the Status file continue to show a steady decreasing trend, the probability of a successful 100% route is good.

General guidelines can be used to predict the probability of achieving 100% completion. These guidelines are summarized below:

Initial Phase	
Pass 1	all connections should be completed or less than 2% unroutes remaining; no more than five conflicts per connection
Pass 2	conflict reduction at least 30%
Pass 3	conflict reduction at least 30%
Pass 4	conflict reduction at least 30%
Pass 5	conflict reduction at least 30%; no remaining unroutes
Converge Phase	
Pass 6	steady decrease in number of conflicts
...	
...	
Pass <*n*>	zero conflicts

During the Initial Phase, SPECCTRA will generally achieve a steady and significant reduction in conflicts. Every connection is ripped up and new pathways are tried. The conflicts should be reduced by 30% or more for each pass. During the Converge Phase, SPECCTRA will continue to eliminate conflicts but at a slower rate as it concentrates on eliminating the remaining conflicts and fine-tuning the routing patterns.

Evaluating and Correcting Poor Progress

Because SPECCTRA attempts to complete all of the connections in the first five passes, the routing statistics at the end of the Initial Phase predict, with good accuracy, whether the layout can be routed to 100% completion. After the fifth pass, the statistics reveal whether autorouting can be accomplished under the specified design parameters. The warning signs for a design that will probably not route to completion are:

- More than 2% unroutes remain after the first pass.
- More than 5 conflicts per connection after the first pass.
- Conflict reduction is less than 30% during passes 2 through 5.
- Unroutes remain after pass 5.

Various design parameters can inhibit the router from finding adequate routing pathways. Either the layout and/or the design rules will need to be changed in order to complete the autorouting task. Typically, SPECCTRA must be stopped without saving existing routes to the Layout Database. After improving the layout and adjusting the routing parameters within PCBoards, autorouting is restarted from scratch with the updated design.

To stop autorouting

1. Click Pause.
2. Click Stop.
3. After the Stop button changes to Idle, select File/Quit.

To take appropriate corrective action and restart the autorouter

1. Modify the layout or design rules as described in the remainder of this chapter.
2. Click on Tools/CCT: Autoroute to restart the autorouter with the modified setup.

Troubleshooting Guidelines - Initial Phase

The following sections describe problems that may occur in the Initial Phase and the action that should be taken once the autorouter has been stopped.

Design rule errors

The intended routing strategy may not succeed because of conflicts in the design rule definitions. For example, trace-to-pad or trace-to-trace clearance settings may be too large to allow for multiple routing channels between pads.

Verify all trace clearance, width, and grid definitions to be sure that the design rules are not inhibiting the router.

To check/change trace design rules

1. For board-wide settings, select Tools/CCT: Setup and verify/change values in the Default Settings, Trace Grid, and Via Grid frames.
2. For per net settings, select Tools/CCT: Net Rules and verify/change values in the Net Attributes frame for each net or net class as required.
3. Check the type of via being used. The specified via padstack may be too large to allow for enough routing channels; using a smaller via may provide additional pathways for the router.

To select a different via padstack

1. For board-wide settings, select Tools/CCT: Setup; in the Default Settings frame, select a definition in the Padstack list box.

ADV

2. For per net settings, select Tools/CCT: Net Rules and choose ADV; in the Via Control frame, set the appropriate via-padstack association for each net or net class, as required.

Incorrect routing bias

Improvements in routing efficiency can be achieved by designating specific directions (bias) for the trace routing on particular layers. More routing channels are generally available on a given layer when the majority of traces are running in a particular direction, either horizontally or vertically.

To change layer bias

1. Select Configure/Layers.

2 Select desired layer.

3 Choose Edit.

4 In the Routing Bias frame, select Horz or Vert.

5 Click OK to save.

6 Click OK to exit.

Fixed traces that block pathways

SPECCTRA is not able to rip-up and reroute fixed traces. So, any fixed traces that have been interactively routed opposite to the biasing direction will restrict the router from using many potential pathways.

Prerouted traces should be fixed only when necessary, and they should follow the biasing rules as much as possible. If not, either:

- Inspect any fixed traces in the layout and reroute them if they violate the biasing rules. (See **Enabling/disabling routing on nets** for a description of the controls used to either fix or unfix a net.)
- Redefine the biasing direction for the layers in question prior to autorouting. *Refer to the* MicroSim PCBoards User's Guide..

Areafills that block pathways

If power and ground planes are defined, the autorouter will not attempt to route the nets associated with the areafills that make up the planes. By default, PCBoards interprets layers with areafills covering at least 80% of the layer as a plane. Layers with areafills comprising less than 80% of the available routing area are called mixed layers, and autorouting is permitted (though not through an areafill).

If there is a problem, inspect any mixed layers before autorouting and eliminate or modify any areafills that may act as barriers to the autorouter.

Because areafills block potential routing pathways, mixed layers can have a significant impact on the speed of the autorouting process. Judicial use of areafills will improve the speed and efficiency of the autorouter.

The percentage areafill coverage that distinguishes plane from mixed layers can be adjusted for special circumstances.

Troubleshooting Guidelines - Converge Phase

Although the autorouter may be achieving marginal success after the first five passes, other design problems can prevent SPECCTRA from reaching 100% completion during the Converge Phase. In this case, the following items should be considered when re-evaluating the layout.

Poor component placement

The placement of the components may need improvement.

- Inspect placement to determine if a better arrangement will open up additional routing corridors, reduce the overall length of the routes, or improve the general flow of the connections.
- Consider grouping parts that route to connectors or to major bus lines.

Keepouts and text that block pins

Keepouts can prevent routing to certain pins or components if they do not allow adequate access for trace runs. For example, a keepout that is inadvertently defined under a component pin will prevent routing to that pin on that layer. The same situation can result from text placed on signal layers. In general, text items in etch should be placed near a board edge to avoid restricting routing paths or access to component pins.

Inadequate number of routing layers

In the case of very dense layouts, the specified number of routing layers may be inadequate to complete all of the required connections. Additional routing layers may need to be defined. This is especially true for surface mount designs where routing on the surface layers is severely hampered by the presence of high-pitch footprints that do not allow routing between pads. Use Configure/Layers/New from within PCBoards to create new signal layers. For more information, refer to the MicroSim PCBoards User's Guide..

Corrective Action When there is Not 100% Completion

Any or all of the guidelines described in this section may need to be considered to assure 100% routing completion. These should be checked prior to the initial routing attempt in order to avoid obvious problems at the outset and thus increase the probability of finishing the routing on the first try.

When to Interrupt the Autorouting Process

Autorouting should be allowed to continue unless the total number of conflicts reaches a plateau and remains fairly constant for ten consecutive passes. If this condition is reached, SPECCTRA will probably not make any further significant progress. If all of the design parameters have been checked and optimized, and SPECCTRA still shows poor results, additional resources may be called upon to achieve completion.

Corrective Action

The following sections describe ways to achieve 100% completion.

Completing routes interactively

In many cases SPECCTRA may complete all but a handful of the connections. It may be more efficient to complete the remaining unconnects interactively rather than attempting to reroute the entire board. Depending on the complexity of the design, the number and length of the remaining unrouted connections, and the time constraints involved, this is often a preferred solution for completing unrouted nets.

Depending on the purchased options, there are two ways to interactively edit the routes:

- Using the PCBoards Layout Editor.
- Using Cooper & Chyan Technology's EditRoute option.

For information on using EditRoute, see **Routing Interactively in SPECCTRA (EditRoute Option)**. The remainder of this section describes using the PCBoards Layout Editor for trace editing.

When SPECCTRA runs to completion, the routes are automatically saved in the Routes file, `<layout database name>`.RTE. If the SPECCTRA run is interrupted, the routes must be deliberately written to the Routes file. This file can then be imported into the design with the PCBoards window; the remaining connections can be interactively routed.

Completing routes using the PCBoards Layout Editor

1. Save the routes and exit.
2. If routing is in progress:
   a. Choose Pause.
   b. Choose Stop. The Idle button will appear (greyed-out).
   c. Select File / Write / Routes.
   d. Within the Write Routes dialog:
   e. Set the file name to `<layout database name>.rte`.
   f. If there are any test points, check the Include Testpoints box.
   g. Click OK.
3. Select File/Quit.
4. Click YES when presented with the confirmation request.
5. Import the routes and proceed with interactive routing.
   a. Select Tools / CCT: Read Routes.
   b. Interactively route remaining connections using the direct manipulation techniques described in Chapter 6 in the MicroSim PCBoards User's Guide.

Completing routes using the autorouter with the ROUTE command (Do File)

If, after exiting SPECCTRA, the current routes are imported into the Layout Database, SPECCTRA can be restarted from the last completed pass without losing the trace routing progress made so far. Thus, design parameters, netlist, and component placement can be modified and used to constrain the next autorouting attempt on the remaining connections.

To change the design/constraints and restart the autorouter from the last stopping point.

1. Save the routes and exit.
2. If routing is in progress:
   a. Choose Pause.
   b. Choose Stop. The Idle button will appear (greyed-out).
   c. Select File / Write / Routes.
   d. Within the Write Routes dialog:
      - Set the file name to `<layout database name>`.rte.
      - If there are any test points, check the Include Testpoints box.
   e. Click OK.
3. Select File/Quit.
4. Click YES when presented with the confirmation request.

From within PCBoards

5 Select Tools/CCT: Read Routes.

6 Change autorouting rules and layout as required within the work area, Tools/CCT: Setup dialog, and/or Tools/CCT: Net Rules dialog.

7 Select File/Save.

8 Select Tools/CCT: Edit Do file.

9 Change the smart_route or route command to
route <passes> <starting pass>
where <passes> defines the total number of passes to run, and <starting pass #> defines the next pass in the sequence as follows:

Completed Passes	Setting
to<*last pass*> + 1	less than 15 passes set <*starting pass*>
15 passes or more	set <*starting pass*> to 16

10 Select File/Save then File/Quit to save and exit the Do file.

11 Select Tools/CCT: Autoroute to restart the autorouter.

Opening routing channels using clean passes (Do File)

Each routing pass can leave unnecessary jogs and loops in the traces that can prevent the use of adjacent routing pathways. *Clean* passes straighten out trace runs and eliminate extra vias and loops. Previously unavailable routing channels are opened by the clean passes.

To add clean and route passes

1 Select Tools/CCT: Edit Do File.

The smart_route command automatically performs four clean passes.

2 Insert the command `clean <number of passes>` after a `route` or `smart_route` command in the `#Routing commands` section.

3 Insert additional `route` and `clean` commands as needed.

4 Select File/Save then File/Exit to save and close the file.

Analyzing Long Routing Time

Although SPECCTRA may be successfully completing connections and removing conflicts, the speed of the autorouting process may seem inordinately slow. There are several conditions that can slow down the router and prevent efficient use of the router's resources. These are described in the next few sections.

Components or pins placed outside the keepin boundary

If a component or certain pins of a component are mistakenly placed outside the signal-keepin boundary, the router will still attempt to make connections to these. This will show up in the Status file as large numbers of unroutes and failures. SPECCTRA will waste routing time by trying to find pathways to these pins that cannot be connected.

To solve this problem, return to PCBoards and either:

- Relocate the components that may be outside the keepin.
- Redefine the boundaries of the keepin to include those components.
- If the design requires connections outside the keepin area, interactively complete those connections and *fix* them prior to autorouting; SPECCTRA ignores fixed traces.

Once these corrections are made, restart the autorouting process using the updated layout (see **Completing routes using the autorouter with the ROUTE command (Do File)**).

Disk paging and low memory problems

The recommended memory configuration for operating SPECCTRA is a minimum of 16 MB of extended RAM; for larger and more complex designs, 64 MB of RAM may be required. If your system is running on less main memory, disk paging may be taking place to accommodate the memory needs of the router. Disk paging will significantly slow the performance of the router. To check if disk paging is taking place, compare the elapsed time to the CPU time, as shown in the SPECCTRA Output subwindow. If the elapsed time is significantly greater than the CPU time, the router is sharing CPU time with another application or is paging to disk. The solution is to increase system memory.

ECO Incorporation and SPECCTRA

When changes are made to the schematic, the Forward ECO process is used to update the layout in PCBoards. (Refer to the MicroSim PCBoards User's Guide.). Once the layout has been updated, autorouting can be continued by following the instructions outlined in **Completing routes using the autorouter with the ROUTE command (Do File)** for restarting the autorouter. This should handle ECO situations efficiently because the annotation functions in PCBoards log all of the updates to the Design file.

If the ECOs involve a major reconfiguration of the layout (for instance, several new components have been added, the placement has been rearranged, major additions or deletions have been made to the netlist, etc.) then it may be more efficient to restart the autorouting process from the beginning. Often, better results will be obtained if the updated layout is treated as a whole new routing job in SPECCTRA.

Special attention should be given to the following guidelines when using the autorouter after incorporating ECOs:

- All design parameters (grid size, trace width and clearance, biasing, etc.) in the updated database should be set the same as in the previous routing session.
- All critical nets and test vias should be protected.
- If the `miter` command was executed in the previous session prior to saving, the `unmiter` command should be used before proceeding with the new routing session (see **To unmiter corners**).

Routing Interactively in SPECCTRA (EditRoute Option)

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Introduction

EditRoute is the Cooper & Chyan Technology shape-based tool for interactively routing printed circuit board connections using automatic plow and shove techniques to work around existing traces and vias on the board. When routing new traces, EditRoute automatically pushes existing traces aside and routes around pins (plow). When moving trace segments or vias, existing traces blocking the path are pushed ahead, even over other pins and vias (shove).

While a trace segment or via move is in progress, the effect of plow and shove are dynamically displayed allowing for immediate evaluation and adjustment of the edit. At any time, the multi-level undo feature can be used to revert to previous routing configurations.

EditRoute can be used in either a grided or gridless environment. EditRoute also supports on-line checking of trace width, clearance, and order (daisy-chain) rules set in the Tools/CCT: Setup and Tools/CCT: Net Rules dialogs, or within the SPECCTRA Interactive Routing Setup dialog.

Editroute does not support fast circuit rules for: shielding, differential pairs, regions, length, round corners, parallel and tandem segments, parallel and tandem coupled noise.

Starting SPECCTRA for Interactive Routing

EditRoute is run from within the SPECCTRA window. It is used either stand-alone or in combination with the SPECCTRA autorouter. For instance, if autorouting progress is very slow, the session can be stopped and the troublesome conflicts can be resolved interactively using EditRoute; when done, SPECCTRA can be restarted to automatically route the remaining conflicts and/or unconnects.

To first autoroute and then halt the session for interactive trace editing

1. Select Tools/CCT: Autoroute.
2. When appropriate, click Pause at the bottom of the SPECCTRA subwindow.
3. When the Pause button is replaced with Stop, click Stop.

To start SPECCTRA for interactive use only

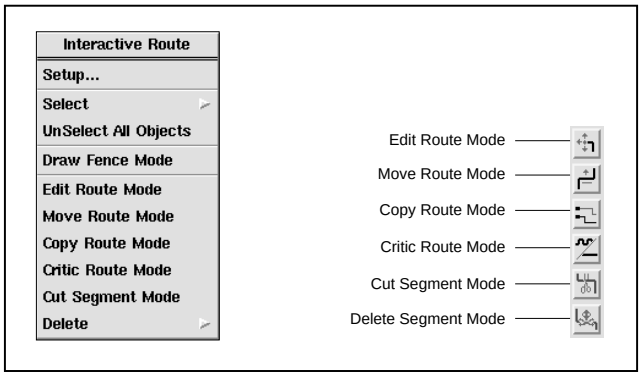
1. Select Tools/CCT: Edit Do File.
2. Remove or comment out the smart_route or route commands, and any clean commands.
3. Click OK.
4. Select Tools/CCT: Autoroute.

Using EditRoute

First, design rules and editing preferences need to be defined. Then, editing modes are selected so that specific actions can be taken to change existing routes or create new routes shown in the graphic display.

Setup functions and mode selections are chosen from the Interactive Route menu or from corresponding toolbar buttons as shown in the figure below.

Interactive Route Menu and Corresponding Toolbar Icons



To display the Interactive Route menu and select a command, do the following from within the SPECCTRA window:

1. Position the cursor within the graphical display showing the design.
2. Press and hold the right mouse button.
3. Slide the cursor to the desired command.
4. Release the right mouse button to select the command.

An outline of the suggested steps for using EditRoute follows.

To use EditRoute

1. Set up board-wide layout rules in the Tools/CCT: Setup dialog.
2. Set up net-specific layout rules in the Tools/CCT: Net Rules dialog. (Rules defined using the ADV, DFM, HYB, or FST subdialogs are not considered when running EditRoute.)
3. Set up additional editing preferences or overrides to the settings made in steps 1 and 2 (see the section **Setting the Routing Environment within SPECCTRA**):
   a. Press and hold the right mouse button to display the Interactive Route menu and select Setup.
   b. Fill in the Interactive Routing Setup dialog as required (see **Setting the Routing Environment within SPECCTRA**).
   c. Click OK or Apply.

Set the primary and secondary routing layers using the toolbar button to bring up the Layer panel (see **Setting Primary and Secondary Routing Layers**).

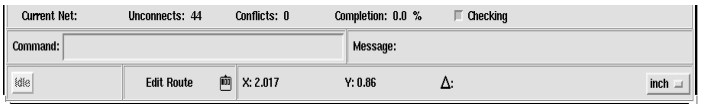
4. Select the routing mode.
5. Press and hold the right mouse button to display the Interactive Route menu and select one of the modes (listed in the table below).
6. Edit and route traces, as needed, in the graphical display (SPECCTRA subwindow) using the left mouse button (see **Routing Traces** through **Deleting Traces**).

EditRoute can be used in any of six editing modes as summarized in the table below.

Mode	Description
Edit Route	Creates new trace paths and adds vias. Traces that are not protected or fixed are shoved aside to add the new path if Push is checked in the Interactive Routing Setup dialog box.
Move Route	Moves a single trace or via. All movable traces in the path of a trace or via that is being moved, are shoved aside if Push is checked in the Interactive Routing Setup dialog box.
Copy Route	Copies an existing trace to an unroute with a similar length and path.
Critic Route	Removes extra bend points in one or more traces within a drawn rectangular box.
Cut Segment	Breaks a single trace segment into two segments.
Delete	Segment Mode: removes a single trace segment. Trace Mode: removes a complete trace (all segments and attached vias. Net Mode: removes all traces and vias on a net. Repair Net Mode: removes all traces and vias that violate fromto order rules on a net.

The current mode is displayed below the command line as shown below

Mode Status Area



The remaining sections present details on how to use EditRoute to set up the session and to route/edit traces using the various EditRoute modes.

Setting the Routing Environment within SPECCTRA

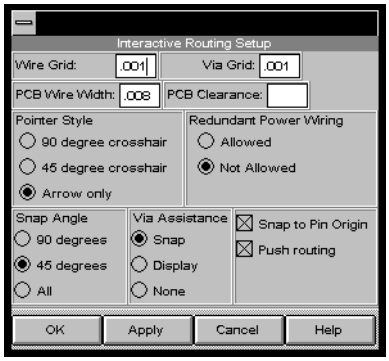
In addition to the controls PCBoards provides for defining layout rules (using the Tools/CCT: Setup and Tools/CCT: Net Rules dialogs), SPECCTRA provides controls to define design constraints and editing preferences used by EditRoute. These include:

- Trace (wire) and via grids
- Board-wide trace (wire) width and clearance rules
- Pointer style
- Redundant traces
- Routing snap angle
- Via assistance
- Snap to pin origins
- Push routing

The terms *trace* used within PCBoards dialogs and this manual, and *wire* used within EditRoute dialogs, are equivalent.

To set up the environment for interactive routing

1. Within the SPECCTRA window, position the cursor in the graphic display of the design.
2. Press and hold the right mouse button. The Interactive Route menu is displayed.
3. Select Setup from the Interactive Route menu. The Interactive Routing Setup dialog is displayed.



4. Define or change one or more of the settings described in the succeeding subsections.
5. Click OK or Apply.

Setting Trace and Via Grids

Although trace and via grids can be set separately, grids are not required. A gridless mode can be employed by setting trace and via grids to zero. Initially, the Wire Grid and Via Grid edit controls are set to the values specified in the Tools/CCT: Setup dialog (Trace Grid frame: Spacing text box; Via Grid frame: Spacing text box).

To set trace and via grids

1. Enter a trace spacing value in the Wire Grid text box.
2. Enter a via spacing value in the Via Grid text box.

Setting Board-Wide Trace Width and Clearance Rules

Trace width and all clearance rules can be set at the board-wide level. Rules at the board-wide (PCB) level have the lowest precedence in the SPECCTRA rule hierarchy and can be overridden by net rules specified in the Tools/CCT: Net Rules dialog. Initially, the PCB Wire Width and PCB Clearance edit controls are set to the values specified in the Tools/CCT: Setup dialog (Default Settings frame: Width and Clearance text boxes, respectively).

To set PCB trace width and clearance rules

1. Enter a board-wide trace width value into the PCB Wire Width text box.
2. Enter a board-wide trace clearance value into the PCB Clearance text box.

Setting the Pointer Style

When using Edit Route mode, a full-size crosshair can be added to the cursor. Crosshair segments can be viewed at either 90-degree or 45-degree intervals starting from horizontal. The 45-degree crosshair is only displayed if Snap Angle is also set to either 45 degrees or All.

To set the pointer style

Choose one of the following:

- Arrow only, which displays an arrow cursor without crosshairs.
- 90 degree crosshair, which displays orthogonal crosshairs.
- 45 degree crosshair, which displays both 90 and 45-degree crosshairs. Check that Snap Angle is set to 45 degrees or All.

Controlling Redundant Routes

By default, EditRoute eliminates trace loops and extra vias during interactive routing.

To control redundant routes on power connections

Choose one of the following:

- Allowed, which permits redundant traces and vias on power nets (useful, for instance, when increased current capacity to a power connection is needed).
- Not Allowed, which prevents redundant routes on power nets.

Redundant traces and vias on power connections are not automatically protected. Use one of the protect commands on the SPECCTRA Edit menu to prevent the autorouter from eliminating redundant traces and vias on power connections.

Setting the Routing Snap Angle

When routing, Snap Angle defines whether the cursor snaps to any angle or to a 45- or 90-degree angle.

To set the routing snap angle

Choose one of the following:

- 90 degrees, which allows orthogonal routing only.
- 45 degrees, which allows 90- and 45-degree routing angles.
- All, which allows all routing angles.

Controlling Via Assistance

The Via Assistance controls determine whether:

- New vias are automatically snapped to a legal site.
- Visual cues showing legal via locations are displayed.

For example, when routing a connection, a via is added by clicking twice in the same location. If the Snap option is enabled, the cursor snaps to the closest via site. If Display is enabled, nearby legal via sites are displayed when the current location is not a legal via site.

To enable via-snap assistance

Check the Snap box in the Via Assistance frame.

To enable via-display assistance

Check the Display box in the Via Assistance frame.

To disable visual via assistance

Check the None box in the Via Assistance frame.

For more information, see **Using a Via Grid**.

Controlling Snap-to-Pin Origin

The Snap to Pin Origin check box controls whether the cursor snaps to the origin of a noncircular pin. If Snap to Pin Origin is enabled (default), and the cursor is anywhere inside of a noncircular pin when the mouse button is clicked, the current trace snaps to the pin origin. If Snap to Pin Origin is disabled, a connection to a noncircular pin is considered complete if it is simply within the boundary of the pin shape. Traces always snap to the origins of circular pins, regardless of how this control is set.

To snap to pin origins

1 Check the Snap to Pin Origin box.

Controlling Push Routing

EditRoute can push aside traces as new routes are established and still comply with relevant trace-to-trace clearance rules. This feature reduces the need to interrupt routing when existing traces block a path.

To set EditRoute to automatically push aside traces and vias

1 Check the Push routing box.

Setting Primary and Secondary Routing Layers

Before routing, the primary and secondary routing layers must be set. The primary layer is the active signal layer for interactive routing. The secondary layer is the layer to which EditRoute switches when a via is added; after the switch, the secondary layer becomes the primary layer and the layer that was primary becomes secondary. Primary and secondary layers must be supported by at least one via padstack that contains shapes on both primary and secondary layers.

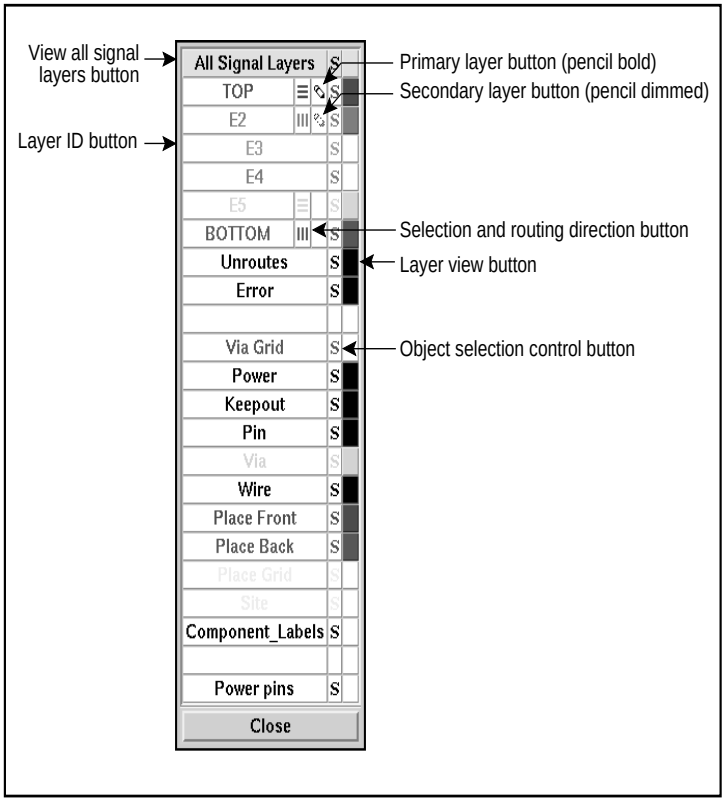
The layer configuration is displayed by clicking the  toolbar button. The primary routing layer is indicated in the layer panel by a bold pencil icon. The secondary layer is marked by a dimmed pencil icon.

When routing from an SMD pad or existing trace, the layer on which the pad or trace is located automatically becomes the primary (active) layer.

To choose primary and secondary routing layers

1. Click  on the toolbar to display the layer panel.
2. Select the visible layers by clicking the layer view button (square icon) to the far right of the layer name. When set to visible, the button color appears in the color used for layer display.
3. Click the pencil button for the secondary layer; the pencil icon must be dim.
4. Click the pencil button for the primary layer; the pencil icon must be bold.

Example Layer Panel



Routing Traces

EditRoute mode is used to route new traces, and to add, change, or replace existing traces. When in this mode, an envelope surrounds the current trace segment to indicate that the trace-to-trace clearance rule is in effect. Arrows and alignment marks are also added when the cursor aligns with a nearby trace, pin, or via that is on the current net.

To route a trace

1 Click  in the toolbar.

Press and hold the right mouse button to display the Interactive Route menu and select Edit Route Mode.

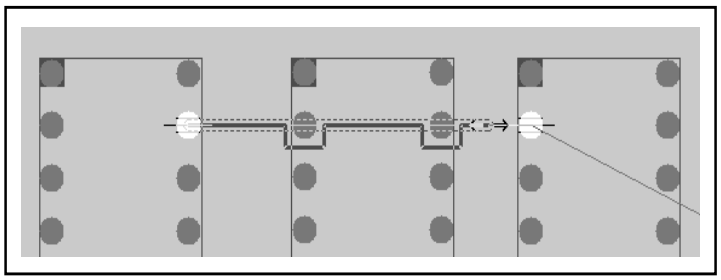
2 Click on a pin, via, rat, or trace segment to start.

3 When starting from a through-pin or via, the layer marked as primary in the layer panel is used. When starting from an SMD pad or a trace, the primary layer is automatically set by SPECCTRA.

4 Move the cursor to the next vertex and click to add the trace segment.

While routing a connection, a preview trace stretches as the cursor is moved from the last vertex. The preview trace jogs around shapes that are not part of the same net, showing the intended path before completing the segment. Below is an example of a preview trace that jogs around several wiring obstacles as the cursor is moved from the starting pin on the left to the target pin on the right.

The Preview Trace



Changing a Routing Path

Before completing a connection, a portion of the segment can be deleted.

To delete a portion of the current trace segment

Move back over the section of trace to be removed and click. The segment is trimmed to the current cursor position.

To undo prior completed edits

Press the <Undo> or <F3> key to undo the last interactive design change. Multiple undo operations will remove the effect of each edit in reverse completion-order.

To restore (redo) a previous undo operation

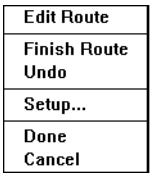
Press <Shift Undo> or <Shift F3>.

Automatically Finishing a Connection

When a route is in progress, SPECCTRA can be used to finish a connection automatically from the ending vertex of the last completed segment. SPECCTRA searches for a path that is within the Finish Route search area. If a direct path is not available, the connection cannot be completed and SPECCTRA abandons the operation.

To automatically finish routing the current connection

1 Press and hold the right mouse button to display the Edit Route menu.



2 Slide the cursor to Finish Route and release the right mouse button.

After completing a connection between two pins, the trace disconnects from the cursor. EditRoute remains in Edit Route mode, awaiting the next interactive routing operation.

Interrupting Routing

An incomplete route, such as that shown in the the figure below, can be retained or removed.

To interrupt routing and retain the incomplete connection

1 Press and hold the right mouse button to display the Interactive Route menu.

2 Select Done.

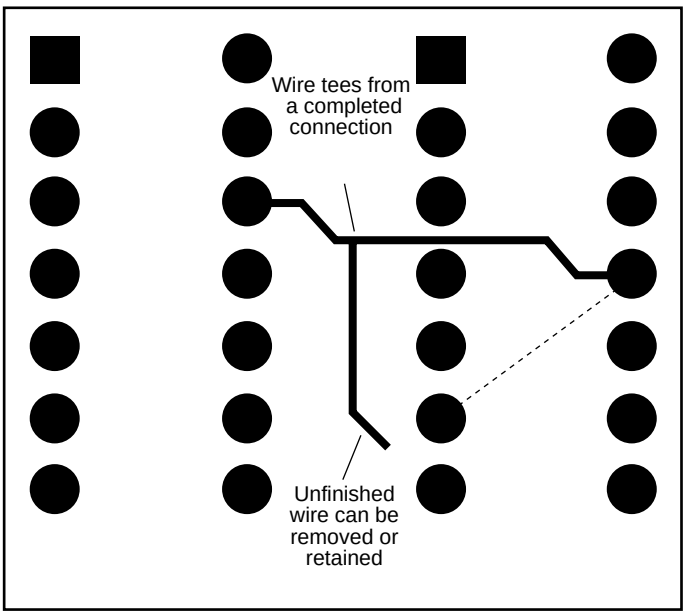
Click on any icon in the toolbar.

To interrupt routing and remove the incomplete portion

1 Press and hold the right mouse button to display the Interactive Route menu.

2 Select Cancel.

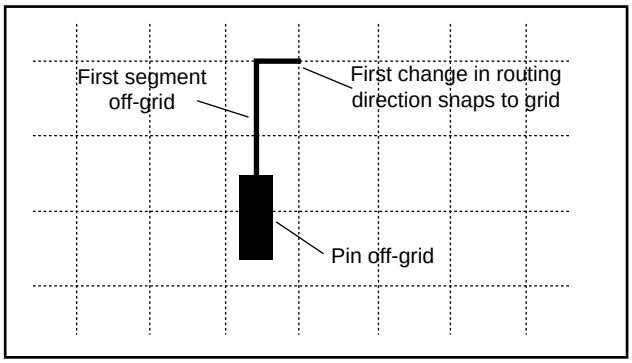
Trace Segments that Can be Removed or Retained



Using a Trace Grid

EditRoute always uses the trace grid defined for the primary layer (the layer currently used for routing). When using a trace grid, the center of the trace is positioned on the grid, unless the route starts on an off-grid pin, or ends on an off-grid pin or trace. When entering or exiting a pin that is off-grid, the entire first segment into or out of that pin is off-grid. The next vertex established in a different X or Y direction is on-grid. The figure below shows how EditRoute typically routes from a pin that is off-grid.

First Trace Segment from an Off-Grid Pin

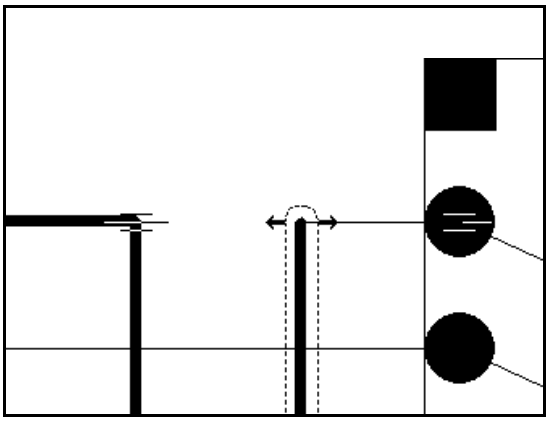


To view the trace grid

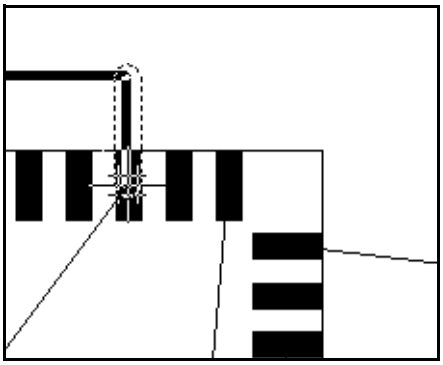
1. Click  in the toolbar.
2. Click the Wire Grid layer button.

Aligning Traces with Target Traces, Pins, and Vias

When routing, if the cursor aligns with a trace, pin, or via on the same net, an arrow is displayed at the end of the current trace. Alignment marks also appear over target traces, pins, or vias when they are aligned with the currently routed trace, as shown below.



When the end of the current trace is over either the vertex of a target trace or origin of a target pin or via, both horizontal and vertical alignment marks appear, as shown below.



Selecting a Via for Routing

When more than one via is available in a design, the via used to route a connection depends on which vias are currently selected, which layers are defined as primary and secondary, and whether via type rules apply. The Select/Vias/By List dialog (shown next page) allows one or more vias to be selected from those that are available in the design.

If no via is specified for use, or if more than one via is selected, SPECCTRA chooses a via that has shapes defined on the fewest layers and the smallest X, Y dimensions for those shapes.

A via cannot be used to connect to a layer if the via has no shape defined on that layer.

Selecting one via for interactive routing

To unselect all vias

1. Select Select/Vias/By List to display the [Un]Select Vias dialog box.
2. Choose the UnSelect option in the Action panel.
3. In the Vias list, select all vias.
4. Click Apply.

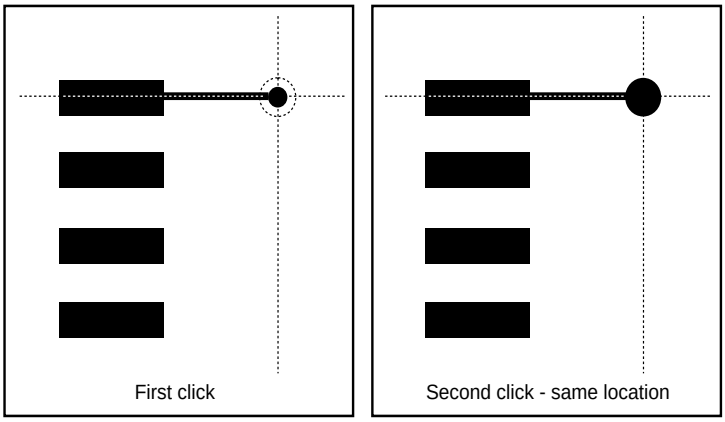
To select the one via to be used

1. Click the Select button in the Action panel.
2. In the Vias list, select the via to be used.
3. Click OK.

Adding a Via while Routing a Connection

When routing, a small filled circle appears when the cursor is over the last established vertex. A second click at that location adds a via if the location is a legal via site. The figure below illustrates the process of adding a via.

Appearance of Display When Adding a Via



To add a via while routing a connection

1. Click  in the toolbar.
2. Click on a pin, trace, or via to begin routing.
3. Click at the location where a via should be added.
4. Position the cursor precisely over the last established vertex; a small filled circle appears.
5. Click a second time at the same location to add a via.

If the location is not a legal via site, a via is not added. Instead, the Message area displays: `Via is illegal there (violation). Select a via site.`

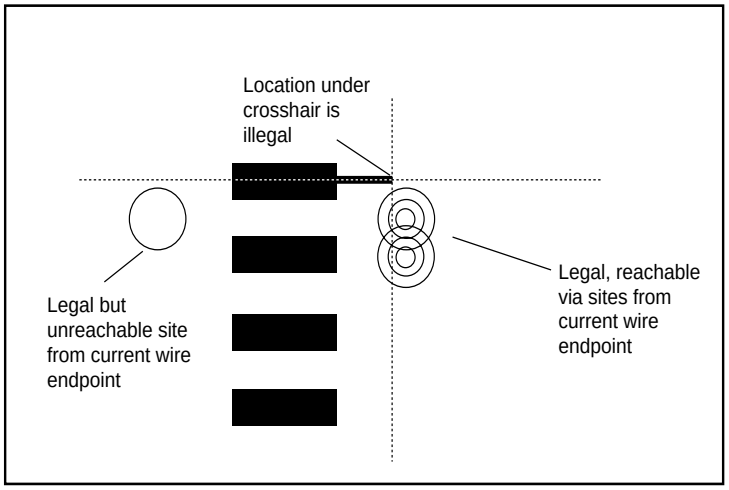
Using a Via Grid

If a via grid is defined, vias are always placed on the grid. There are three scenarios to consider depending on where the cursor is positioned when attempting to add the via, and the current editing preferences. These are:

- Adding a via on grid (double-clicking over a grid location) that is a legal via site: EditRoute immediately adds a via.
- Adding a via off grid that is within one via radius of a legal via site and Snap is enabled (Interactive Routing Setup dialog box): The cursor snaps to the grid and a via is added.
- Adding a via off grid at an illegal via site and Snap is disabled: EditRoute issues the warning, `Via is illegal there (off-grid). Select a via site.`

If Display is enabled (Interactive Routing Setup dialog), and an attempt is made to add a via at an illegal site, alternative legal via sites become visible in the graphic display. Such a display is shown below.

Example: Alternative Via Sites After Adding a Via



Two types of alternative via sites can display: reachable vias and unreachable vias.

- Reachable vias display as a bull's eye (concentric circles) that can be reached from the end of the current trace segment.
- Unreachable vias sites display as single circles that can not be reached from the end of the current trace segment; more trace segments are required to reach the via.

If Display is disabled, all via sites that are on grid are displayed as reachable in the error color; this indicates that checking is off.

To add a via at a reachable via site

1. Move the crosshair to one of the reachable via sites. The concentric circles under the crosshair change to a single filled circle.
2. Click to add the via.

To add a via at an unreachable site

1. Add more trace segments to reach the via site.
2. Click to add the via.

Moving a Trace Segment or Via

Move Route mode is used to move existing trace segments and vias. When moving a segment, other connecting segments are stretched and adjusted as needed. Trace corners can be moved diagonally to modify or eliminate a bevel.

Traces blocking the segment or via being moved, can be pushed aside if Push routing is enabled. Clearance and trace width rules are maintained for all traces involved in a Move Route operation.

To move a trace segment

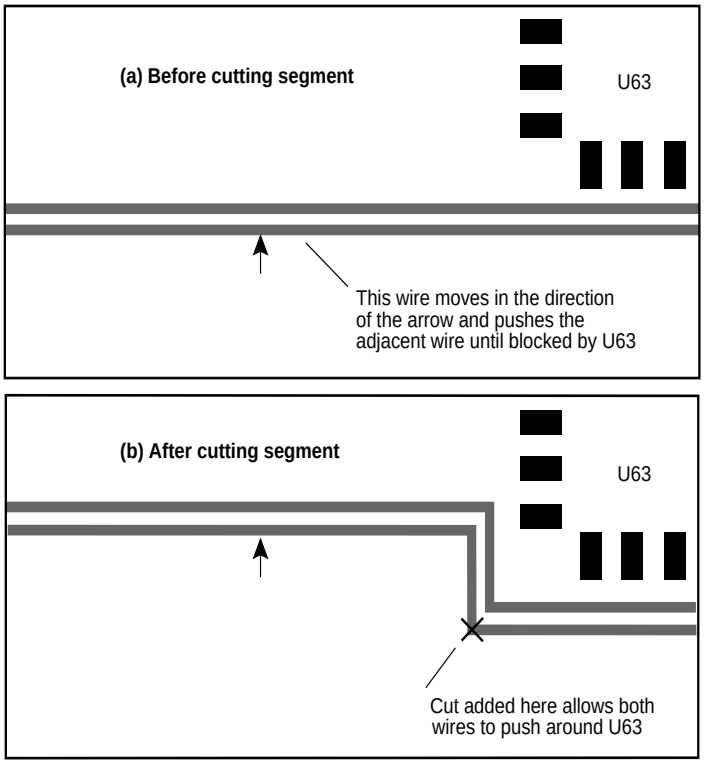
1. Click  in the toolbar.
2. Click on the trace segment or via to be moved.

   The trace or via attaches to the cursor. When moving the cursor, all connected traces stretch to follow. If Push is enabled, other traces in the path are pushed aside to maintain required clearances.
3. Click to place the trace at the location under the cursor.
4. Repeat steps 2-3 for as many move operations as are needed.

Moving a Trace Segment Around an Obstacle

The Cut Segment mode is used to create a new segment in a trace, so that as it is moved, it can route around an obstacle. Any adjacent traces that are pushed aside in the process, also create a new segment. Below is shown how a cut in the trace segment being moved pushes an adjacent trace around an obstacle.

Cutting a Segment in One Location (and Any Blocking Traces) Pushes Around an Obstacle When Moved.



To cut a segment into two pieces

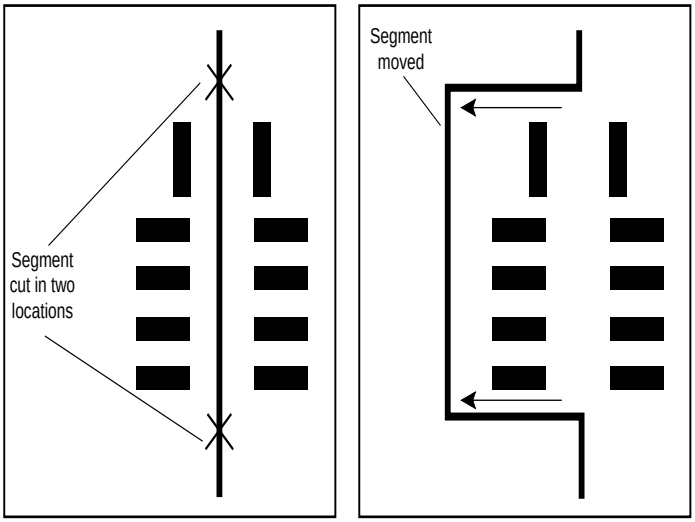
1. Click  in the toolbar.
2. Click on the trace (to be moved) at the position of the cut location. Two trace segments are created.

Use the Move Route mode to move the separate trace segments.

Creating Three Trace Segments from One

If it is impossible to move a long segment because it is blocked, a segment can be cut in two locations to move a portion of the trace around the obstacle, as shown below.

Effect of Cutting a Segment in Two Locations: Routing Around an Obstacle



To create three trace segments from one

1. Click  in the toolbar.
2. Click at two cut locations on a trace segment.

When cutting a trace segment, the cut locations are maintained only until the next operation. Move or delete the segment immediately after marking the cuts. Cut points are not maintained once a trace is manipulated by an operation such as Critic Route.

Copying Traces and Vias

The Copy Route mode copies existing traces and vias to unrouted connections. The traces and vias that can be copied include fanout patterns created in SPECCTRA. The path of the target unroute must be approximately the same topology and length as the path being copied.

When using a pin to define the path, and the pin has more than one connecting path, EditRoute can not determine which path to copy or replace and the operation is abandoned.

To copy a trace to an unrouted connection

1. Click  in the toolbar.
2. Click on a trace or pin on the path to be copied. Both pins of the connection highlight.
3. Click on the rat or target pin where the copied route should be placed.

During the Copy Route operation, segment lengths are adjusted to match the pin locations of the target unroute. Before EditRoute completes the new path, design rule violations are checked. If the new path violates a rule, the copy operation is abandoned and the message area displays: `Path cannot be copied.`

When using a trace grid, Copy Route follows the grid for both orthogonal and diagonal paths. This can create larger gaps between adjacent diagonal paths. To maintain smaller gaps, define a smaller trace grid.

Removing Bends in a Trace

The Critic Route mode removes extra bends and acute angles from traces. It can also improve pad and via entries and exits. Critic Route can apply to a single trace or pin, or to all unprotected traces that pass through a drawn region.

To remove extra bends from traces and improve pad and via entries and exits

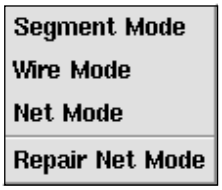
1. Click  in the toolbar.
2. Click on a trace or pin to select a single connection.

Alternate Methods:

- Press and hold the right mouse button to display the Interactive Route menu and select Critic Route Mode.
- Drag the cursor to create a rubberbanding rectangle; release the mouse when the rectangle encloses one or more trace segments.

Deleting Traces

EditRoute provides four delete modes (shown below), which can be used to delete entire traces or portions of traces that are unprotected.



To delete a trace segment

1. Click  in the toolbar.
2. Click on a segment to remove the segment and replaced it by a rat.

A complete trace that comprises all the segments between two terminal points can also be deleted. A terminal is a pin, a via, or a tjunction.

To delete a complete trace

1. Press and hold the right mouse button to display the Interactive Route menu and select Delete/Wire Mode.
2. Click on a trace.

The clicked segment and all other segments of the trace are deleted and replaced by a rat. Vias connecting to the trace are also deleted.

All traces on a net can be removed with a single action. Only the traces are deleted; EditRoute cannot delete a net from a design.

To delete all traces on a net

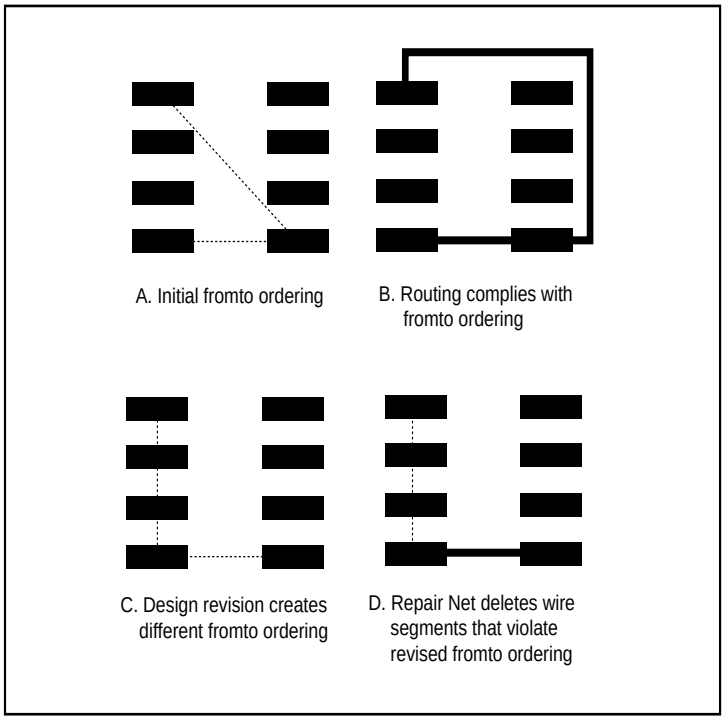
1. Press and hold the right mouse button to display the Interactive Route menu and select Delete/Net Mode.
2. Click on a segment, pin, or a via.

Repairing a Net

The Repair Net mode deletes trace segments that violate fromto order rules. Trace segments that comply with fromto order rules are not affected.

Fromto order violations can result from a design revision. For example, if an engineering change to a finished design alters fromto ordering, the design file must be re-extracted, loaded into SPECCTRA, and the routes or session file from the previous session must be read in. Repair Net Mode is then used to delete the incorrect routing on the affected nets. Below is shown how Repair Net removes incorrect routing.

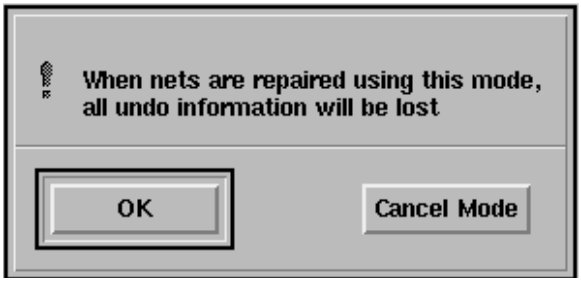
Repair Net Mode Removes Traces that Violate Fromto Order Rules



To repair a net

1 Press and hold the right mouse button to display the Interactive Route menu and select Delete/Repair Net Mode.

The warning box, shown below, appears.



2 Click OK.

3 Click on a pin, via, or trace on the net to be repaired.

Using Undo and Redo

Undo restores the design to its state before the last EditRoute command. Some EditRoute operations, such as moving routes, can cause many traces to change. Undo restores the state that existed before the last interactive route operation. Redo reverses Undo. All EditRoute operations, except Repair Net, can be reversed with Undo.

Edit/Undo and Edit/Redo are available from the menu bar. Or, depending on the keyboard, use the function keys summarized in the following table.

Function	Key Selections
Undo	<Undo> <F3>
Redo	<Shift Undo> <Shift F3>

Checking Design Rule Violations

EditRoute checks and marks design rule violations. However, not all design rule violations are marked—for example, acute angles.

It is useful to generate a conflicts report before ending the interactive routing session. Some conflicts may remain because checking was disabled during the routing or editing session. Use the conflicts report to verify that all violations are resolved.

To check for design rule violations

1. Enable (check) the Checking box on the status line at the bottom of the SPECCTRA subwindow.
2. Select Report/Conflicts.

Layout Editor Interface-to-Autorouting Reference

Previous Chapter

Index

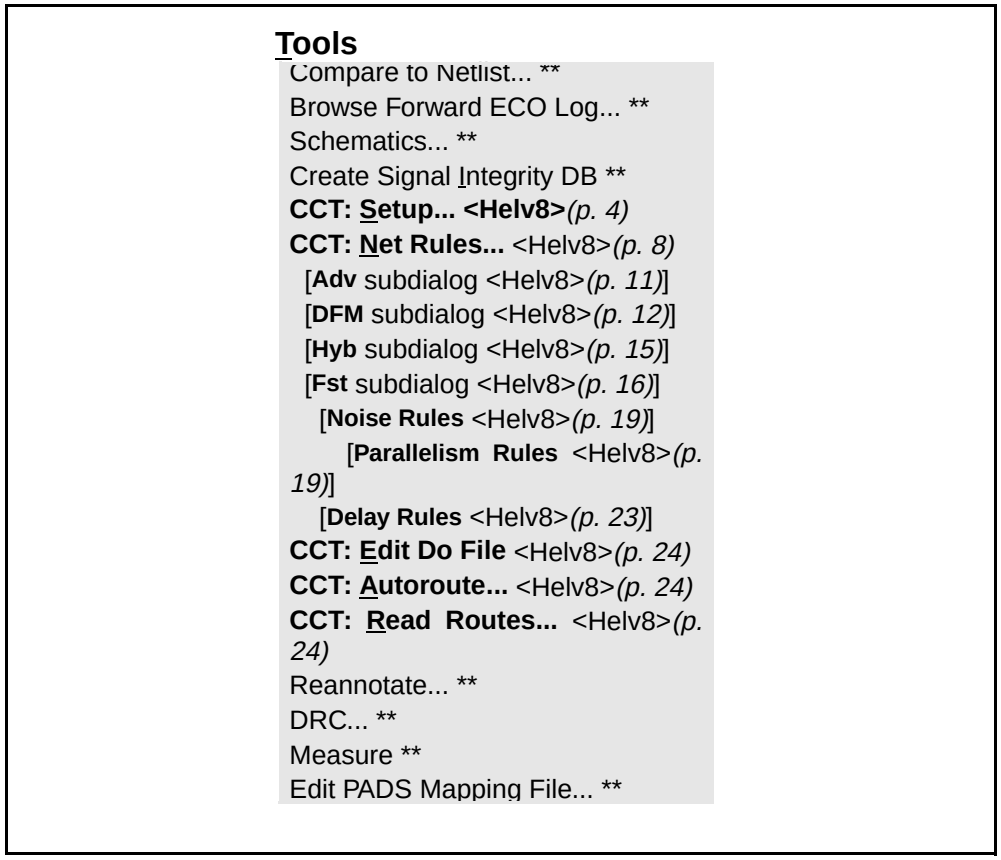
Introduction

The PCBoards Layout Editor provides menu selections and dialogs used to setup and execute a SPECCTRA autorouting run, and to incorporate completed routes into the Layout Database. These controls are used to:

- Set board-wide (default) layout rules
- Set net-specific layout rules
- Preset manufacturability and test requirements
- Set controls for vias used in SMT designs
- Set rules for coupled noise and timing in high-speed circuits
- Edit the SPECCTRA Do file for custom strategies and special-case autorouting commands
- Start the autorouter
- Apply completed routes to the Layout Database

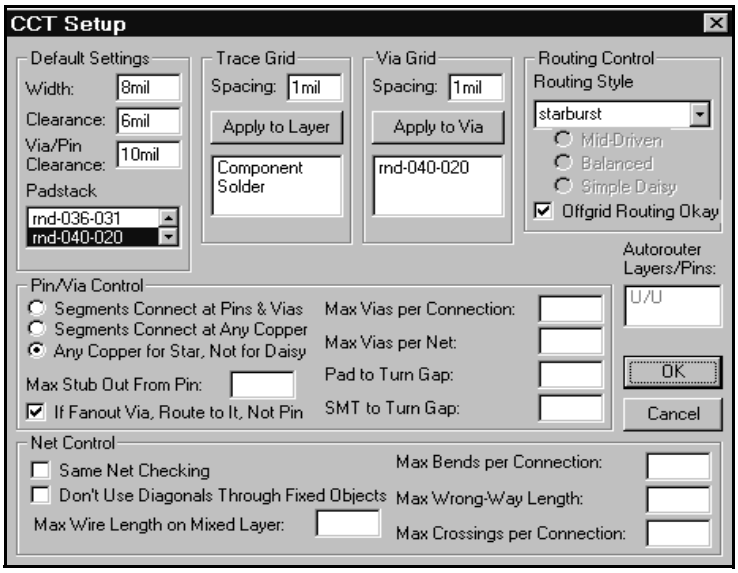
Tools Menu: SPECCTRA Interface

The menu items pertaining to setting up and running Cooper &Chyan Technology's (CCT) SPECCTRA autorouter are found in the Tools menu—shown in bold below. The remainder of this chapter describes the CCT menu selections, dialogs, and subdialogs.



CCT: Setup

The CCT: Setup dialog box is used to define board-wide layout rules such as: default trace properties, grid size for routing and via placement, routing style, connection rules, layer pairs, and trace topology constraints.



Corresponding rules are written to the Do file. Select Tools/CCT: Edit Do File to view or update this file. Refer to **Custom Setup and Strategies—Using the Do File** for more information.

To set new defaults

1. Enter values into the:
   - Default Settings
   - Routing Control
   - Net Control
   - Pin/Via Control
2. Set the grid spacings in: Trace Grid and Via Grid.
3. Define the required set of signal layer pairs in Layer Pairs.
4. Click OK.

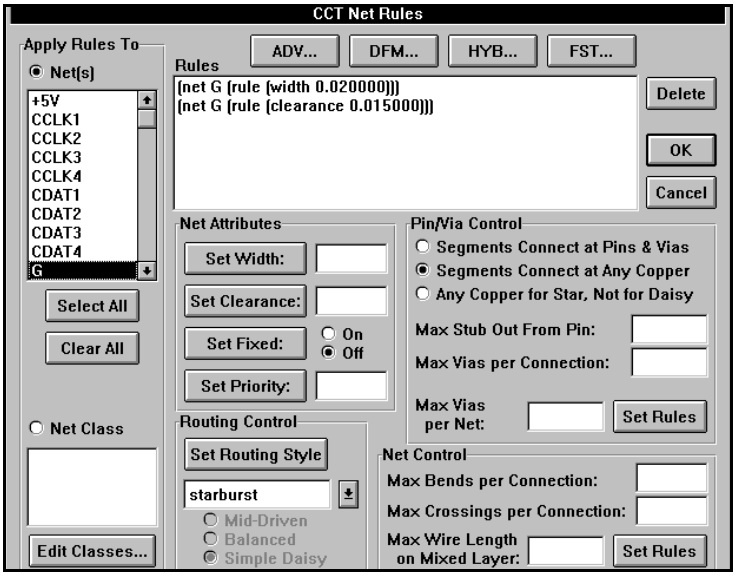
Section	Description	Format/Notes
Default Settings	Defines the trace properties applied to all nets that do not have custom settings.	
Width	Defines the trace thickness.	<*width value*>[*units*]
Clearance	Defines the required space between the trace and other layout objects.	<*clearance value*>[*units*]
Via / Pin Clearance	Defines the required space between traces and padstacks associated with vias and pins. The initial value is the largest clearance of all pin and via padstacks in the design.	<*clearance value*>[*units*]
Via Padstack	Defines the padstack definition to be used for vias unless there is an overriding net rule (see the ADV subdialog on page 7-11). This list contains only the round padstack definitions that are currently available for use.	
Trace Grid	Defines the default grid spacing for routing. Either a single board-wide grid can be set, or different grids can be used for different layers. To set up different grids, enter dimension values, select one or more layers in the Apply to Layer list, and click Apply.	
Spacing	Defines the horizontal and vertical grid spacing.	<*grid spacing*>[*units*]
Apply to Layer	Lists the configured signal layers. A selection from this list is associated with the current dimension when the Apply button is chosen.	
Via Grid	Defines the minimum grid spacing for via placement applied to all routing passes after the first three. For the first three passes, the autorouter calculates a larger initial via grid that allows two wires between vias.	To use one via grid for all passes, replace the smart route command in the Do file with a route <# of passes> command.
	Either a single board-wide grid can be set, or different grids can be used for different via-padstack combinations. To set up different grids, enter the dimension, select one padstack definition in the Apply to Via list, and click Apply.	<*grid spacing*>[*units*]
Spacing	Defines the horizontal and vertical grid spacing.	
Apply to Via	Lists the available padstack definitions. A selection from this list is associated with the current dimension when the Apply button is chosen.	
Routing Control	Defines how trace segments are established for a given net—i.e., placement order and position on / off the trace grid.	

Section	Description	Format/Notes
Routing Style	Defines the order in which trace segments should be joined. To set this, choose either `Daisy` or `Starburst` from the drop-down list.	
Starburst	Uses a minimum spanning tree algorithm and permits multiple entries and exits on pins.	
Daisy	Permits only a single entry and a single exit for the net on each pin.	
Mid-driven / Balanced / Simple Daisy	Determines the kind of daisy-chain ordering that will be implemented.	
Mid-driven	Causes a terminator to be placed at each end of the net, and the loads are added back to a source. There must be exactly two terminators, or the net is ordered as a simple optimized daisy chain. If there is more than one source, the sources are chained together first before the rest of the net is processed.	
Balanced	Evenly distributes loads between source and terminator pins. If more than one source pin is defined, the terminator and load branches are chained back to the closest source pin and the remaining source pins are ordered as an optimal daisy chain.	To apply balanced ordering, the net must have at least one source pin and two or more terminator pins. If not, the net is ordered as a simple optimized daisy chain.
Simple Daisy	Disallows tjunctions. Unless otherwise specified, Simple Daisy is the method used when Daisy is selected from the drop-down list.hhen	
Off-grid routing OK	Allows the router to place traces and vias between the routing and via grid lines, respectively.	
Pin / Via Control	Parameters define the constraints for connecting trace segments to other metal.	
Segments Connect at Pins & Vias	Limits trace connections to pins and vias only.	
Segments Connect at Any Copper	Allows trace connections to pins, vias, and other segments.	
Any Copper for Star, Not for Daisy	Restricts daisy chain orderings to connect to pins and vias. Starburst orderings can connect to pins, vias, and areafills.	
Max Stub Out from Pin	Defines the maximum stub length allowed on daisy-chain connections. Stub length is measured from the edge of the pad to the center of the tjunction.	*<stub length>*[*units*] where a length value of 0 disallows stubs
If Fanout Via, Route to It (Not Pin)	Enforces connections to existing fanouts rather than corresponding pins, when checked.	

Section	Description	Format/Notes
Max Vias per Connection	Defines the total number of vias that may be established for a pin-to-pin connection.	<*integer*>
Max Vias per Net	Defines the total number of vias that may be used for a net.	<*integer*>
Pad-to-Turn Gap	Defines the minimum clearance between the edge of the pad to the first trace corner.	<*clearance value*>[*units*]
SMT-to-Turn Gap	Defines the minimum clearance between the edge of the SMT pad to the first trace corner.	<*clearance value*>[*units*]
Net Control	Define the limits and rules governing trace geometry. If this is enabled, and an ambiguous situation occurs, the autorouter might flag a net as having a violation when it does not. Verify that the violation is a true violation.	
Same Net Checking	Enables violation checking within an individual net, when checked.	
Don't Use Diagonal Through Fixed Objects	Disallows diagonal trace segments through immovable objects like components, when checked.	
Max Wire Length on Mixed Layer	Defines the maximum length of a trace segment on a layer that also has areafills.	<*trace length*>[*units*]
Max Bends per Connection	Defines the maximum number of bend points that can be used in a pin-to-pin trace.	<*integer*>
Max Wrong-Way Length	Defines the maximum length of any trace segment routed in the direction opposite to the configured bias for a given layer (as established in the Configure / Layers dialog).	<*wrong-way length*>[*units*]
Max Crossings per Connection	Defines the maximum number of crossing conflicts a given pin-to-pin trace can have with existing traces.	<*integer*>
Autorouter Layers/Pins	Applies to network installations where multiple PCBoards licensing agreements are available. The list box shows all of the autorouter package configurations that are available on the network. When the dialog is first displayed, the highlighted autorouter package reflects the minimum configuration required to route the current design given the number of signal layers and pins.	The design can also be autorouted with any configuration supporting more layers and pins than used in the design. This can be useful when the autorouter setup requires options (Advanced, DFM, Hybrid, or Fast Circuit) not available in the minimum required autorouter configuration.

CCT: Net Rules

The CCT:Net Rules dialog box is used to define layout rules specific to nets and groups of nets (classes). The rules that can be set are similar to the board-wide defaults provided in the Tools/CCT: Setup dialog.



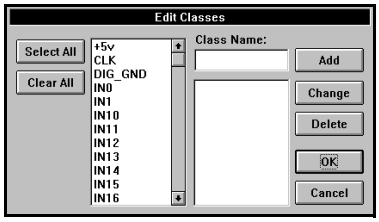
Nets and net classes with custom layout rules are displayed in the Rules list box. To set custom rules for individual nets, select one or more net entries in the Net(s) list box or one entry in the Net Class list box, specify the routing parameters, and click the corresponding Set <xxx> button. The corresponding rule is added to the Rules list. To delete a rule, select the rule statement in the Rules frame and click Delete.

When a net with custom rules also belongs to a net class with custom rules, the rules for the individual net take precedence. The precedence hierarchy is summarized in the section on **Repairing a Net**.

Section	Description
Apply Rules To	Used to assign layout rules to individual nets or net classes.
Net(s)	Indicates that the rule assignments apply to the one or more nets selected in the Net(s) list box.
Select All	Selects (highlights) all of the net names in the Net(s) list box. Subsequent clicks on highlighted entries will deselect them.
Clear All	Deselects all of the net names in the Net(s) list box. Subsequent clicks on highlighted entries will reselect them.
Net Class	Indicates that the rule assignments apply to the one net class selected in the Net Class list box.

Edit classes

To create a net class, type a name into the Net Class text box, select two or more entries in the Net(s) list box, then click Add. To change a net class definition, select one entry in the Net Class list box, toggle the selections in the Net(s) list box as required, and click Change. To remove a net class definition, select one entry in the Net Class list box and click Delete.



Rules

Lists the currently defined net and net class rules. Rules for individual nets and net classes are presented in CCT-rules syntax; for details, please refer to the Rules section of the **CCT Design Language Online Reference Manual**.

Net Attributes

Net Attributes parameters define the trace properties that are applied to the currently selected net(s) or net class when routed, or whether to prevent them from being routed.

Parameter	Description
Set Width	Defines the trace thickness. To set this, enter a value using the format <width value>[units] and click Set Width. **Alternate Method**: Set the NET_TRACE_WIDTH attribute on the relevant net(s).
Set Clearance	Defines the required space between the trace and other layout objects. To set this, enter a value using the format <clearance value>[units] and click Set Clearance. **Alternate Method:** Set the NET_CLEARANCE attribute on the relevant net(s).
Set Fixed	Determines whether the selected net(s) or net class are excluded from routing and rerouting. When On is chosen, the selected net(s) are excluded. To set this, click on either On or Off, then click Set Fixed. **Alternate Method:** Set the NET_FIXED attribute on the relevant net(s).
Set Priority	Used to schedule the routing order amongst nets and net classes. To set this, enter a value suing the format <0≤integer priority value ≤255>and click Set Priority. The highest priority is 255; default priority is 10. When assigning priorities to multiple nets, separate each entry by 10 or more. **Alternate Method:** Set the NET_PRIORITY attribute on the relevant net(s).

Routing Control

Routing control parameters define how a net's connections are scheduled for routing and how trace segments are established for an individual net or net class—i.e., placement order and position on/off the trace grid. See **Routing Control** for descriptions of the Routing Style, Mid-driven, Balanced, and Simple Daisy controls. Use the Set Routing Style button to save the settings for the selected net(s) or net class.

Pin/Via Control

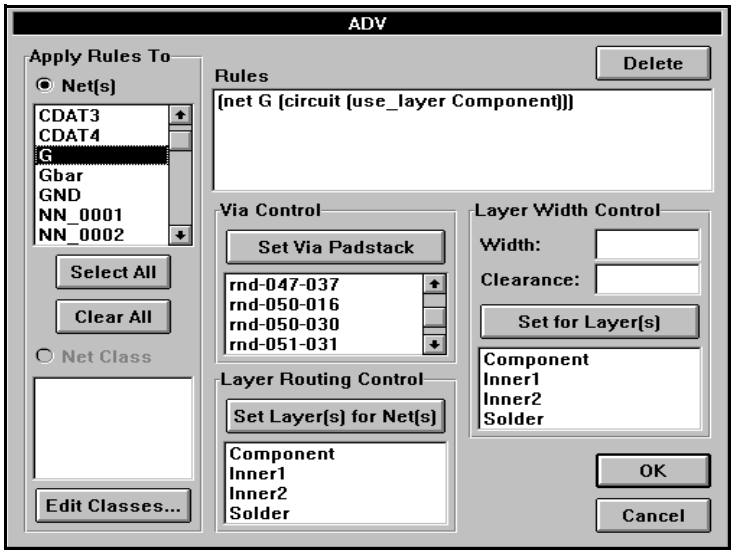
Pin/Via Control parameters define the constraints for connecting trace segments to other metal for the currently selected net(s) or net class. See **Pin / Via Control** for descriptions of all of the parameters. Use the Set Rules button to save the settings for the selected net(s) or net class.

Net Control

Net Control parameters define the limits governing trace geometry for the currently selected net(s) or net class. See **Net Control** for descriptions of the Max bends per connection, Max crossings per connection, and Max wire length on mixed layer controls. Use the Set Rules button to save the settings for the selected net(s) or net class.

ADV

Displays a dialog used to assign via-padstacks to nets, nets to layers, and trace properties to layers. This capability is only available with autorouters that include the Advanced option.



Rule assignments to one or more nets or to a net class are made in the same way as in the Tools/CCT: Net Rules dialog. See **CCT: Net Rules** for a description of the Apply Rules To and Rules frames

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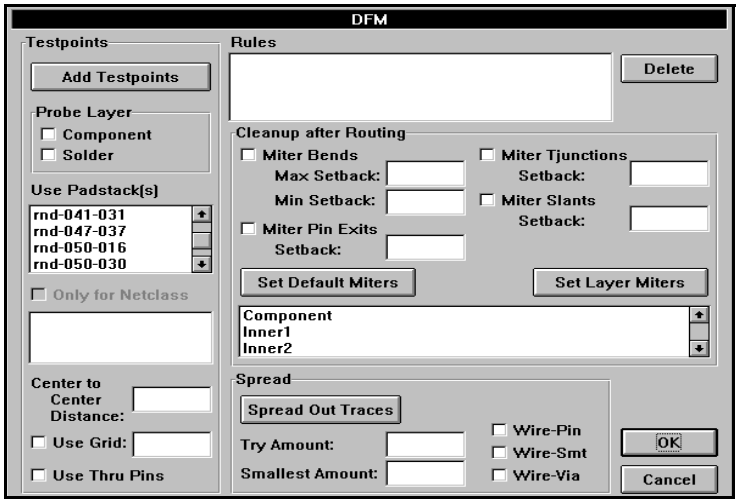
Parameter	Description
Via Control	Define the via-padstack association to be used for selected net(s) or net classes. To define a custom via-padstack association for the chosen net(s), select one padstack definition within the list box and click Set Via Padstack. To create new padstack definitions, use Configure / Padstacks.
Layer Routing Control	Define the layers on which specific nets must be routed. To define net-layer associations, select one or more layers within the list box and click Set Layer(s) for Net(s).
Layer Width Control	Define the trace properties for the currently selected layers and currently selected net(s) or net classes. To define custom trace properties per layer, enter values for Width and Clearance, select one or more layers within the list box, and click Set for Layer(s).
Width	Defines the trace thickness. Format is <*width value*>[*units*].
Clearance	Defines the required space between the trace and other layout objects. Format is <*clearance value*>[*units*].

DFM

Displays a dialog used to define layout rules that address manufacturing and test requirements—addition of test points, increased clearances, and elimination of 90-degree corners on routed signal nets. This capability is only available with autorouters that include the DFM option.



See **CCT: Net Rules** for a description of the Rules frame.

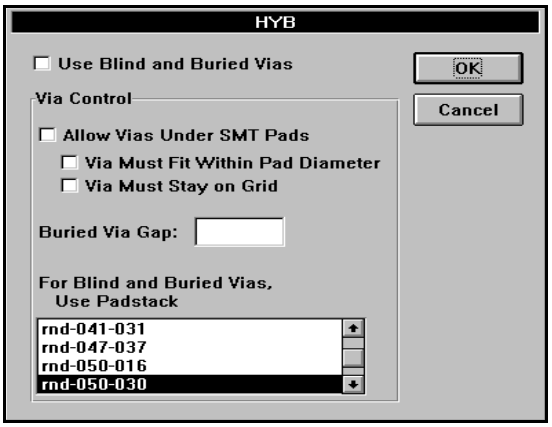
Parameter	Description
Testpoints	Used to create testpoints with identical properties for all nets, or to create testpoints with different properties for different net classes. Exposed vias (not covered by a component on the probing layer(s)) and through-hole pins that already exist in the design are used where appropriate. If needed, new exposed vias are created. To create test points, set the properties in the Testpoints frame and click Add Testpoints.
Probe Layer	Defines the surface(s) on which a new test via should be exposed for probing. Component, when checked, defines the [Top] layer as the probing layer. Solder, when checked, defines the [Bottom] layer as the probing layer. Checking both boxes will create a test point that is exposed on both surfaces.
Use Padstack(s)	Lists the available padstack definitions that can be associated with through-hole vias. Select one or more definitions from this list.
Only for Netclass	Adds the test point to the selected netclass only. Otherwise, testpoints with the specified properties are added to all nets. To set this, check the Only for Netclass box and select a netclass entry in the corresponding list box.
Center-to-Center Distance	Defines the minimum center-to-center spacing between test points. Format is <test point spacing>[units].

Parameter	Description
Use Thru Pins	Allows the autorouter to use existing through-hole pins as test points.
Use Grid	Causes the autorouter to use the grid spacing defined in the corresponding Use Grid text box for test point vias. Format is <probing grid spacing>[units]. When unchecked, the via grid specified under Tools/CCT: Setup is used.
Cleanup after Routing	Used to eliminate 90-degree corners. To define default mitering rules, fill in the Cleanup after Routing properties and click Set Default Miters. To define layer-specific mitering rules, fill in the properties, select one or more layers from the layers list box at the bottom of the frame, and click Set Layer Miters.
Miter bends	Allows the autorouter to attempt to replace all 90-degree segment-to-segment corners with 135-degree cuts for the selected net(s) or net class. The Max Setback value is used as a starting point. When all attempts fail during the initial iteration, the value of Max Setback is divided by two and the new value is used when attempting to miter all remaining 90-degree corners. If required, additional iterations are attempted using the previous setback value divided by two. When the setback value is less than Min Setback, the mitering operation terminates.
Max Setback	Defines the initial horizontal and vertical distance from the vertex that can be used when mitering corners. Format is <maximum setback distance>[units]. When unspecified, Max Setback defaults to one-half inch.
Min Setback	Defines the smallest horizontal and vertical distance from the vertex that can be attempted. Format is <minimum setback distance>[units]. When unspecified, Min Setback defaults to trace width.
Miter pin exits	Replaces 90-degree corners from pin-leads with 135-degree cuts when the pin-to-corner length is equal to or greater than Setback.
Setback	Defines the minimum pin-to-corner distance required before mitering is applied. Format is <minimum setback distance>[units]. When unspecified, Setback defaults to one inch.
Miter tjunctions	When checked, adjusts trace segments at tjunctions to have 135-degree cuts starting at the value of Setback.
Setback	Defines the minimum distance from the junction to the start of the 135-degree cut. Format is <minimum setback distance>[units]. When unspecified, Setback defaults to one inch.
Miter slants	Replaces wrong-way segments with 135-degree segments when the wrong-way length is equal to or greater than the corresponding Setback value.
Setback	Defines the wrong-way segment length required before mitering is applied. Format is <minimum setback distance>[units]. When unspecified, Setback defaults to one inch.

Parameter	Description
Spread	Used to increase clearances between traces and other metal (pads). The autorouter makes incremental attempts (up to five) to adjust the position of trace segments using progressively smaller clearance values. If an adjustment would result in a conflict, it is not made. The first pass attempts to add the value of Try Amount to the existing clearances. After the first pass, Try Amount is divided by two, and that value is attempted for the second pass. This process continues until the divide-by-two operation results in a value equal to or less than Smallest Amount, or five passes have been completed
Try Amount	Defines the starting clearance increment to be used to spread out traces and other metal. Format is <largest clearance delta>[units]. When unspecified, Try Amount defaults to one-half the Via/Pin Clearance set in the Tools/CCT: Setup dialog.
Smallest Amount	Defines the lowest clearance increment that can be used to spread out traces and other metal. Format is <smallest clearance delta>[units].
Wire-Pin/ Wire-SMT/ Wire-Via	Govern which clearances should be increased using the algorithm and values described above. Wire-Pin, when checked, allows trace-to-pad (through-hole pin) clearances to be increased. Wire-SMT, when checked, allows trace-to-SMT-pad clearances to be adjusted. Wire-Via, when checked, allows trace-to-via clearances to be adjusted. If no boxes are checked (the default), all types of spread are allowed.

HYB

Displays a dialog used to define layout rules for blind and buried vias. This capability is only available with autorouters that include the Hybrid option.



To define custom vias, set the properties in the Via Control frame and click OK.

Use blind and buried vias

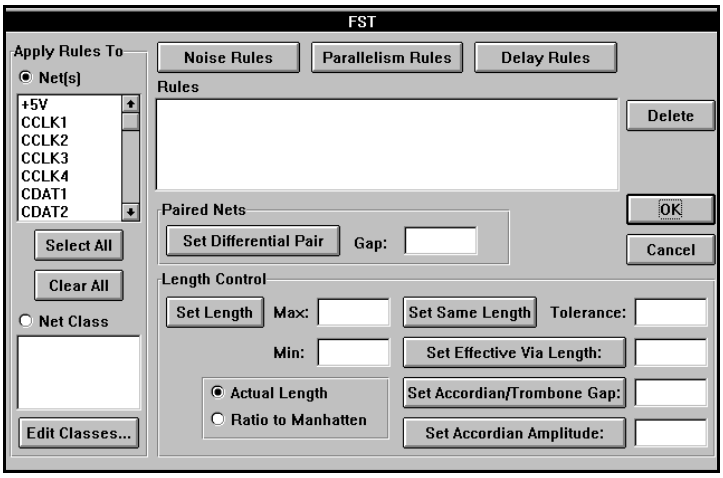
When checked, causes PCBoards to create and apply blind and buried via padstacks based on the currently selected padstack definition in the Use Padstack list and the signal layers specified in the design. When unchecked, only through-hole via padstacks are used.

Via control

Parameter	Description
Allow Vias under SMT Pads	Permits via placement under surface mount pads when checked. To further constrain via placement, check Via Must Fit within Pad Diameter and/or Via Must Stay on Grid as required.
Buried Via Gap	Defines the clearance between buried vias on different layers. Format is <clearance value>[units].
For Blind and Buried Vias, Use Padstack	Lists the existing padstack definitions that can be assigned to the blind and buried vias used in the layout. New definitions can be added using Configure/Padstacks.

FST

FST displays a dialog used to define layout rules that address high-speed circuit requirements to prevent coupled noise and timing problems—trace length limits, differential (balanced) pairs, shielding, noise margins, parallel trace proximity limits, and delay limits This capability is only available with autorouters that include the Fast option.



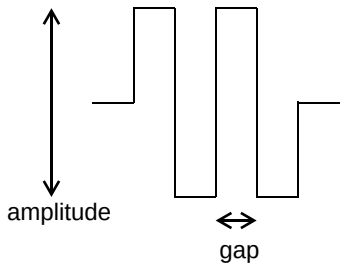
Rule assignments are made in the same way as in the Tools/CCT: Net Rules dialog. See **CCT: Net Rules** for a description of the Apply Rules To and Rules frames.

When setting timing controls, a net or net class cannot have both length rules (defined in this dialog) and delay rules (defined in the Tools/FST/Delay Rules dialog). If both length and delay rules have been defined, the autorouter will use the last rule defined. Check the Rules frame for any possible conflict. The rules are listed in the same order they are read by the autorouter.

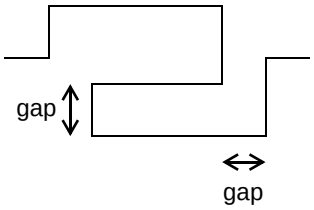
Paired Nets

Parameters	Description
Set Differential Pair	Routes two nets in parallel. To do so, select exactly two nets in the Net(s) list box (in the Apply Rules To frame), enter a Gap value, and click Set Differential Pair.
Gap	Defines the spacing between the two parallel nets. Format is <clearance value>[units].
Length Control	Used to control timing by setting physical limits on the trace length in terms of actual dimension or as a ratio of Manhattan length to the routed length.
Set Length	Defines the largest and smallest allowable lengths for a routed net. To set this, enter values for Max and Min, and click Set Length.
Max	Defines the largest allowable length for a routed net. When Actual Length is selected (see below), format is <maximum trace length>[units]. When Ratio to Manhatten is chosen, format is <Manhatten length/routed length>.
Min	Defines the smallest allowable length for a routed net. When Actual Length is selected (see below), format is <maximum trace length>[units]. When Ratio to Manhatten is chosen, format is <Manhatten length/routed length>.
Actual Length/ Ratio to Manhatten	Choices govern how the autorouter will interpret the length limits. When Actual Length is chosen, the autorouter interprets the values as the physical dimensions. When Ratio to Manhatten is chosen, the autorouter interprets the values as multipliers of the Manhatten length.
Set Same Length	Routes all nets in a net class with the same length within the specified value of Tolerance. To set this, enter a value for Tolerance using the format <tolerance value>[units], and click Set Same Length.
Effective Via Length	Defines the length to be used for vias when calculating trace length. To set this, enter a value using the format <via length>[units] and click Effective Via Length.
Set Accordian/ Trombone Gap	Defines the minimum space between parallel segments of the same trace when routed in either an accordian or trombone pattern. To set this, enter a value using the format <segment-to-segment spacing>[units] and click Set Accordian/Trombone Gap.
Set Accordian Amplitude	Defines the side-to-side excursion of a trace segment for a trace routed in an accordian pattern. To set this, enter a value using the format <excursion distance>[units] and click Set Accordian Amplitude.

Accordian Pattern

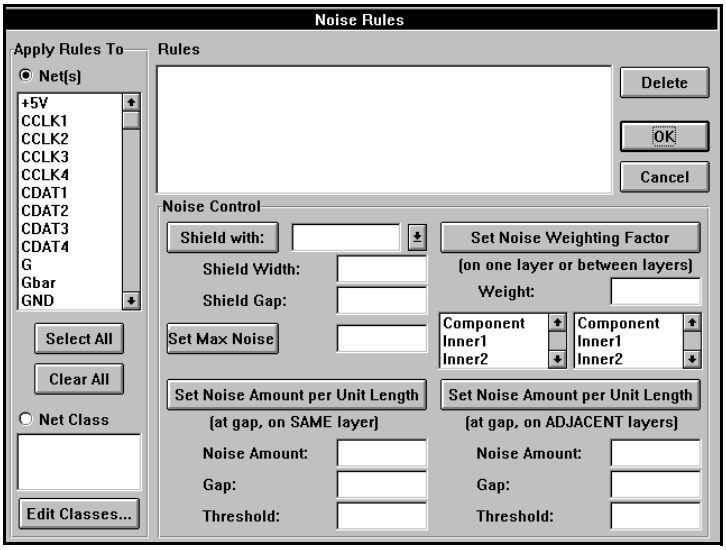


Trombone Pattern



Noise Rules

Noise Rules displays a dialog used to define noise margins, shielding, and noise estimates per unit length for calculating total noise. This capability is only available with autorouters that include the Fast option.



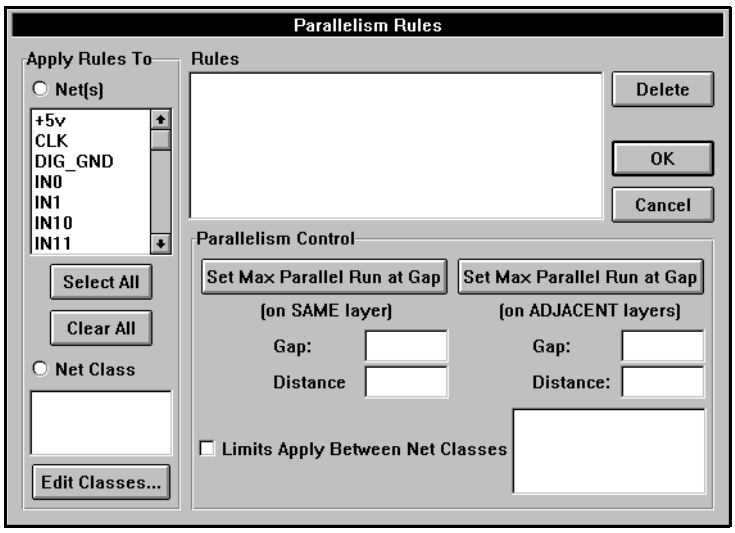
Rule assignments to one or more nets or to a net class are made in the same way as in the Tools/CCT: Net Rules dialog. See **CCT: Net Rules** for a description of the Apply Rules To and Rules frames.

Noise Control Parameters

Parameters	Description
Shield with	Defines the net and net properties that the autorouter must use to shield the selected net(s) or net class from ground. To set this, select a net from the drop-down list; (only those nets assigned to the power plane are available for shielding), enter values for Shield Width and Shield Gap, and click Shield with.
Shield Width	Defines the width of the shielding trace. Format is <width value>[units].
Shield Gap	Defines the spacing between the signal trace and the shielding trace. Format is <clearance value>[units].
Set Max Noise	Defines the noise margin within which total noise calculations for the net should remain. If total calculated noise exceeds this value, a coupled noise violation is reported. To set this, enter a value using the format <total allowable noise in volts or mvolts> and click Set Max Noise.

Parameters	Description
Set Noise Weighting Factor	Used to create a table of weighting factors that the autorouter can use to calculate coupled noise between parallel segments on the same layer or adjacent layers for the selected net(s) or net class (on one layer or between layers). To set a weighting factor for one layer, enter the Weight value, select one layer name in either list box, and click Set Noise Weighting Factor. To set a weighting factor for a layer pair, enter a Weight value, select the upper layer in the left-hand list box, select the lower layer in the right-hand list box, and click Set Noise Weighting Factor.
Weight	Defines the weighting factor assigned to the layer or pair of layers selected in the corresponding list boxes. Format is <0 £ decimal weighting factor £ 1>.
Set Noise Amount per Unit Length (at gap, on ADJACENT layers)	Settings provide the autorouter with criteria for calculating coupled noise between parallel segments on adjacent layers for the selected net(s) or net class. The calculation is only made when the Gap and Threshold requirements are met. To set this, enter noise calculation criteria
Noise Amt	Defines the noise per unit of routed length. Format is <noise in volts or mvolts> per current default units (mils or mm as defined in Tools/Options).  Be sure to specify Noise Amt in the same units as the Set Max Noise value.
Gap	Defines the clearance between traces below which parallel noise calculations are made. Format is <clearance value>[units].
Threshold	Defines the minimum parallel length before parallel noise calculations are made. Format is <length value>[units].
Set noise amount per unit length (at gap, on SAME layer)	Settings provide the autorouter with criteria for calculating coupled noise between parallel segments on the same layer for the selected net(s) or net class. The calculation is only made when the Gap and Threshold requirements are met.
Noise Amt	Defines the noise per unit of routed length. Format is <noise in volts> per current default units (mils or mm as defined in Tools/Options).  Be sure to specify Noise Amt in the same units as the Set Max Noise value.
Gap	Defines the clearance between traces below which parallel noise calculations are made. Format is <clearance value>[units].
Threshold	Defines the minimum parallel length before parallel noise calculations are made. Format is <length value>[units].

Parallelism Rules



Parallelism Rules displays a dialog used to control coupled noise between parallel trace segments. This capability is only available with autorouters that include the Fast option.

Rule assignments to one or more nets or to a net class are made in the same way as in the Tools/CCT: Net Rules dialog. See **CCT: Net Rules** for a description of the Apply Rules To and Rules frames.

Parallelism Control

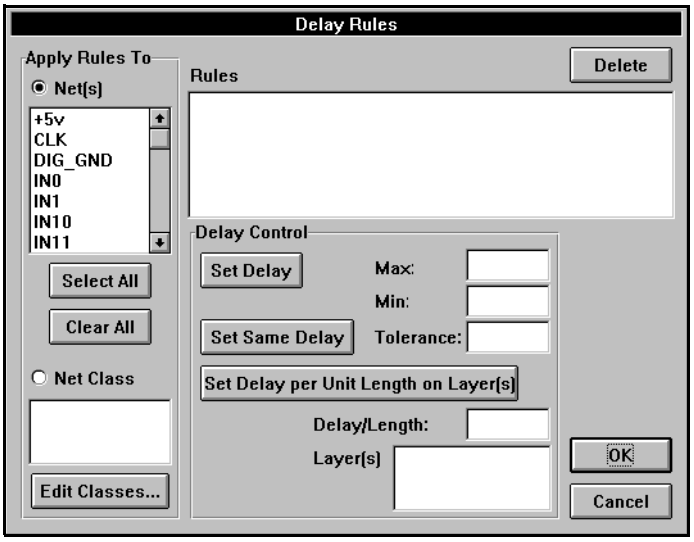
Parameter	Description
Set Max Parallel Run at Gap (on SAME layer)	Settings provide the autorouter with length and spacing requirements when routing parallel trace segments on the same layer. If these constraints are not adhered to, a parallel segment violation is reported. To set this, enter Gap and Distance values, and click Set Max Parallel Run at Gap (on same layer).
Gap	Defines the minimum trace-to-trace spacing that must exist between parallel trace segments (on the same layer) of length up to that specified by Distance. Format is <minimum trace-to-trace spacing>[units].
Distance	Defines the maximum trace segment length that can run parallel to another trace segment on the same layer, and must clear the parallel segment by at least the value of Gap. Format is <maximum parallel trace segment length>[units].
Set Max Parallel Run at Gap (on ADJACENT layers)	Settings provide the autorouter with length and spacing requirements when routing parallel trace segments on adjacent layers. If these constraints are not adhered to, a parallel segment violation is reported. To set this, enter Gap and Distance values, and click Set Max Parallel Run at Gap (on ADJACENT layers).

Parameter	Description
Gap	Defines the minimum trace-to-trace spacing that must exist between parallel trace segments (on an adjacent layer) of length up to that specified by Distance. Format is <minimum trace-to-trace spacing>[units].
Distance	Defines the maximum trace segment length that can run parallel to another trace segment on an adjacent layer, and must clear the parallel segment by at least the value of Gap. Format is <maximum parallel trace segment length>[units].
Limits Apply Between Net Classes	When checked, enforces length and spacing requirements on parallel trace segments between net classes selected from the accompanying list box.

Delay Rules

Delay Rules displays a dialog used to define total and per-unit-length delay limits. This capability is only available with autorouters that include the Fast option.

A net may have either length or delay rules, but not both.



Rule assignments to one or more nets or to a net class are made in the same way as in the Tools/CCT: Net Rules dialog. See **CCT: Net Rules** for a description of the Apply Rules To and Rules frames.

Delay Control

Parameter	Description
Set Delay	Defines the largest and smallest allowable time delays for the selected net(s) or net class. To set this, enter values for Max and Min, and click Set Delay.
Max	Defines the maximum amount of allowed time delay. Format is <delay value in nsec> where delay value can have up to three decimal places.
Min	Defines the minimum amount of allowed time delay. Format is <*delay value in nsec*> where *delay value* can have up to three decimal places.
Set Same Delay	Used to route all nets in a net class with the same total delay within the specified value of Tolerance. To set this, enter a value for Tolerance using the format <tolerance value>, and click Set Same Delay.
Set Delay Per Unit Length on Layer(s)	Settings provide the autorouter with time delay criteria for a given layer. To set this, enter delay per unit length in the Delay/Length edit control, select one or more assignments in the Layer(s) list, and click Set Delay Per Unit Length on Layer(s).
Delay/Length	Defines the delay per unit length. Format is <time delay in nsec> per current default units (mils or mm as defined in Tools/Options).
Layer(s)	Lists the signal layers to which delay values can be assigned.
CCT: Edit Do File	Opens the Do file for viewing and update. PCBoards automatically configures the Do file with command statements appropriate for the autorouting setup values in the Tools/CCT: Setup dialog, Tools/CCT: Net Rules dialog, and corresponding subdialogs. For selected commands, it is necessary to edit this file directly. Refer to **Custom Setup and Strategies—Using the Do File** for details on Do file structure and function, and the **CCT Design Language Online Reference Manual**.
CCT: Autoroute	Invokes the Cooper and Chyan Technology SPECCTRA autorouter. The autorouter uses the current setup instructions and layout rules defined in the Tools/CCT Setup and Tools/CCT: Net Rules dialogs, respectively. By default, the autorouter evaluates the design and determines the best strategy for fanout, routing, and cleanup. For custom strategies, the Do file can be edited.
CCT: Read Routes	Loads the routes database created with Tools/CCT: Autoroute into the Layout Database. Any existing traces that are redundant with the traces in the routes database are replaced.

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