

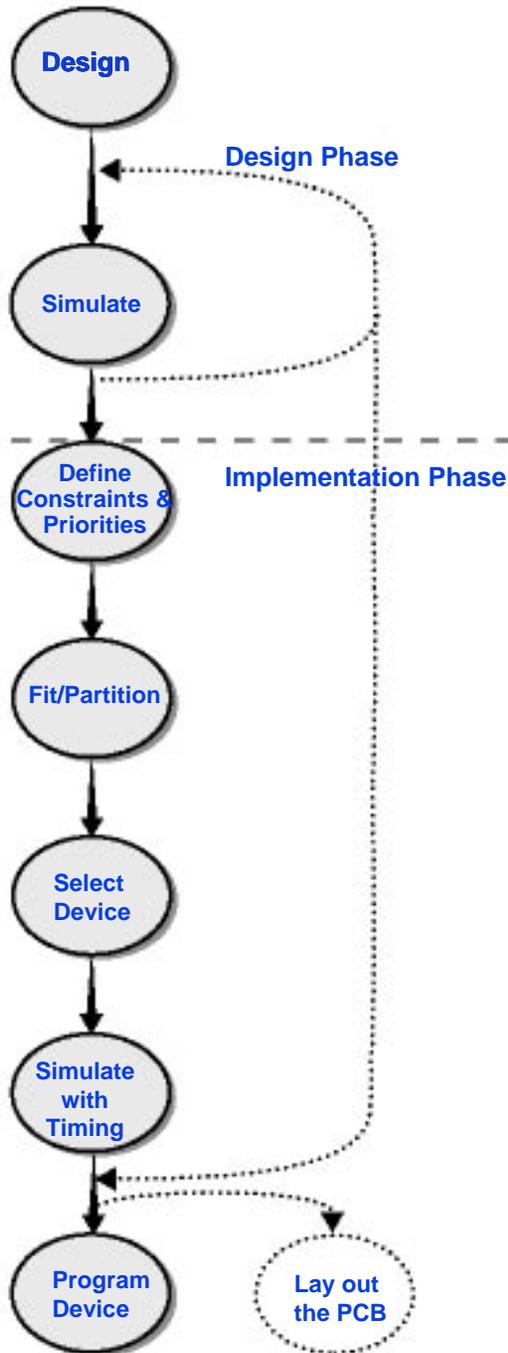
What Is MicroSim PLSyn?

- Used to design PLDs (Programmable Logic Devices) and CPLDs (Complex PLDs).
- Works with MicroSim Schematics and MicroSim PSpice A/D.
- Includes a part library with up to 3,500 PLDs and CPLDs from 12 manufacturers: Altera, AMD, Atmel, Cypress, ICT, Lattice, and more!
- Allows mixed-mode (schematic and language) design entry.
- Automatically partitions your design into multiple devices (with the PLSyn Partitioning option).
- Only PC-based tool that can integrate PLDs and CPLDs into your overall mixed analog/digital system design.

Why Use MicroSim PLSyn?

- **Create** integrated designs combining PLDs and CPLDs with analog and discrete digital devices.
- **Generate** a list of device solutions that meet your design specifications; you then select the configuration that best fits your design.
- **Perform** functional simulation (before fitting and part selection).
- **Perform** timing simulation (after part selection).
- **Generate** fuse map files.

Using MicroSim PLSyn



- 1 Enter your design in Schematics.
- 2 Perform functional simulation, and analyze simulation results in Probe.
- 3 Set device constraints and priorities.
- 4 Run the PLSyn fitter to create a list of device solutions; solutions can be a single device or multiple devices (with the Partitioning option).
- 5 Select a solution to implement your design.
- 6 Perform timing simulation, and analyze simulation results in Probe.
- 7 Generate fuse maps to program the PLDs and/or CPLDs in your design.



Part Browser Advanced

Part Name: Description Search:
Description: D-type flip-flop Create New Part List

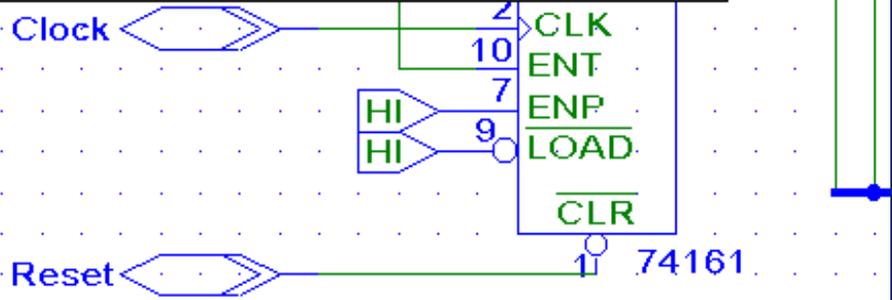
Library: c:\msim71\lib\dig_prim.slb

DFF
DFFC
DFFCR
DFFCRH
DFFCRS
DFFCRSH
DFFCS
DFFCSH
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DFFRS
DFFRSH
DFFS
DFFSH
DH0006
DH0006C
DH0006CH

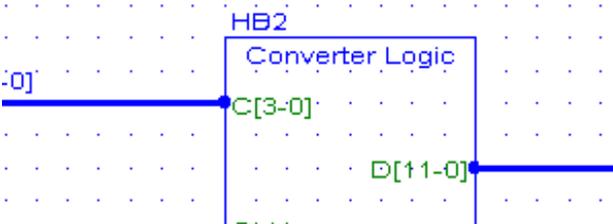
Placing Logic Symbols in Your Design

You can easily select and place logic symbols with the Part Browser.

Use generic (e.g., gates or flip-flops), or 7400 Series logic symbols.



Placing DSL Blocks in Your Design



DSL context-sensitive help by pressing F1.

```
sa_cntrl.dsl* - MicroSim Text Editor
File Edit Search View Insert Help

PROCEDURE SAPR(
  INPUT C1k, Cmp, C[3..0];
  OUTPUT D[11..0] CLOCKED_BY C1k DEFAULT_TO LAST_VALUE);

" Control logic for successive approximation AtoD converter

CASE C
  WHEN 0 => D = 100000000000b; "start with msb
  WHEN 1 => D[10] = 1; D[11] = Cmp;
  WHEN 2 => D[9] = 1; D[10] = Cmp;
  WHEN 3 => D[8] = 1; D[9] = Cmp;
  WHEN 4 => D[7] = 1; D[8] = Cmp;
  WHEN 5 => D[6] = 1; D[7] = Cmp;
  WHEN 6 => D[5] = 1; D[6] = Cmp;
  WHEN 7 => D[4] = 1; D[5] = Cmp;
  WHEN 8 => D[3] = 1; D[4] = Cmp;
  WHEN 9 => D[2] = 1; D[3] = Cmp;
  WHEN 10 => D[1] = 1; D[2] = Cmp;
  WHEN 11 => D[0] = 1; D[1] = Cmp;
  WHEN 12 => D[0] = 0; D[1] = Cmp;
END CASE;

END sapr;
```

Enter blocks of DSL (Design Synthesis Language) to specify logic for your design.

MicroSim PLSyn Help

File Edit Bookmark Options Help

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DSL CASE Statement

Syntax CASE *expression*
 WHEN *value_or_range* =>
 statements
 [ELSE
 statements]
END CASE;

Term	Description
<i>value_or_range</i>	a single value, a list of values, or a range of numbers to which <i>expression</i> is compared
<i>statements</i>	one or more statements. If any <i>expression</i> matches <i>value_or_range</i>

MicroSim Text Editor

Insert Template

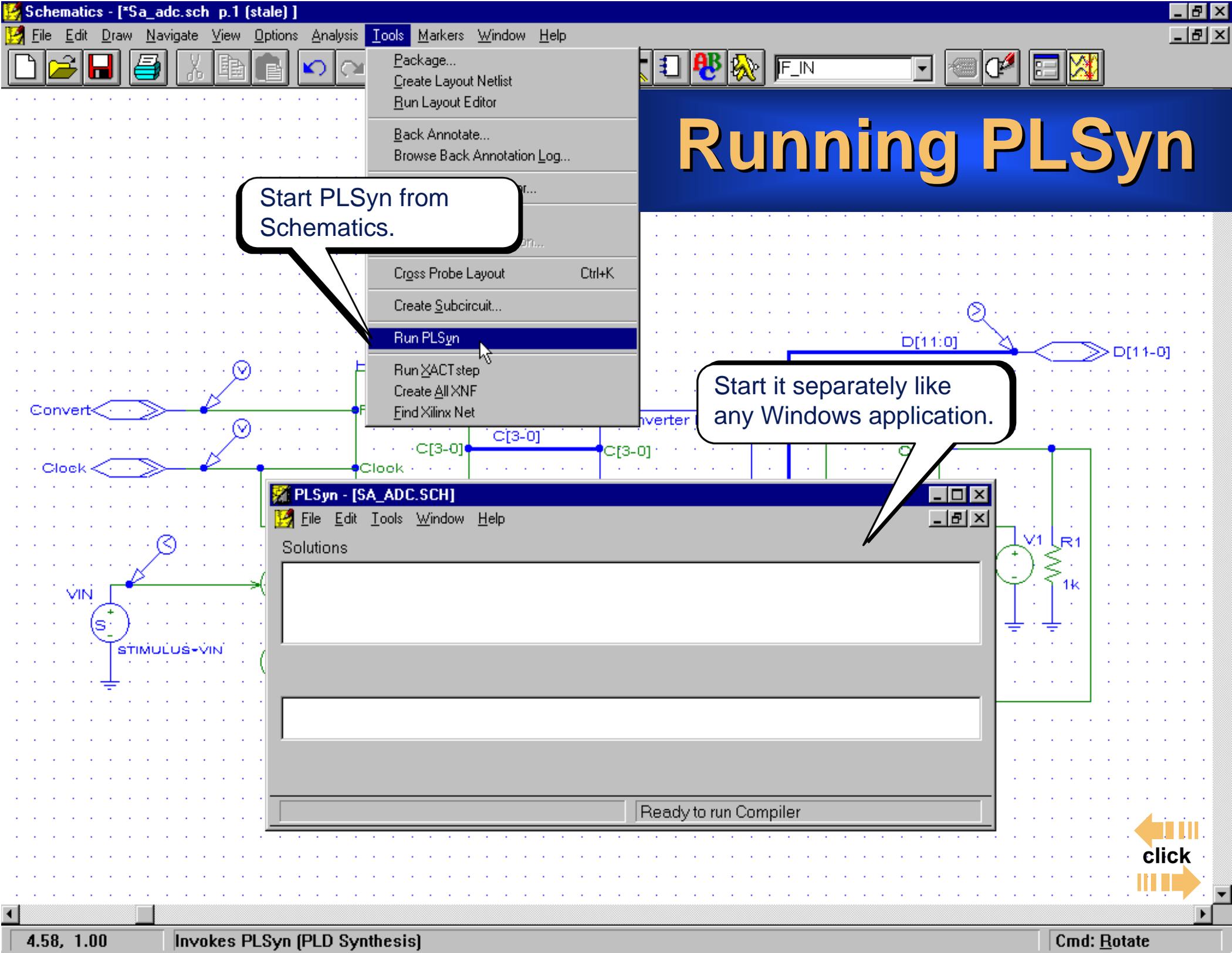
Available DSL templates:

- CASE
- D_FLOP (w/preset)
- D_FLOP (w/reset)
- D_FLOP (w/reset and preset)
- D_LATCH (w/preset)
- D_LATCH (w/reset)
- D_LATCH (w/reset and preset)
- FUNCTION
- IF
- IF-THEN-ELSE
- INCLUDE
- JK_FLOP (w/preset)
- JK_FLOP (w/reset)
- JK_FLOP (w/reset and preset)

Buttons: Insert, Cancel, Help

Insert pre-defined DSL "templates."





Running PLSyn

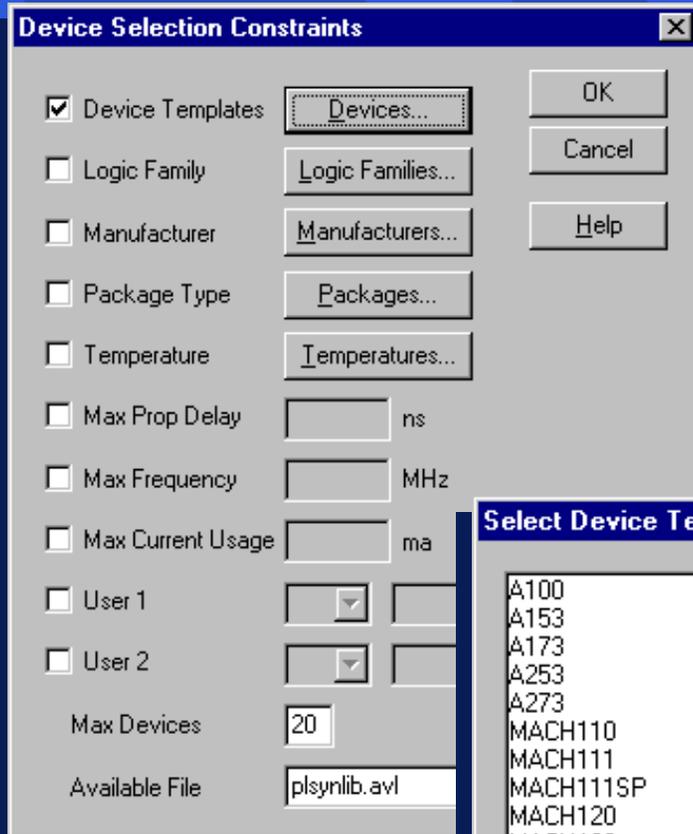
Start PLSyn from Schematics.

Start it separately like any Windows application.



Setting Constraints

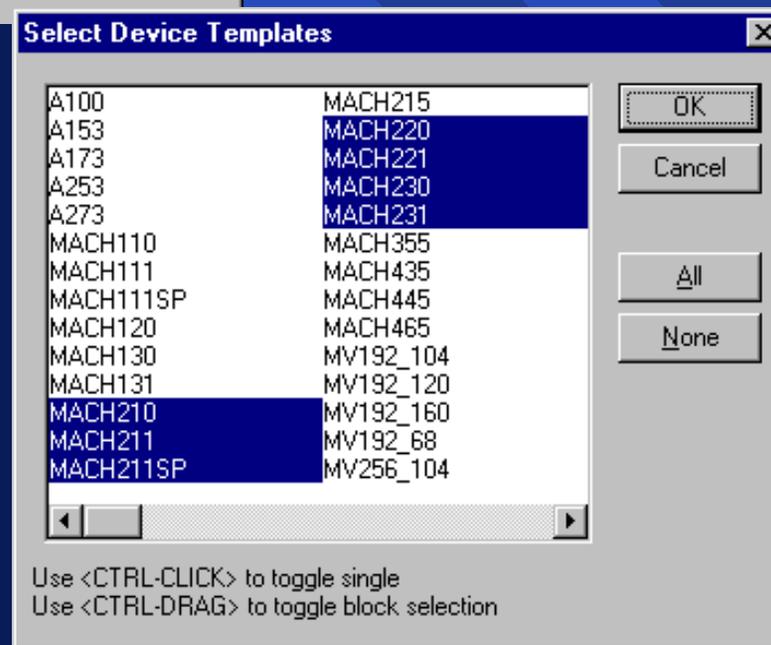
Constraints allow you to narrow the list of devices that the PLSyn fitter considers when searching for solutions to your logic design.



The 'Device Selection Constraints' dialog box contains the following settings:

- Device Templates: Devices...
- Logic Family: Logic Families...
- Manufacturer: Manufacturers...
- Package Type: Packages...
- Temperature: Temperatures...
- Max Prop Delay: [] ns
- Max Frequency: [] MHz
- Max Current Usage: [] ma
- User 1: [] []
- User 2: [] []
- Max Devices: 20
- Available File: plsynlib.avl

Buttons: OK, Cancel, Help



The 'Select Device Templates' dialog box displays a list of device templates:

A100	MACH215
A153	MACH220
A173	MACH221
A253	MACH230
A273	MACH231
MACH110	MACH355
MACH111	MACH435
MACH111SP	MACH445
MACH120	MACH465
MACH130	MV192_104
MACH131	MV192_120
MACH210	MV192_160
MACH211	MV192_68
MACH211SP	MV256_104

Buttons: OK, Cancel, All, None

Use <CTRL-CLICK> to toggle single
Use <CTRL-DRAG> to toggle block selection

Fitting the Logic

Select the solution that best meets your requirements.

Run the PLSyn Fitter to find solutions based on your constraints. Solutions can be a single device or

multiple devices with the same or different architectures.

PLSyn - [SA_ADC.sch]

File Edit Tools Window Help

Solutions

Solution	Configuration	Icc	Tmin	Price
1.	2 X P16V8A, P22V10	270ma	55ns	\$3.20
2.	P16V8A, P16R8, P22V10	280ma	55ns	\$3.22
3.	2 X P16R8, P22V10	290ma	55ns	\$3.24
4.	2 X P16V8A, P18V10	295ma	27ns	\$3.40
5.	P16V8A, P16R8, P18V10	305ma	33ns	\$3.42
6.	2 X P16R8, P18V10	315ma	33ns	\$3.44
7.	P16V8A, 2 X P22V10	270ma	55ns	\$4.45
8.	P16R8, 2 X P22V10	280ma	55ns	\$4.47
9.	P16V8A, P22V10, P18V10	295ma	55ns	\$4.65
10.	P16R8, P22V10, P18V10	305ma	55ns	\$4.67

Solution Detail

Device Name

PALCE16V8-25JC
PALCE16V8-25JC

Select Device

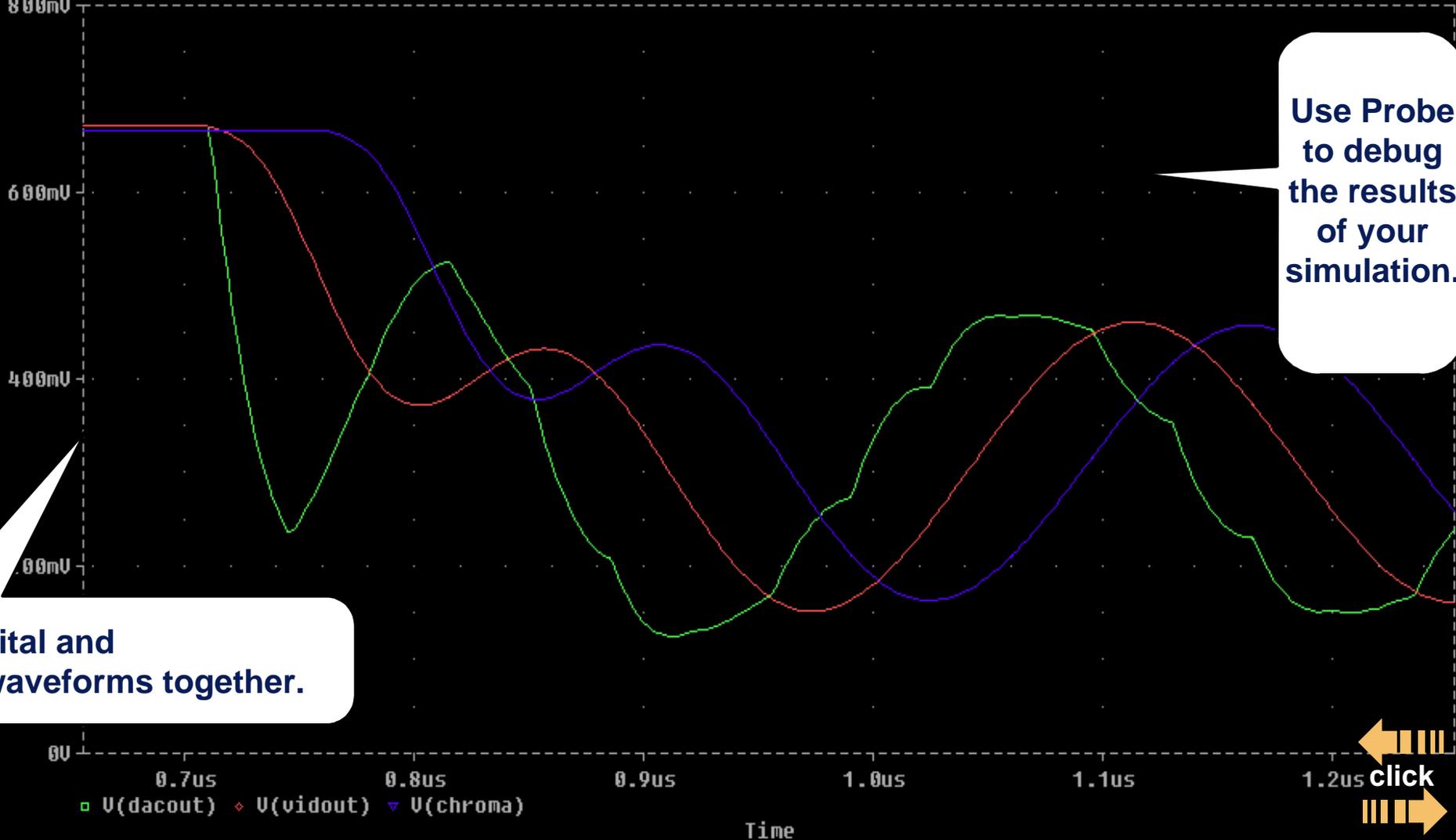
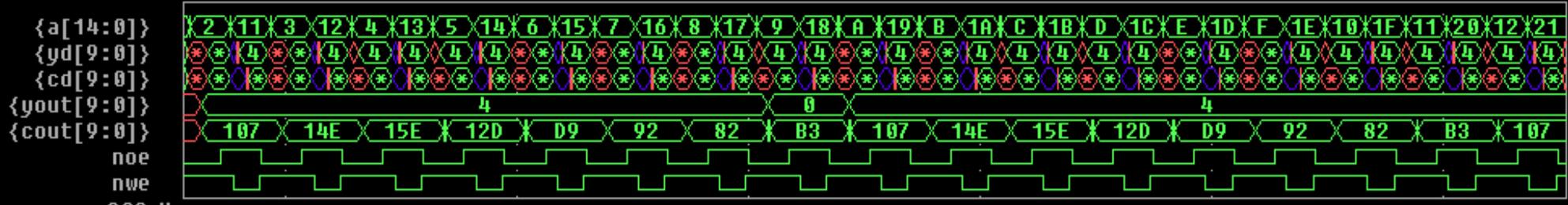
Device Name	Mfg.	Fam.	Pkg.	Temp.	Icc	Tmin	Price	U1	U2
PALCE16V8-25JC	CYP	CMOS	JLCC	COM	90ma	27ns	\$0.65	0	0
PALCE16V8-25PC	CYP	CMOS	DIP	COM	55ma	27ns	\$0.65	0	0
PALCE16V8-15PC	CYP	CMOS	DIP	COM	90ma	22ns	\$0.70	0	0
PALCE16V8-15JC	CYP	CMOS	JLCC	COM	90ma	22ns	\$0.75	0	0
PALCE16V8L-25JC	CYP	CMOS	JLCC	COM	55ma	22ns	\$0.75	0	0
PALCE16V8-25PI	CYP	CMOS	DIP	EXT	130ma	27ns	\$0.80	0	0
PALCE16V8-25JI	CYP	CMOS	JLCC	EXT	130ma	27ns	\$0.85	0	0
PALCE16V8-15PI	CYP	CMOS	DIP	EXT	130ma	22ns	\$0.95	0	0
PALCE16V8H-25JC/4	AMD	CMOS	JLCC	COM	90ma	27ns	\$0.98	0	0
PALCE16V8H-25PC/4	AMD	CMOS	DIP	COM	90ma	27ns	\$0.98	0	0
ATF16V8B-15JC	ATM	CMOS	JLCC	COM	115ma	21ns	\$1.00	0	0

OK Cancel Help

Select the part(s) to use for the chosen solution.



Functional & Timing Simulation



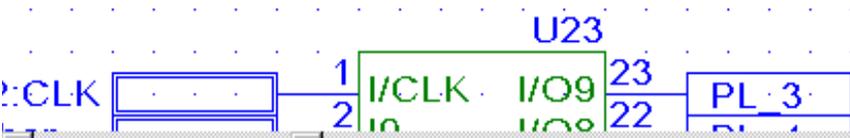
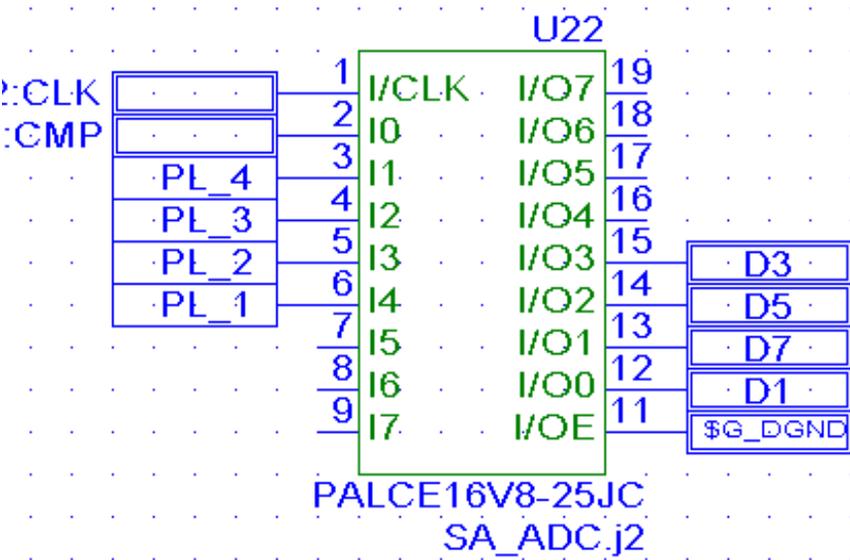
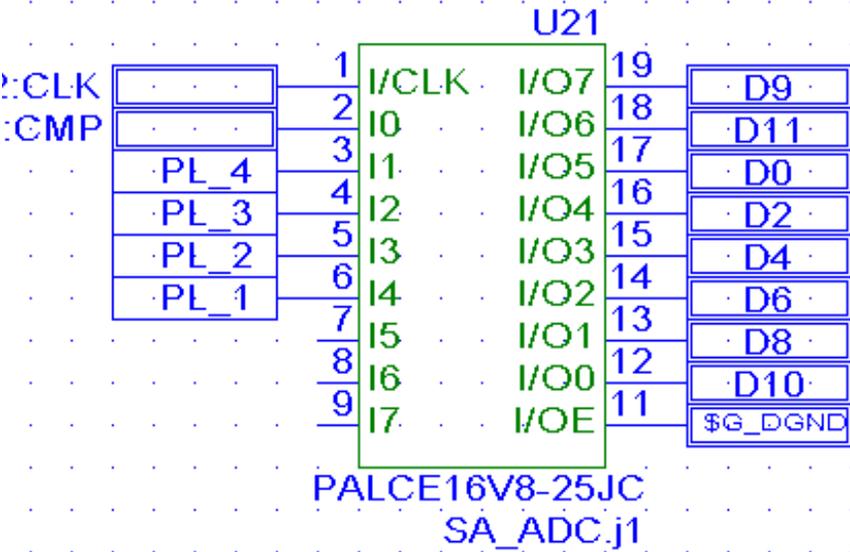
Use Probe to debug the results of your simulation.

View digital and analog waveforms together.

click

0.7us 0.8us 0.9us 1.0us 1.1us 1.2us
□ U(dacout) ♦ U(vidout) ▼ U(chroma)

Time



Preparing for PCB Layout

Use PLSyn to update the schematic with the selected part(s).

When you create the PCB netlist for the system, the PLDs/CPLDs will be included.



MicroSim PLSyn

Lets you bring accurate circuits to market faster!

- Only PC-based tool that integrates PLDs and CPLDs with analog and discrete digital devices in a complete system design.
- Creates a list of device solutions to your logic design; so you can select the best solution.
- Integrated simulation—functional and timing analysis are accessed through Schematics.