What Is MicroSim PLSyn?

- Used to design PLDs (Programmable Logic Devices) and CPLDs (Complex PLDs).
- Works with MicroSim Schematics and MicroSim PSpice A/D.
- Includes a part library with up to 3,500 PLDs and CPLDs from 12 manufacturers: Altera, AMD, Atmel, Cypress, ICT, Lattice, and more!
- Allows mixed-mode (schematic and language) design entry.
- Automatically partitions your design into multiple devices (with the PLSyn Partitioning option).
- Only PC-based tool that can integrate PLDs and CPLDs into your overall mixed analog/digital system design.

MicroSim®

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Why Use MicroSim PLSyn?

- ***Create*** integrated designs combining PLDs and CPLDs with analog and discrete digital devices.
- ***Generate*** a list of device solutions that meet your design specifications; you then select the configuration that best fits your design.
- ***Perform*** functional simulation (before fitting and part selection).
- ***Perform*** timing simulation (after part selection).
- ***Generate*** fuse map files.

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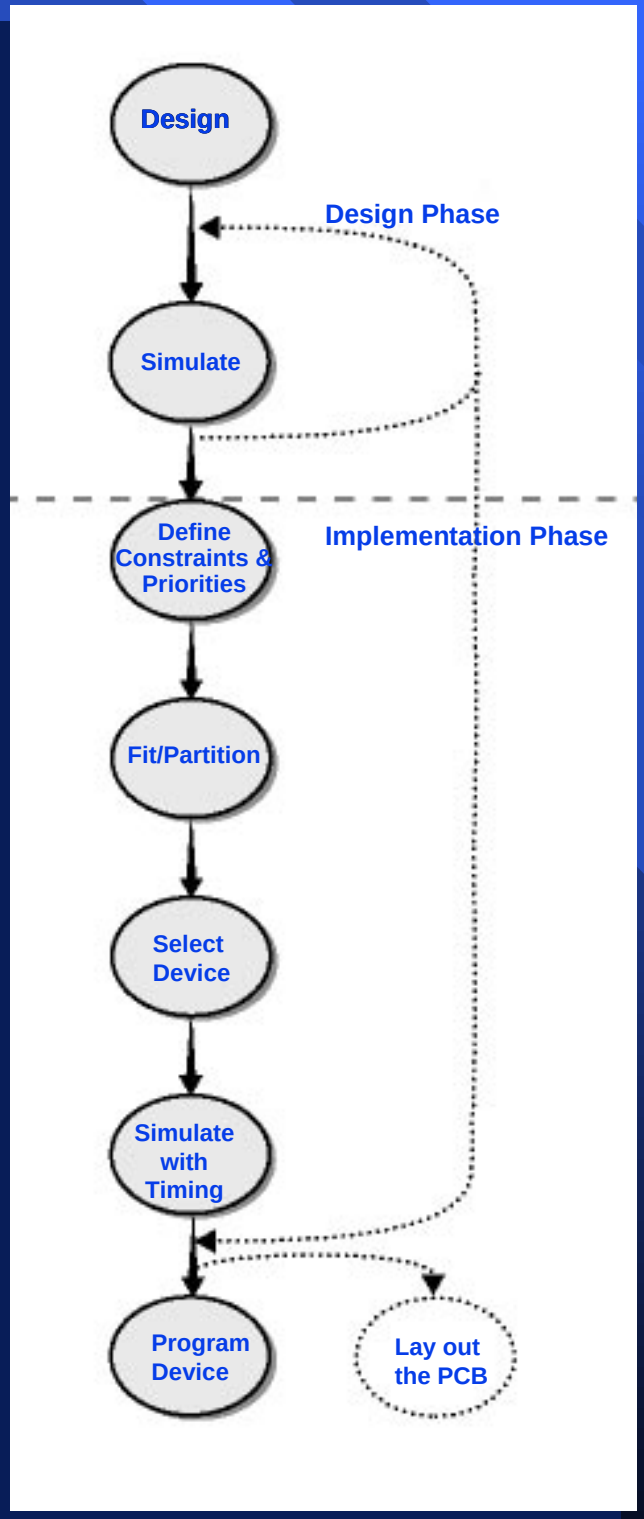
Using MicroSim PLSyn



1. Enter your design in Schematics.
2. Perform functional simulation, and analyze simulation results in Probe.
3. Set device constraints and priorities.
4. Run the PLSyn fitter to create a list of device solutions; solutions can be a single device or multiple devices (with the Partitioning option).
5. Select a solution to implement your design.
6. Perform timing simulation, and analyze simulation results in Probe.
7. Generate fuse maps to program the PLDs and/or CPLDs in your design.

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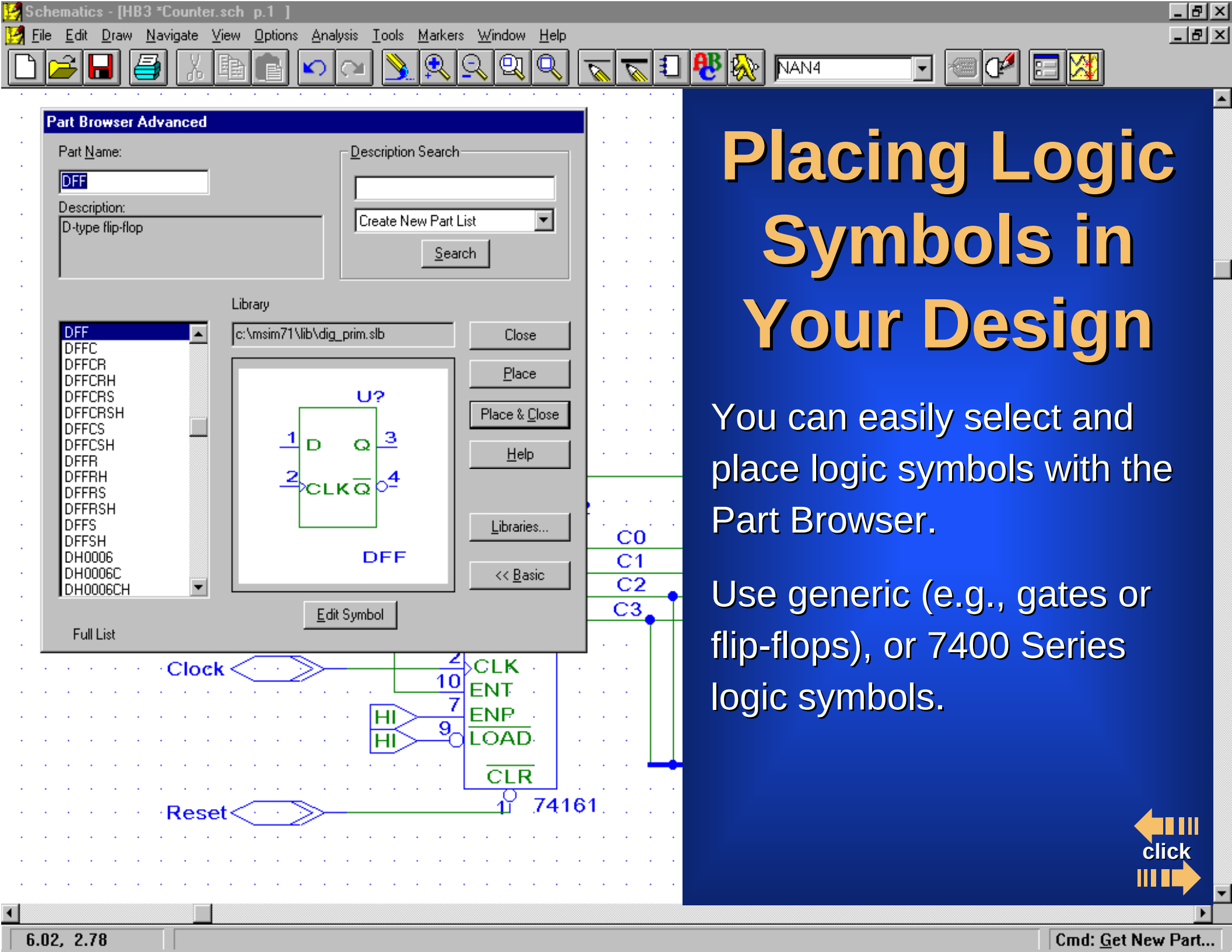

Placing Logic Symbols in Your Design

You can easily select and place logic symbols with the Part Browser.

Use generic (e.g., gates or flip-flops), or 7400 Series logic symbols.

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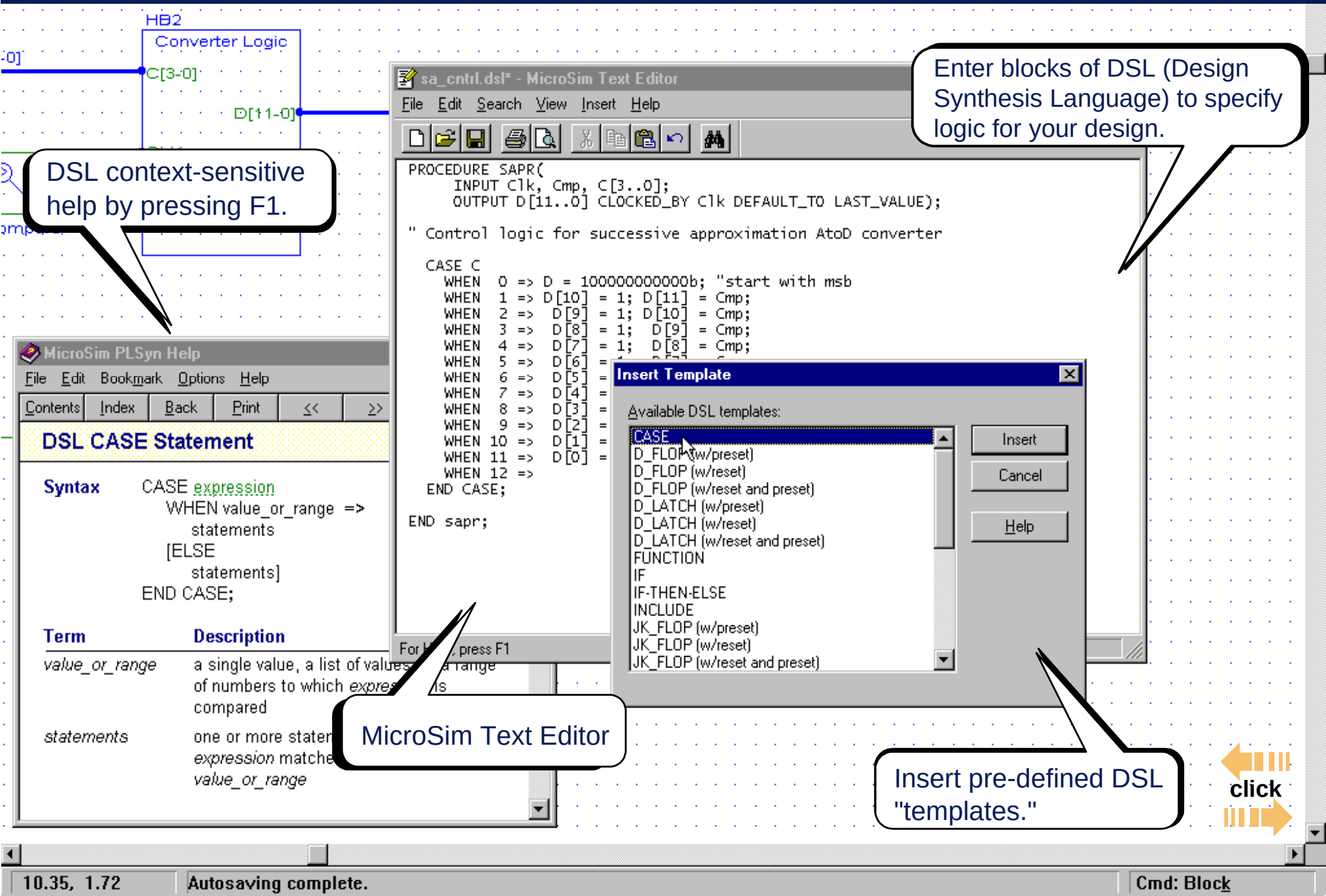
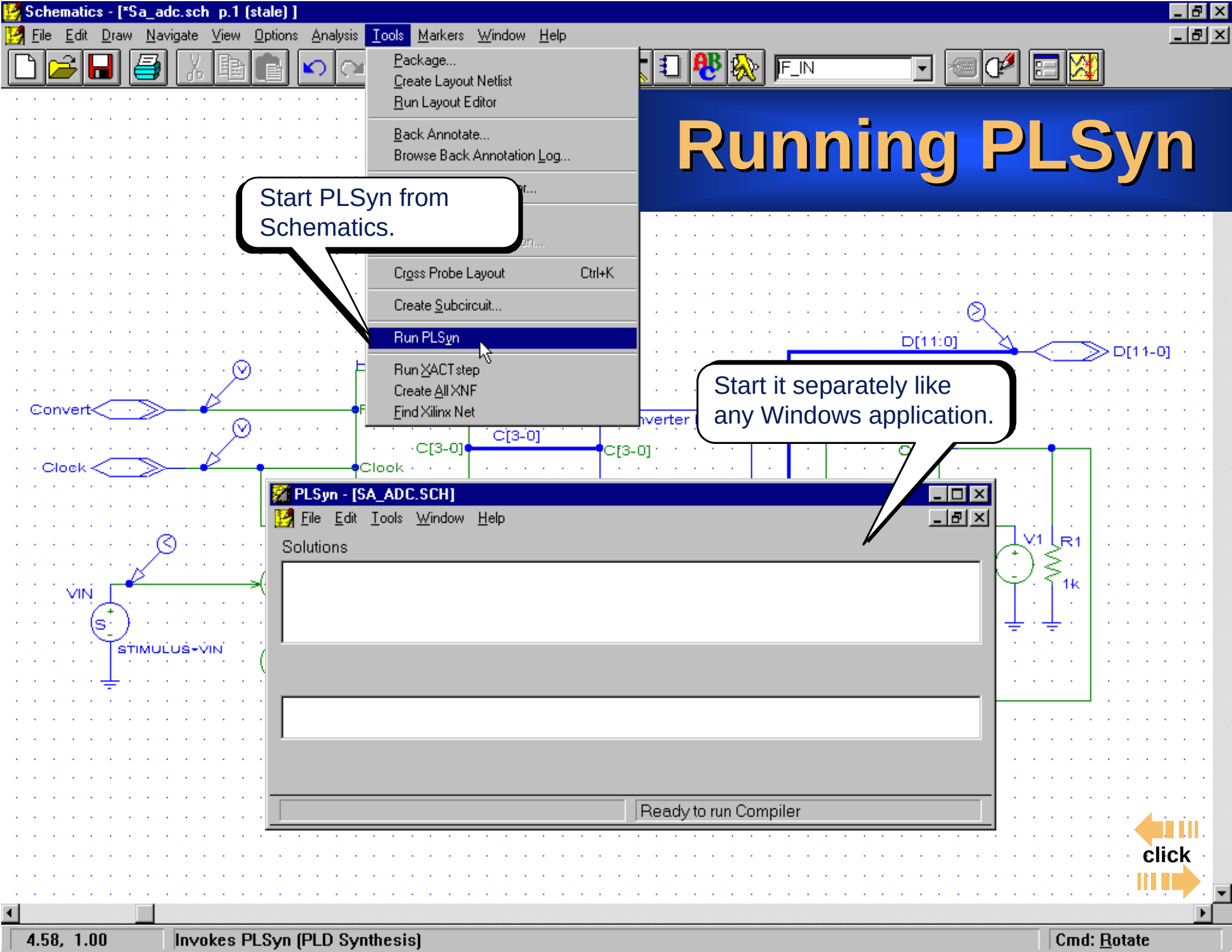
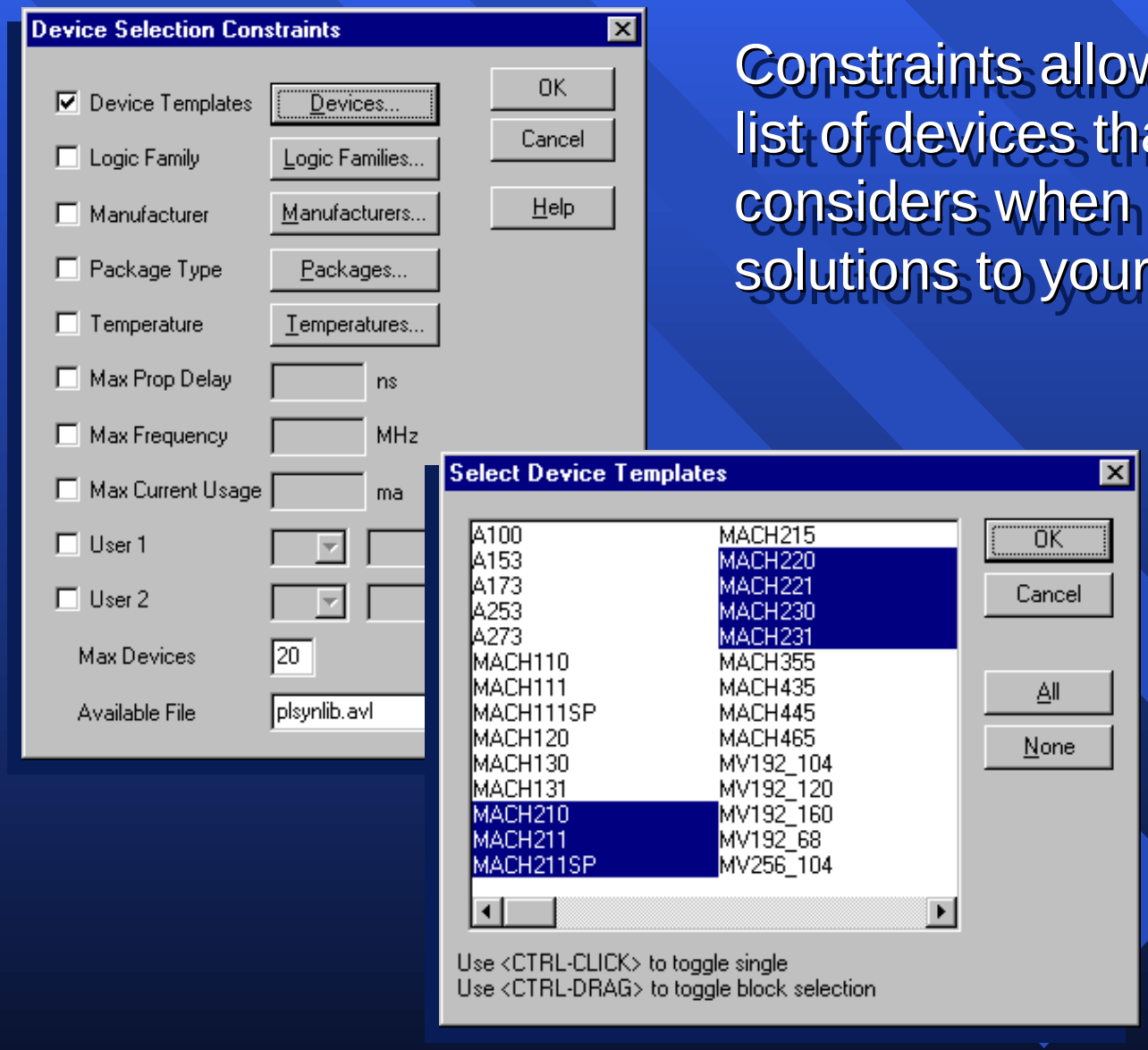
Placing DSL Blocks in Your Design




Schematics - [*Sa_adc.sch p.1 (stale)]
File Edit Draw Navigate View Options Analysis Tools Markers Window Help
Package...
Create Layout Netlist
Run Layout Editor
Back Annotate...
Browse Back Annotation Log...
Cross Probe Layout Ctrl+K
Create Subcircuit...
Run PLSyn
Run XACTstep
Create All XNF
Find Xilinx Net
F_IN
Running PLSyn
Start PLSyn from Schematics.
Start it separately like any Windows application.
D[11:0]
Convert
Clock
C[3-0]
VIN
STIMULUS-VIN
V1
R1
1k
PLSyn - [SA_ADC.SCH]
File Edit Tools Window Help
Solutions
Ready to run Compiler
click
4.58, 1.00
Invokes PLSyn (PLD Synthesis)
Cmd: Rotate

Setting Constraints



Constraints allow you to narrow the list of devices that the PLSyn fitter considers when searching for solutions to your logic design.

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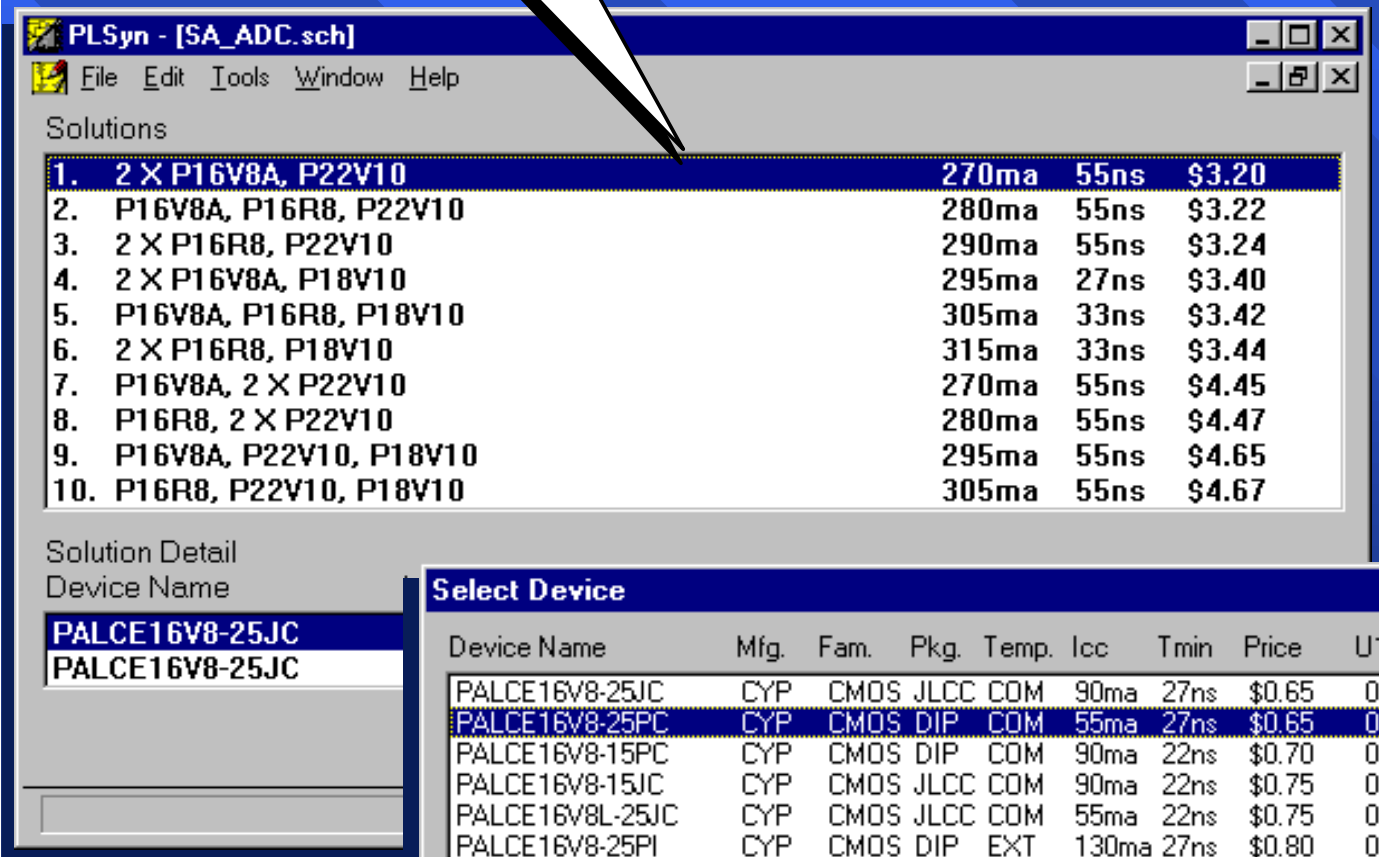
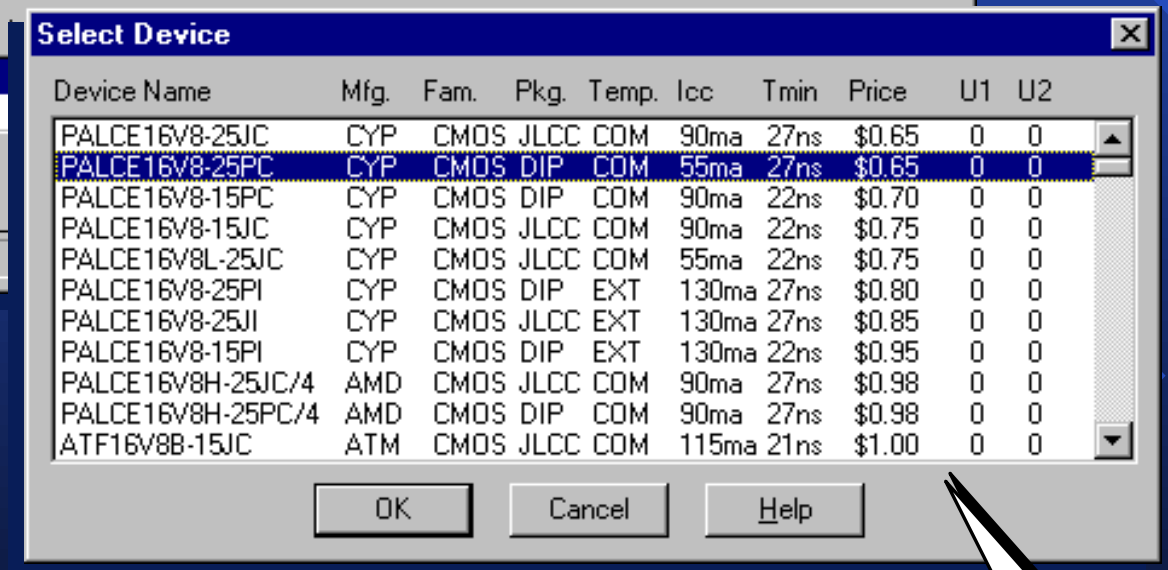
Fitting the Logic

Select the solution that best meets your requirements.





Run the PLSyn Fitter to find solutions based on your constraints. Solutions can be a single device or multiple devices with the same or different architectures.

Select the part(s) to use for the chosen solution.

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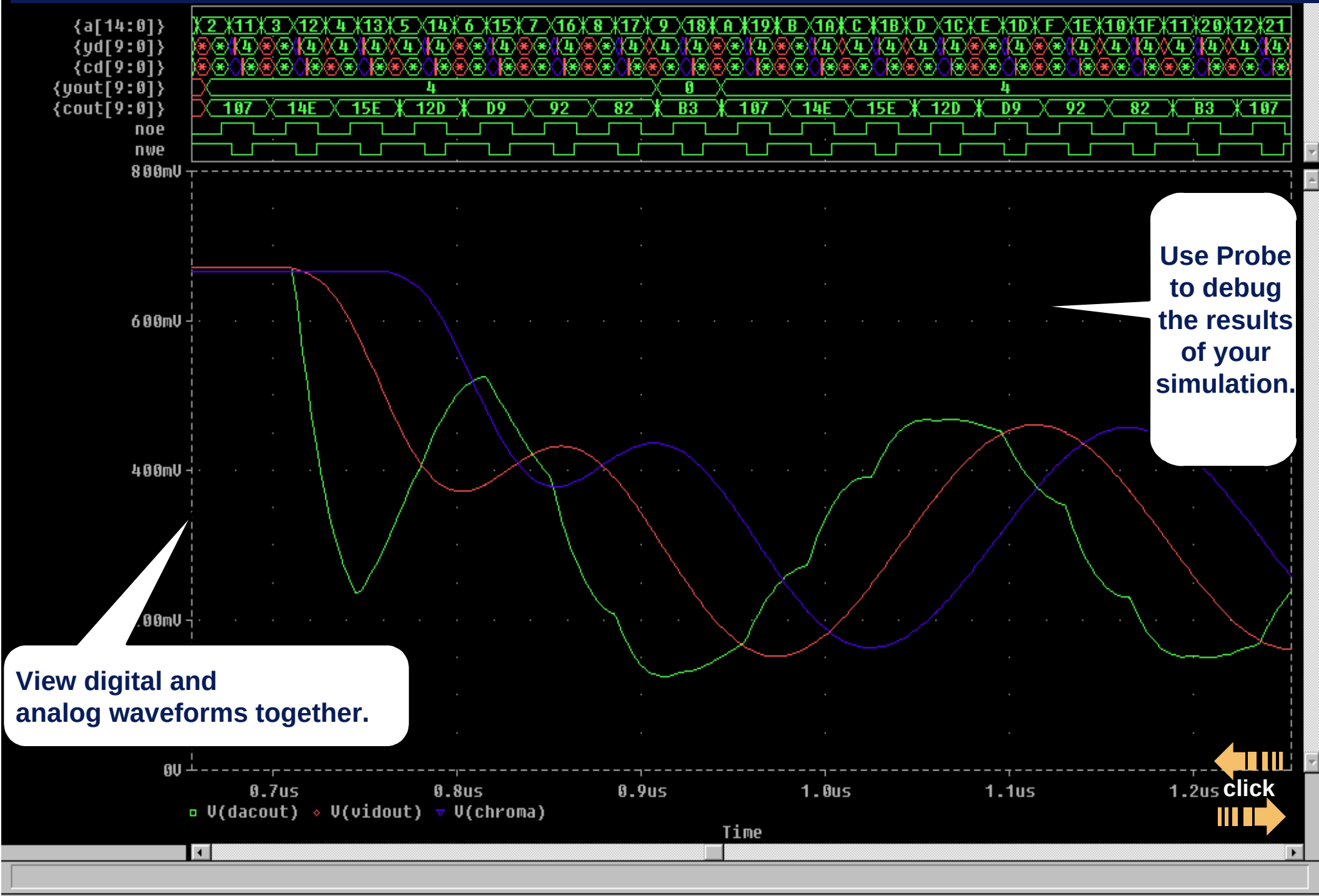
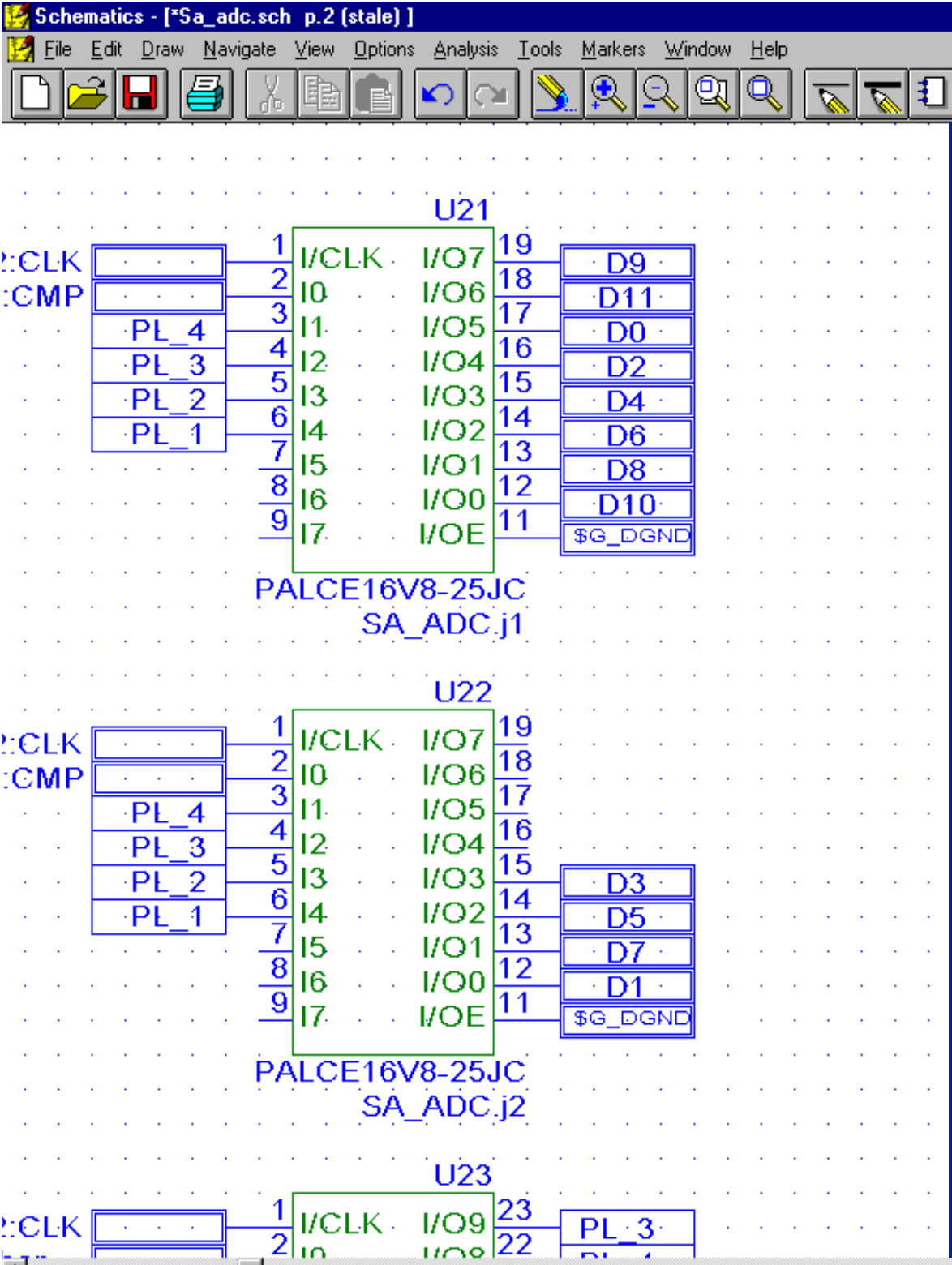
Functional & Timing Simulation





Preparing for PCB Layout

Use PLSyn to update the schematic with the selected part(s).

When you create the PCB netlist for the system, the PLDs/CPLDs will be included.

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MicroSim PLSyn

Lets you bring accurate circuits to market faster!

- Only PC-based tool that integrates PLDs and CPLDs with analog and discrete digital devices in a complete system design.
- Creates a list of device solutions to your logic design; so you can select the best solution.
- Integrated simulation–functional and timing analysis are accessed through Schematics.

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Press Esc to return to the Acrobat Reader.