Introduction

The proliferation of I/O standards and the need for improved I/O performance have made it critical that low-cost devices have flexible I/O capabilities. Selectable I/O capabilities such as SSTL-2, SSTL-3, and LVDS compatibility allow Cyclone™ devices to connect to other devices on the same printed circuit board (PCB) that may require different operating and I/O voltages. With these aspects of implementation easily manipulated using the Altera® Quartus® II software, the Cyclone device family enables system designers to use low-cost FPGAs while keeping pace with increasing design complexity.

This application note is a guide to understanding the input/output capabilities of the Cyclone devices, including:

- Supported I/O standards
- I/O banks
- Programmable current drive strength
- Hot socketing
- Termination guidelines
- Pad placement and DC guidelines

In addition, “Quartus II Software Support” on page 16 describes how to use the Quartus II software to specify device and pin options and assign pins to implement the above features of Cyclone devices.

Supported I/O Standards

Cyclone devices support the I/O standards shown in Table 1.

See the Cyclone FPGA Family Data Sheet for more details on the I/O Standards discussed in this section.
Table 1. I/O Standards Supported by Cyclone Devices

<table>
<thead>
<tr>
<th>I/O Standard</th>
<th>Type</th>
<th>Input Voltage Level (v)</th>
<th>Output Voltage Level (V)</th>
<th>Input VREF (V)</th>
<th>Output VCCIO (V)</th>
<th>Termination VTT (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.3V LVTTL/LVCMOS</td>
<td>Single-ended</td>
<td>3.3/2.5</td>
<td>3.3</td>
<td>N/A</td>
<td>3.3</td>
<td>N/A</td>
</tr>
<tr>
<td>2.5V LVTTL/LVCMOS</td>
<td>Single-ended</td>
<td>3.3/2.5</td>
<td>2.5</td>
<td>N/A</td>
<td>2.5</td>
<td>N/A</td>
</tr>
<tr>
<td>1.8V LVTTL/LVCMOS</td>
<td>Single-ended</td>
<td>3.3/2.5/1.8</td>
<td>1.8</td>
<td>N/A</td>
<td>1.8</td>
<td>N/A</td>
</tr>
<tr>
<td>1.5V LVCMOS</td>
<td>Single-ended</td>
<td>3.3/2.5/1.8/1.5</td>
<td>1.5</td>
<td>N/A</td>
<td>1.5</td>
<td>N/A</td>
</tr>
<tr>
<td>PCI</td>
<td>Single-ended</td>
<td>3.3</td>
<td>3.3</td>
<td>N/A</td>
<td>3.3</td>
<td>N/A</td>
</tr>
<tr>
<td>SSTL-3 Class I and II</td>
<td>Voltage-referenced</td>
<td>-0.3 to 3.9</td>
<td>3.3</td>
<td>1.5</td>
<td>3.3</td>
<td>1.5</td>
</tr>
<tr>
<td>SSTL-2 Class I and II</td>
<td>Voltage-referenced</td>
<td>-0.3 to 3.0</td>
<td>2.5</td>
<td>1.25</td>
<td>2.5</td>
<td>1.25</td>
</tr>
<tr>
<td>LVDS Compatibility</td>
<td>Differential</td>
<td>0 to 2.4</td>
<td>VOD = 0.25 to 0.55</td>
<td>N/A</td>
<td>2.5</td>
<td>N/A</td>
</tr>
</tbody>
</table>

Notes to Table 1:
(1) The EP1C3 device in the 100-pin thin quad flat pack (TQFP) package does not have support for a PLL LVDS input or an external clock output.
(2) Cyclone devices have dual-purpose differential inputs. Outputs are balanced SSTL outputs requiring an external resistor divider.

3.3-V LVTTL (EIA/JEDEC Standard JESD8-B)

The 3.3-V LVTTL I/O standard is a general-purpose, single-ended standard used for 3.3-V applications. The LVTTL standard defines the DC interface parameters for digital circuits operating from a 3.0-V/3.3-V power supply and driving or being driven by LVTTL-compatible devices.

The LVTTL input standard specifies a wider input voltage range of -0.3 V <= V1 <= 3.9 V. Altera recommends an input voltage range of -0.5 V <= V1 <= 4.1 V. The LVTTL standard does not require input reference voltages or board terminations. Cyclone devices support both input and output levels for 3.3V LVTTL.
3.3-V LVCMOS (EIA/JEDEC Standard JESD8-B)

The 3.3-V LVCMOS I/O standard is a general-purpose, single-ended standard used for 3.3-V applications. The LVCMOS standard defines the DC interface parameters for digital circuits operating from a 3.0-V or 3.3-V power supply and driving or being driven by LVCMOS-compatible devices.

The LVCMOS standard specifies the same input voltage requirements as LVTTL (-0.3 V <= VI <= 3.9 V). The output buffer drives to the rail to meet the minimum high-level output voltage requirements. The 3.3-V I/O Standard does not require input reference voltages or board terminations. Cyclone devices support both input and output levels specified by the 3.3V LVCMOS I/O standard.

2.5-V LVTTL Normal & Wide Voltage Ranges (EIA/JEDEC Standard EIA/JESD8-5)

The 2.5-V I/O standard is used for 2.5-V LVTTL applications. This standard defines the DC interface parameters for high-speed, low-voltage, non-terminated digital circuits driving or being driven by other 2.5-V devices. The input and output voltage requirements are:

- The 2.5-V normal and wide range input standards specify an input voltage range of -0.3 V <= VI <= 3.0 V.
- The normal range minimum high-level output voltage requirement (VOH) is 2.1 V.
- The wide range minimum high-level output voltage requirement (VOH) is VCCIO - 0.2 V.

The 2.5-V standard does not require input reference voltages or board terminations. Cyclone devices support input and output levels for both 2.5-V LVTTL ranges.

2.5-V LVCMOS Normal & Wide Voltage Ranges (EIA/JEDEC Standard EIA/JESD8-5)

The 2.5-V I/O standard is used for 2.5-V LVCMOS applications. This standard defines the DC interface parameters for high-speed, low-voltage, non-terminated digital circuits driving or being driven by other 2.5-V parts. The input and output voltage ranges are:

- The 2.5-V normal and wide range input standards specify an input voltage range of -0.3 V <= VI <= 3.0 V.
- The normal range minimum VOH requirement is 2.1 V.
- The wide range minimum VOH requirement is VCCIO - 0.2 V.
The 2.5-V standard does not require input reference voltages or board terminations. Cyclone devices support input and output levels for both 2.5-V LVCMOS ranges.

**1.8-V LVCMOS Normal & Wide Voltage Ranges (EIA/JEDEC Standard EIA/JESD8-7)**

The 1.8-V I/O standard is used for 1.8-V LVCMOS applications. This standard defines the DC interface parameters for high-speed, low-voltage, non-terminated digital circuits driving or being driven by other 1.8-V devices. The input and output voltage ranges are:

- The 1.8-V normal and wide range input standards specify an input voltage range of \(-0.3 \text{ V} \leq V_I \leq 2.25 \text{ V}\).
- The normal range minimum $V_{OH}$ requirement is $V_{CCIO} - 0.45 \text{ V}$.
- The wide range minimum $V_{OH}$ requirement is $V_{CCIO} - 0.2 \text{ V}$.

The 1.8-V standard does not require input reference voltages or board terminations. Cyclone devices support input and output levels for both normal and wide 1.8-V LVCMOS ranges.

**1.5-V LVCMOS Normal & Wide Voltage Ranges (EIA/JEDEC Standard JESD8-11)**

The 1.5-V I/O standard is used for 1.5-V applications. This standard defines the DC interface parameters for high-speed, low-voltage, non-terminated digital circuits driving or being driven by other 1.5-V devices. The input and output voltage ranges are:
The 1.5-V normal and wide range input standards specify an input voltage range of -0.3 V ≤ Vᵢ ≤ 1.9 V.
- The normal range minimum VₒH requirement is 1.05 V.
- The wide range minimum VₒH requirement is Vᵦ – 0.2 V.

The 1.5-V standard does not require input reference voltages or board terminations. Cyclone devices support input and output levels for both normal and wide 1.5-V LVCMOS ranges.

3.3-V (PCI Special Interest Group (SIG) PCI Local Bus Specification Revision 2.2)

The PCI local bus specification is used for applications that interface to the PCI local bus, which provides a processor-independent data path between highly integrated peripheral controller components, peripheral add-in boards, and processor/memory systems. The conventional PCI specification revision 2.2 defines the PCI hardware environment including the protocol, electrical, mechanical, and configuration specifications for the PCI devices and expansion boards. This standard requires 3.3-V Vᵦ. The 3.3-V PCI standard does not require input reference voltages or board terminations.

Although PCI is not supported on the smallest member of the Cyclone device family, the EP1C3, all other Cyclone devices are fully compliant with the 3.3-V PCI Local Bus Specification Revision 2.2 and meet 32-bit/66-MHz operating frequency and timing requirements. The devices support PCI input and output levels on I/O banks 1 and 3 only. See “Cyclone I/O Banks” on page 7 for more details.

SSTL-3 Class I & II (EIA/JEDEC Standard JESD8-8)

The SSTL-3 I/O standard is a 3.3-V memory bus standard used for applications such as high-speed SDRAM interfaces. This standard defines the input and output specifications for devices that operate in the SSTL-3 logic switching range of 0.0 to 3.3 V. The SSTL-3 standard specifies an input voltage range of -0.3 V ≤ Vᵢ ≤ Vᵦ + 0.3 V. SSTL-3 requires a 1.5-V Vᵦ and a 1.5-V Vᵦ to which the series and termination resistors are connected (see Figures 1 and 2). In typical applications, both the termination voltage and reference voltage track the output supply voltage.
Cyclone devices support both input and output SSTL-3 Class I & II levels.

**SSTL-2 Class I & II (EIA/JEDEC Standard JESD8-9A)**

The SSTL-2 I/O standard is a 2.5-V memory bus standard used for applications such as high-speed double data rate (DDR) SDRAM interfaces. This standard defines the input and output specifications for devices that operate in the SSTL-2 logic switching range of 0.0 V to 2.5 V. This standard improves operation in conditions where a bus must be isolated from large stubs. The SSTL-2 standard specifies an input voltage range of \(-0.3 \leq V_I \leq V_{CCIO} + 0.3\) V. SSTL-2 requires a \(V_{REF}\) value of 1.25 V and a \(V_{TT}\) value of 1.25 V connected to the series and termination resistors (see Figures 3 and 4).
Cyclone devices support both input and output SSTL-2 Class I & II levels.

**LVDS (ANSI/TIA/EIA Standard ANSI/TIA/EIA-644)**

The LVDS I/O standard is a differential high-speed, low-voltage swing, low-power, general-purpose I/O interface standard. This standard is used in applications requiring high-bandwidth data transfer, backplane drivers, and clock distribution. The ANSI/TIA/EIA-644 standard specifies LVDS transmitters and receivers capable of operating at recommended maximum data signaling rates of 655 Mbps. Devices can operate at slower speeds if needed however, and there is a theoretical maximum of 1.923 Gbps. Due to the low-voltage swing of the LVDS I/O standard, the electromagnetic interference (EMI) effects are much smaller than CMOS, TTL, and PECL. This low EMI makes LVDS ideal for applications with low EMI requirements or noise immunity requirements. The LVDS standard specifies a differential output voltage range of 250 mV ≤ VOD ≤ 550 mV.

The Cyclone device family meets the ANSI/TIA/EIA-644 standard and is LVDS-compatible but, unlike previous products with LVDS support, Cyclone does not have dedicated SERDES or LVDS drivers. While external resistors are required for LVDS output support, Cyclone does have direct LVDS-compatible input support throughout the chip. This flexible approach to LVDS support allows LVDS compatibility on every bank of the Cyclone chip at speeds up to 311Mbps. (Contact Altera Applications for the latest LVDS specification).

See the *Cyclone FPGA Family Data Sheet* for more details on the I/O Standards discussed in this section.

**Cyclone I/O Banks**

The I/O pins on Cyclone devices are grouped together into I/O banks and each bank has a separate power bus. This permits designers to select the preferred I/O standard for a given bank enabling tremendous flexibility in the Cyclone device’s I/O support.
Each Cyclone device supports four I/O banks regardless of density. Similarly, each device I/O pin is associated with one of these specific, numbered I/O banks. To accommodate voltage-referenced I/O standards, each Cyclone I/O bank has a common $V_{\text{REF}}$ bus and each bank supports 3 $V_{\text{REF}}$ pins (see Figure 5). In the event these pins are not used as $V_{\text{REF}}$ pins, they may be used as regular I/O pins.

**Figure 5. Cyclone Power Bank & $V_{\text{REF}}$ Arrangement**
Additionally, each Cyclone I/O bank has its own VCCIO pins. Any single I/O bank must have only one VCCIO setting from among 1.5, 1.8, 2.5 or 3.3 V. Although there can only be one VCCIO voltage, Cyclone devices permit additional input signaling capabilities as shown in Table 2.

<table>
<thead>
<tr>
<th>Bank VCCIO</th>
<th>Acceptable Input Levels</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.3-V</td>
<td>✓</td>
</tr>
<tr>
<td>2.5-V</td>
<td>✓ ✓</td>
</tr>
<tr>
<td>1.8-V</td>
<td>✓ ✓ ✓</td>
</tr>
<tr>
<td>1.5-V</td>
<td>✓ ✓ ✓ ✓</td>
</tr>
</tbody>
</table>

For more information on acceptable input levels, see *AN 258: Using Cyclone Devices in Multi-Voltage Systems*.

Any number of supported single-ended or differential standards can be simultaneously supported in a single I/O bank as long as they use compatible VCCIO levels for input and output pins. For example, an I/O bank with a 2.5-V VCCIO setting can support 2.5-V LVTTL inputs and outputs, 2.5-V LVDS-compatible inputs and outputs, and 3.3-V LVCMOS inputs only.

Voltage-referenced standards can be supported in an I/O bank using any number of single-ended or differential standards as long as they use the same VREF and a compatible VCCIO value. For example, if you choose to implement both SSTL-3 and SSTL-2 in your Cyclone device, I/O pins using these standards—because they require different VREF values—must be in different banks from each other. However, SSTL-3 and 3.3-V LVCMOS could be supported in the same bank with the VCCIO set to 3.3 V and the VREF set to 1.5 V.

See “Pad Placement & DC Guidelines” on page 12 for more information.

All four I/O banks support all of the I/O standards with the exception of PCI, which is only supported on banks 1 and 3 (see Figure 6).
Programmable Current Drive Strength

The Cyclone device I/O standards support various output current drive settings as shown in Table 3. These programmable drive-strength settings are a valuable tool in helping decrease the effects of simultaneously switching outputs (SSO) in conjunction with reducing system noise. The supported settings ensure that the device driver meets the specifications for $I_{OH}$ and $I_{OL}$ of the corresponding I/O standard.

<table>
<thead>
<tr>
<th>I/O Standard</th>
<th>$I_{OH}/I_{OL}$ Current Strength Setting</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.3-V LVTTL</td>
<td>24, 16, 12, 8, 4 mA</td>
</tr>
<tr>
<td>3.3-V LVC莫斯</td>
<td>12, 8, 4, 2 mA</td>
</tr>
<tr>
<td>2.5-V LVTTL/LVCmos</td>
<td>16, 12, 8, 2 mA</td>
</tr>
<tr>
<td>1.8-V LVTTL/LVCmos</td>
<td>12, 8, 2 mA</td>
</tr>
<tr>
<td>1.5-V LVCmos</td>
<td>8, 4, 2 mA</td>
</tr>
<tr>
<td>SSTL-3 class I and II</td>
<td>Min. Strength</td>
</tr>
<tr>
<td>SSTL-2 class I and II</td>
<td>Min. Strength</td>
</tr>
</tbody>
</table>
These drive-strength settings are programmable on a per-pin basis (for output and bidirectional pins only) using the Quartus II software. To modify the current strength of a particular pin, see “Programmable Drive Strength Settings” on page 18.

**Hot Socketing**

Cyclone devices support any power-up or power-down sequence (VCCIO and VCCINT) to facilitate hot socketing. You can drive signals into the device before or during power-up or power-down without damaging the device. Cyclone devices will not drive out until the device is configured and has attained proper operating conditions.

You can power up or power down the VCCIO and VCCINT pins in any sequence. The power supply ramp rates can range from 100 ns to 100 ms and I/O pins can be driven by active signals with rise/fall times of 2 ns to 40 ns. Additionally, during power-up, the I/O pin capacitance is less than 15 pF and the clock pin capacitance is less than 20 pF.

- The hot socketing DC specification is $|I_{O\text{PIN}}| < 300 \mu\text{A}$.
- The hot socketing AC specification is $|I_{O\text{PIN}}| < 8 \text{ mA}$ for 10 ns or less.

**I/O Termination**

The majority of the Cyclone I/O standards are single-ended, non-voltage-referenced I/O standards and, as such, the following I/O standards do not specify a recommended termination scheme:

- 3.3 V LVTTL / LVCMOS
- 2.5 V LVTTL / LVCMOS
- 1.8 V LVTTL / LVCMOS
- 1.5 V LVCMOS
- 3.3-V PCI

The Cyclone device family does not feature on-chip I/O termination resistors.

**Voltage-Referenced I/O Standard Termination**

Voltage-referenced I/O standards require both an input reference voltage, $V_{REF}$, and a termination voltage, $V_{TT}$. The reference voltage of the receiving device tracks the termination voltage of the transmitting device.

For more information on termination for voltage-referenced I/O standards, see “Supported I/O Standards” on page 1.
Differential I/O Standard Termination

Differential I/O standards typically require a termination resistor between the two signals at the receiver. The termination resistor must match the differential load impedance of the bus.

LVDS is the only differential I/O standard supported by Cyclone devices. For information on LVDS termination, contact Altera Applications.

Pad Placement & DC Guidelines

This section provides pad placement guidelines for the programmable I/O standards supported by Cyclone devices and includes essential information for designing systems using the devices’ selectable I/O capabilities. This section also discusses the DC limitations and guidelines.

Differential Pad Placement Guidelines

In order to maintain an acceptable noise level on the VCCIO supply, there are restrictions on placement of single-ended I/O pads in relation to differential pads. Use the following guidelines for placing single-ended pads with respect to differential pads in Cyclone devices.

- Single-ended inputs may be only be placed four or more pads away from a differential pad.
- Single-ended outputs and bidirectional pads may only be placed five or more pads away from a differential pad.

The Quartus II software generates an error message for illegally placed pads.

VREF Pad Placement Guidelines

In order to maintain an acceptable noise level on the VCCIO supply and to prevent output switching noise from shifting the VREF rail, there are restrictions on the placement of single-ended voltage referenced I/Os with respect to VREF pads and VCCIO/GND pairs. Please use the following guidelines for placing single-ended pads in Cyclone devices.

Input Pads

Each VREF pad supports a maximum of 40 input pads with up to 20 on each side of the VREF pad. This is irrespective of VCCIO/GND pairs.
Output Pads

When a voltage referenced input or bidirectional pad does not exist in a bank, there is no limit to the number of output pads that can be implemented in that bank. When a voltage referenced input exists, each VCCIO/GND pair supports 9 outputs for Fineline BGA packages or 4 outputs for quad flat pack (QFP) packages. Any output pads must be placed greater than 2 pads away from your VREF pad to maintain acceptable noise levels.

Bidirectional Pads

Bidirectional pads must satisfy input and output guidelines simultaneously. If the bidirectional pads are all controlled by the same OE and there are no other outputs or voltage referenced inputs in the bank, then there is no case where there is a voltage referenced input active at the same time as an output. Therefore, the output limitation does not apply. However, since the bidirectional pads are linked to the same OE, the bidirectional pads will all act as inputs at the same time. Therefore, the input limitation of 40 input pads (20 on each side of your VREF pad) will apply.

If the bidirectional pads are all controlled by different output enables (OE) and there are no other outputs or voltage referenced inputs in the bank, then there may be a case where one group of bidirectional pads is acting as inputs while another group is acting as outputs. In such cases, apply the formulas shown in Table 4.

<table>
<thead>
<tr>
<th>Package Type</th>
<th>Formula</th>
</tr>
</thead>
<tbody>
<tr>
<td>FineLine BGA®</td>
<td>(Total number of bidirectional pads) - (Total number of pads from the smallest group of pads controlled by an OE) ≤ 9 (per VCCIO/GND pair)</td>
</tr>
<tr>
<td>QFP</td>
<td>(Total number of bidirectional pads) - (Total number of pads from the smallest group of pads controlled by an OE) ≤ 4 (per VCCIO/GND pair).</td>
</tr>
</tbody>
</table>

Consider an FineLine BGA package with 4 bidirectional pads controlled by OE1, 4 bidirectional pads controlled by OE2, and 2 bidirectional pads controlled by OE3. If OE1 and OE2 are active and OE3 is inactive, there are 10 bidirectional pads, but it is safely allowable because there would be 8 or fewer outputs per VCCIO/GND pair.
When at least one additional voltage referenced input and no other outputs exist in the same V_REF bank, the bidirectional pad limitation applies in addition to the input and output limitations. See the following equation.

\[(\text{Total number of bidirectional pads}) + (\text{Total number of input pads}) \leq 40 \text{ (20 on each side of your V_REF pad)}\]

The bidirectional pad limitation applies to both Fineline BGA packages and QFP packages.

After applying the equation above, apply one of the equations in Table 5, depending on package type.

<table>
<thead>
<tr>
<th>Package Type</th>
<th>Formula</th>
</tr>
</thead>
<tbody>
<tr>
<td>FineLine BGA</td>
<td>((\text{Total number of bidirectional pads}) \leq 9 \text{ (per VCCIO/GND pair)})</td>
</tr>
<tr>
<td>QFP</td>
<td>((\text{Total number of bidirectional pads}) \leq 4 \text{ (per VCCIO/GND pair)})</td>
</tr>
</tbody>
</table>

When at least one additional output exists but no voltage referenced inputs exist, apply the appropriate formula from Table 6.

<table>
<thead>
<tr>
<th>Package Type</th>
<th>Formula</th>
</tr>
</thead>
<tbody>
<tr>
<td>FineLine BGA</td>
<td>((\text{Total number of bidirectional pads}) + (\text{Total number of additional output pads}) - (\text{Total number of pads from the smallest group of pads controlled by an OE}) \leq 9 \text{ (per VCCIO/GND pair)})</td>
</tr>
<tr>
<td>QFP</td>
<td>((\text{Total number of bidirectional pads}) + (\text{Total number of additional output pads}) - (\text{Total number of pads from the VCCIO/GND pair}))</td>
</tr>
</tbody>
</table>

When additional voltage referenced inputs and other outputs exist in the same V_REF bank, then the bidirectional pad limitation must again simultaneously adhere to the input and output limitations. As such, the following rules apply:

\[\text{Total number of bidirectional pads} + \text{Total number of input pads} \leq 40 \text{ (20 on each side of your V_REF pad)}\]
The bidirectional pad limitation applies to both Fineline BGA packages and QFP packages.

After applying the equation above apply one of the equations in Table 7, depending on package type.

### Table 7. Bidirectional Pad Limitation Formulas (Multiple VREF Inputs & Outputs)

<table>
<thead>
<tr>
<th>Package Type</th>
<th>Formula</th>
</tr>
</thead>
<tbody>
<tr>
<td>FineLine BGA</td>
<td>((\text{Total number of bidirectional pads}) + (\text{Total number of output pads}) \leq 9 \text{ (per } \text{VCCIO} / \text{GND pair)})</td>
</tr>
<tr>
<td>QFP</td>
<td>(\text{Total number of bidirectional pads} + \text{Total number of output pads} \leq 4 \text{ (per } \text{VCCIO} / \text{GND pair)})</td>
</tr>
</tbody>
</table>

Each I/O bank can only be set to a single \(\text{V}_{\text{CCIO}}\) voltage level and a single \(\text{V}_{\text{REF}}\) voltage level at a given time. Pins of different I/O standards can share the bank if they have compatible \(\text{V}_{\text{CCIO}}\) values (see Table 2 on page 9 for more details).

In all cases listed above, the Quartus II software generates an error message for illegally placed pads.

### DC Guidelines

There is a current limit of 320 mA per 10 consecutive output pins, as shown by the following equation:

\[
\sum_{\text{pin}} i_{\text{pin}} < 320 \text{ mA}
\]
Table 8 shows the current allowed per pin by select I/O standards as measured under the standard’s defined loading conditions. PCI, LVTTL, LVC MOS, and other supported I/O standards not shown in the table do not have standardized loading conditions. As such, the current allowed per pin in a series-loaded condition for these standards is considered negligible.

<table>
<thead>
<tr>
<th>Pin I/O Standard</th>
<th>I Pin (mA)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>3.3-V $V_{CCIO}$</td>
</tr>
<tr>
<td>SSTL-3 Class I</td>
<td>8</td>
</tr>
<tr>
<td>SSTL-3 Class II</td>
<td>16</td>
</tr>
<tr>
<td>SSTL-2 Class I</td>
<td>N/A</td>
</tr>
<tr>
<td>SSTL-2 Class II</td>
<td>N/A</td>
</tr>
<tr>
<td>LVDS</td>
<td>N/A</td>
</tr>
</tbody>
</table>

Use the Quartus II software to specify which programmable I/O standards to use for Cyclone devices. This section describes Quartus II implementation, placement, and assignment guidelines, including:

- Compiler settings
- Device & pin options
- Assigning pins
- Programmable drive strength settings
- I/O banks in the floorplan view
- Auto placement & verification

**Compiler Settings**

The Compiler Settings dialog box (Processing menu) includes options allowing you to set a default I/O standard, optimize for I/O placement, assign I/O pins, and numerous other I/O-related options. The most pertinent user features are described in detail below.
Device & Pin Options

To access Device & Pin Options, choose Compiler Settings (Processing menu), then choose the Chips and Devices tab. There are numerous categories in the Device & Pin Options dialog box, including General, Configuration, Programming Files, Unused Pins, Dual-Purpose Pins, and Voltage. Similarly, each of these categories contains settings vital to the device operation such as the default I/O standard applied to the chip (Voltage tab), how to reserve all unused pins (Unused Pins tab), and whether or not the device should enable a device-wide reset (General tab).

Assigning Pins

Assuming a specific device has been chosen in the available devices list in the Compiler Settings dialog box, clicking Assign Pins provides the device’s pin settings and pin assignments (see Figure 7). You can view, add, remove and update pin settings under the Available Pins & Existing Assignments section within this window. The information for each pin includes:

- Number
- Name
- I/O bank
- I/O standard
- Type (e.g., row or column I/O and differential or control)
- SignalProbe Source Name
- Enabled (i.e., whether SignalProbe routing is enabled or disabled status)

Figure 7. Assign Pins
While assigned and unassigned pins are displayed in the Assign Pins dialog box, note that this listing does not include dedicated pins. Consult the device pin-out table for a complete listing of pins including dedicated pins.

When you assign an I/O standard that requires a reference voltage to an I/O pin, the Quartus II software automatically assigns \textit{VREF} pins. Refer to Quartus II Help for instructions on how to use an I/O standard for a pin.

\textbf{Programmable Drive Strength Settings}

To specify programmable drive strength settings, perform the following steps:

1. Choose \textit{Assignment Organizer} (Tools menu).
2. Choose the \textit{Edit specific entity & node settings for} setting, then select the output or bidirectional pin for which you will specify the current strength.
3. Select \textit{Options for Individual Nodes Only} in the Assignment Categories dialog box.
4. Select \textit{Click here to add a new assignment}.
5. In the Assignment dialog box, set the \textit{Name} field to \textit{Current Strength} then enter the desired value in the \textit{Setting} field.
6. Click \textit{Add}.
7. Click \textit{Apply} then \textit{OK}.

Note that the Quartus II software displays the entire range of drive strength choices. While the Quartus II software does not prohibit you from specifying any of these for your I/O pin, not every setting is supported by every I/O standard. Please refer to Table 3 on page 10 for supported combinations.

\textit{I/O Banks in the Floorplan View}

View the arrangement of the device I/O banks by choosing \textbf{Interior Cells} (View menu) with the Floorplan View displayed (see \textbf{Figure 8}). Pins that belong to the same I/O bank must use the same $V_{\text{CCIO}}$ voltage. You can assign multiple I/O standards to the I/O pins in any given I/O bank as long as the $V_{\text{CCIO}}$ voltage of the desired I/O standards is the same.
A given bank can have up to three $V_{\text{REF}}$ signals, and each signal can support one voltage-referenced I/O standard. Each device I/O pin belongs to a specific, numbered I/O bank. By default, the Show I/O Banks option is enabled, allowing the I/O banks to be displayed as color coded (See Figure 8).

**Figure 8. Floorplan View Window**

![Floorplan View Window](image)

**Auto Placement & Verification of Selectable I/O Standards**

The Quartus II software automatically verifies the placement for all I/O and $V_{\text{REF}}$ pins and performs the following actions:

- Automatically places I/O pins of different $V_{\text{REF}}$ standards without pin assignments in separate I/O banks and enables the $V_{\text{REF}}$ pins of these I/O banks.
- Verifies that voltage-referenced I/O pins requiring different $V_{\text{REF}}$ levels are not placed in the same bank.
- Reports an error message if the current limit is exceeded for a Cyclone power bank (See “DC Guidelines” on page 15).
- Automatically assigns $V_{\text{REF}}$ pins and I/O pins such that the current requirements are met and I/O standards are placed properly.
Conclusion

Cyclone device I/O capabilities enable system designers to keep pace with increasing design complexity utilizing a low-cost FPGA device family. Support for I/O standards including SSTL and LVDS compatibility allow Cyclone devices to fit into a wide variety of applications. The Quartus II software makes it easy to use these I/O standards in Cyclone device designs. After design compilation, the software also provides clear, visual representations of pads and pins and the selected I/O standards. Taking advantage of the support of these I/O standards in Cyclone devices will allow you to lower your design costs without compromising design flexibility or complexity.

More Information

For more information on Cyclone devices refer to the following resources:

- Cyclone FPGA Family Data Sheet
- AN 258: Using Cyclone Devices in Multi-Voltage Systems
- AN 75: High-Speed Board Layout Guidelines

References

For more information on the I/O standards referred to in this document, see the following sources:

- 1.5-V +/- 0.1 V (Normal Range) and 0.9 V - 1.6 V (Wide Range) Power Supply Voltage and Interface Standard for Non-terminated Digital Integrated Circuits, JESD8-11, Electronic Industries Association, October 2000.
- 1.8-V +/- 0.15 V (Normal Range) and 1.2 V - 1.95 V (Wide Range) Power Supply Voltage and Interface Standard for Non-terminated Digital Integrated Circuits, JESD8-7, Electronic Industries Association, February 1997.
- 2.5-V +/- 0.2V (Normal Range) and 1.8-V to 2.7V (Wide Range) Power Supply Voltage and Interface Standard for Non-terminated Digital Integrated Circuits, JESD8-5, Electronic Industries Association, October 1995.
AN 253: Using Selectable I/O Standards in Cyclone Devices

Revision History

The information contained in AN 253: Using Selectable I/O Standards in Cyclone Devices version 1.1 supersedes information published in previous versions. The following changes were made in version 1.1 of AN 253: Using Selectable I/O Standards in Cyclone Devices:

- Updated “Pad Placement & DC Guidelines”.
- Various textual changes throughout the document.