Introduction

Double data rate (DDR) transmission is used in many applications where fast data transmission is needed, such as memory access and first-in first-out (FIFO) memory structures. DDR uses both edges of a clock to transmit data, which facilitates data transmission at twice the rate of a single data rate (SDR) architecture using the same clock speed. This method also reduces the number of I/O pins required to transmit data.

This application note shows implementations of a double data rate I/O interface using Cyclone™ devices. Cyclone devices support DDR input, DDR output, and bidirectional DDR signaling.

For more information on using Cyclone devices in applications with DDR SDRAM and FCRAM memory devices, see “DDR Memory Support” on page 4.

Double Data Rate Input

The DDR input implementation shown in Figure 1 uses four internal logic element (LE) registers located in the logic array block (LAB) adjacent to the DDR input pin. The DDR data is fed to the first two of four registers. One register captures the DDR data present during the rising edge of the clock. The second register captures the DDR data present during the falling edge of the clock.

Figure 1. Double Data Rate Input Implementation

![Figure 1. Double Data Rate Input Implementation](image-url)
The third and fourth registers synchronize the two data streams to the rising edge of the clock. Figure 2 shows examples of functional waveforms from a double data rate input implementation.

Figure 2. Double Data Rate Input Functional Waveforms

Double Data Rate Output

Figure 3 shows a schematic representation of double data rate output implemented in a Cyclone device. The DDR output logic is implemented using LEs in the LAB adjacent to the output pin. Two registers are used to synchronize two serial data streams. The registered outputs are then multiplexed by the common clock to drive the DDR output pin at two times the data rate.

Figure 3. Double Data Rate Output Implementation

While the clock signal is logic-high, the output from \texttt{reg\_h} is driven onto the DDR output pin. While the clock signal is logic-low, the output from \texttt{reg\_l} is driven onto the DDR output pin. The DDR output pin can be any available user I/O pin.

Figure 4 shows examples of functional waveforms from a double data rate output implementation.
Bidirectional Double Data Rate

Figure 5 shows a bidirectional DDR interface, constructed using the DDR input and DDR output examples described in the previous two sections. As with the DDR input and DDR output examples, the bidirectional DDR pin can be any available user I/O pin, and the registers used to implement DDR bidirectional logic are LEs in the LAB adjacent to that pin. The tri-state buffer (TRI) controls when the device drives data onto the bidirectional DDR pin.
Figure 6 shows example waveforms from a bidirectional double data rate implementation.

**Figure 6. Double Data Rate Bidirectional Waveforms**

**DDR Memory Support**

The Cyclone device family supports both DDR SDRAM and FCRAM memory interfaces up to 133MHz.

For more information on extended DDR memory support in Cyclone devices, see the *Cyclone FPGA Family Data Sheet*.

**Conclusion**

Utilizing both the rising and falling edges of a clock signal, double data rate transmission is a popular strategy for increasing the speed of data transmission while reducing the required number of I/O pins. Cyclone devices can be used to implement this strategy for use in applications such as FIFO structures, SDRAM/FCRAM interfaces, as well as other time-sensitive memory access and data-transmission situations.

**Revision History**

The information contained in *AN 256: Implementing Double Data Rate I/O Signaling in Cyclone Devices* version 1.1 supersedes information published in previous versions.

**Version 1.1**

The following changes were made to *AN 256: Implementing Double Data Rate I/O Signaling in Cyclone Devices* version 1.1:

- Updated text under Figure 3 on page 2.