Optical Metrology for Ultra-thin Oxide and High-K Gate Dielectrics

William W. Chism, Alain C. Diebold, and James Price

Abstract. We review the characterization of optical properties of high-K gate dielectric films and film stacks. Modern high-K dielectrics typically incorporate an ultra-thin oxide interfacial layer designed to preserve the channel mobility. High-K filmstack physical characterization data is presented and correlated to the optical response of the material determined via spectroscopic ellipsometry. In-line measurement of film physical thickness relies on the optical models used for fitting the dielectric function. Optimal optical models for use in process control are discussed, as well as limitations of spectroscopic ellipsometry to characterize high-K dielectric/interfacial oxide stacks. We also discuss the application of spectroscopic ellipsometry to characterize high-K dielectrics on silicon-on-insulator substrates.

Key Words: High-K gate dielectric, interfacial oxide, spectroscopic ellipsometry, silicon-on-insulator.

INTRODUCTION

Ultra-thin high K dielectric films are being developed to enable the continued size and speed scaling of the CMOS transistor. A host of metal oxide and metal-silicon oxide dielectric materials and film stack structures have been evaluated or are currently undergoing evaluation [1]. Additionally, silicon-on-insulator (SOI) and strained silicon substrates are coming into increasing use. Metrology for complex ultra-thin film structures, such as high-K gate dielectric filmstacks on strained Si-SOI substrates, will be needed in the near future.

Historically, manufacturing process control has been done using ellipsometric measurement of film thickness and thickness uniformity. This gate dielectric metrology approach relied on the correlation between the physical thickness of the silicon dioxide gate dielectric as determined by ellipsometric techniques, and the effective electrical thickness in the completed device (transistor) [2]. Implementations of single wavelength ellipsometry and spectroscopic ellipsometry have provided sufficient precision to establish manufacturing control of silicon oxide gate dielectrics. With the increase in actual film thickness corresponding to the introduction of high K gate dielectrics, one might expect that the historical gate dielectric metrology approach would again provide sufficient precision, once the optical response of the high K film is known. However, high K film composition has proven notoriously difficult to control in practice, and results in widely varying dielectric properties. Thus, the characterization of physical thickness and material composition of these films is required. It is also important to note that in order to maintain high channel mobility, the high K film is often stacked on a very thin silicon oxide layer [1,3]. This interfacial oxide layer has a minimal effect on the optical response and is very difficult to measure using ellipsometry [4]. However, the interfacial layer capacitive thickness may comprise a significant portion of the total “capacitance equivalent thickness” (CET). Additionally, as the equivalent oxide thickness becomes smaller, the capacitance of the poly depletion layer and inversion layer in the channel make a larger relative contribution to the CET. Thus the correlation between physical thickness of the gate dielectric and the electrical performance of the gate is substantially compromised [4].

It is likely that process control for high K deposition will be done using measurement of film thickness and uniformity. It is also likely that
processes robust enough for manufacturing will 
establish control of film composition during process 
development. As discussed in this paper, 
measurement of EOT and CET are difficult. Despite 
the significance of these outstanding problems, optical 
metrology for material content in ultra-thin high K 
dielectric filmstacks remains of immediate importance 
especially for process development. In order to 
measure the material content and thickness of silicon 
oxynitride and high K dielectric films, current 
metrology implementations may use a combination of 
single wavelength laser based ellipsometry in 
conjunction with multi-wavelength, lamp based UV 
reflectivity \[5\] or UV-NIR spectroscopic ellipsometry 
[2].

For a given ultra-thin dielectric filmstack, the UV 
absorption typically increases with increasing nitrogen 
or high K metal material content \[6\]. This absorption 
produces changes in the real part of the dielectric 
function not only in the UV, but also in the VIS and 
NIR \[6\]. UV absorption may be measured by 
reflectivity \[5\]. Unfortunately, in ultra-thin dielectric 
films the total UV absorption is necessarily quite 
small. High K films generally have larger absorption 
in the UV relative to oxynitrides, suggesting the UV 
reflectivity approach may meet with increased success 
with higher K. On the other hand, spectroscopic 
ellipsometry is more sensitive to the change in shape 
(dispersion) of the real part of the dielectric function 
which occurs over the entire UV-NIR. Spectroscopic 
ellipsometry is relatively insensitive to ultra-thin film 
absorption. Of course, the absorption and real part of 
the dielectric function are connected (through 
Kramers-Kronig relations), so the metrology challenge 
is to decorrelate ultrathin film material content and 
thickness in simultaneous measurement.

In order to understand better the implications of 
this approach it is useful to return to the ellipsometric 
approach upon which it is founded. Here, the implied 
expression for the device “capacitive electrical 
thickness” (CET) is of the form \[y = mx + b\], where 
CET is \(y\), the slope \(m\) is the dielectric coefficient of 
silicon dioxide, \(x\) is the ellipsometric thickness, and 
the linear offset \(b\) is the total capacitive electrical 
thickness of the interfacial, inversion, and poly-silicon 
depletion layers (assumed fixed). The product \(mx\) is 
commonly known as the “equivalent oxide thickness” 
(EOT). Thus, EOT, as measured by ellipsometry, 
provides predictive information concerning future 
device behavior. In the simultaneous material content 
and film thickness measurement approach for high K 
filmstacks, the expression for EOT becomes

\[EOT = (3.92 + K) \times T_{physical}\]

Now, however, the \(K\) value is also measured and its 
precision must be accounted for in the assessment of 
precision for EOT. To first order, the relative 
uncertainty in EOT is the sum of the relative 
uncertainty in \(1/K\) and \(T_{physical}\).

In practice the material content is determined by 
use of a parameterized dispersion model. The Tauc-
Lorentz model provides superior dispersion 
characterization for high K films in the UV-NIR \[6\]. 
Tauc-Lorentz dispersions known to accurately 
represent process endpoints may be combined into an 
“effective medium approximation” (EMA) \[2\], and 
material composition may be extracted from a fit to 
constituent fraction. This approach has been 
employed successfully to extract material content in 
high-K gate dielectrics over a process window and 
offers the advantage of simplicity in implementation 
and interpretation, and also stable fitting capability \[5\]. 
However, due to limitations with sensitivity to material 
content, this approach will require one to two orders of 
magnitude decrease in measurement precision to 
become viable as a production EOT metrology \[6\].

This paper reports the implementation of UV-NIR 
spectroscopic ellipsometry to characterize ultra-thin 
silicon oxide dielectric layers stacked below ultra-thin 
high-K dielectric films. We also demonstrate the use 
of spectroscopic ellipsometry to characterization of 
gate oxide thickness on SOI substrates and discuss 
implications of the advent of strained silicon and 
ultrathin SOI.

**HIGH-K GATE DIELECTRIC / INTERFACIAL 
OXIDE METROLOGY**

As noted, UV-NIR spectroscopic ellipsometry 
(SE) has demonstrated sensitivity to ultra-thin high K 
film material content and physical thickness. However, 
here our goal is to use SE to extract the physical 
thickness of an interfacial oxide, of perhaps only 
monolayer thickness, which is located below an ultra-
thin high K film. We assume otherwise fixed process 
parameters, in particular, material content of the high 
K. Of course, for any given high-K process, choice 
and calibration of fit parameters must be made- recipes 
are not universal. In order to illustrate the approach, 
we use SE to characterize two similar high-K films of 
slightly different composition. These high K films are 
deposited on ultra-thin oxide dielectrics, and some are 
treated with a post deposition anneal in a nitrogen 
ambient. All High-K/ ultra-thin silicon oxide 
filmstacks were processed at International 
SEMATECH on International SEMATECH “test-
wafer" substrates. Twelve wafers were given an SC1/SC2 clean, followed a dilute HF rinse and an ozone dip which nominally leaves an oxide of ~1.1nm. Four wafers were immediately deposited with ultrathin high K films. Two different high K compositions were used. Then one of each pair was given the post deposition anneal for 30 sec. in a N₂ ambient at 700 °C. The other eight wafers were given an ultrathin interfacial oxide layers using rapid thermal oxidation before receiving identical high K deposition and anneal splits. From TEM analysis on several samples, we were able get a locally accurate values of high K and rapid thermal oxide film thickness, and to verify the high-K and oxide layers remained segregated after the post deposition anneal. We illustrate this in Fig. 1, where we show the TEM image for a high K, which was given a post-deposition anneal -PDA.

**FIGURE 1.** HRTEM micrograph of high k dielectric stacked on ultra-thin oxide, after post deposition anneal. Image courtesy Brendan Foran International SEMATECH.

SE measurements were acquired at International SEMATECH using the Woollam VASE™, and analysis was performed at International SEMATECH using the VASE™ off-line analysis software. Extracted high K dispersions for each of the four high K film process conditions are shown in Fig. 2. The solid line and short dotted line are dispersions for high K composition “#1”, both before and after post deposition anneal, respectively. The dashed line and long dotted line are dispersions for high K composition “#2”, both before and after PDA, respectively. In either case, we note an increase in real part of the dielectric function over most of the UV-NIR with the anneal step. This is accompanied by a change in shape from the “as-deposited” dispersion. The relative change in shape with PDA is remarkably similar for either initial high K film composition. Determination of the high K film dispersions is aided by the knowledge of the interfacial thickness—the background dielectric constant of the high K may be adjusted so that the returned ellipsometric fit value for interfacial thickness agrees with the TEM findings. Once these dispersions are determined they are fixed and input to a recipe which returns accurate oxide interfacial layer thickness and high-K layer thickness across the full wafer set.

**FIGURE 2.** Extracted dispersion curves for each of the film material content and anneal conditions are shown in Fig. 2. The solid line and short dotted line are dispersions for the higher metal content high K film, both before and after post deposition anneal, respectively. The dashed line and long dotted line are dispersions for the lower metal content film, both before and after post deposition anneal, respectively.

Now we discuss the findings from this approach. In order to determine the high K and silicon oxide interfacial film thickness, an optical model for each of the four high K composition and anneal process permutations is needed. Using the Tauc-Lorentz optical model with all fit parameters free except the dielectric background [6], and requiring the ultra-thin rapid thermal oxides do not change in thickness with the anneal, each high K composition and anneal condition dispersion is developed and fixed. Then each fixed high K dispersion model is used to extract high K and interfacial oxide layer thickness. Thus, each recipe is used to fit interfacial oxide thickness for three “interfacial” process conditions— the ozone dip, and two rapid thermal oxidations. The results are summarized in Table 1. The uniform mean squared error exhibited for the rapid thermal oxide interfacial processing conditions indicates optimal dispersion model performance has been achieved across this portion of the wafer set. The thickness of the rapid thermal oxides does not depend on anneal, as seen in
the second column. The high K thickness is extracted simultaneously with interfacial oxide thickness, and the (fixed) high K refractive index is also reported. The extracted interfacial oxide thickness of high K film #1, agrees with the expected ~1.1nm thickness, while high K film #2 has a slightly lower extracted interfacial oxide thickness of ~0.6nm.

<table>
<thead>
<tr>
<th>High K/ Ultra-thin Oxide Process Split</th>
<th>Interfacial Oxide Thickness [nm]</th>
<th>Hi K Thickness [Å]</th>
<th>Hi K Index of Refraction</th>
<th>Fit Mean Square Error</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hi K #1/ Interfacial Oxide/ Si</td>
<td>1.03</td>
<td>3.06</td>
<td>1.96</td>
<td>1.18</td>
</tr>
<tr>
<td>Hi K #1/ Interfacial Oxide / Si w/ PDA</td>
<td>1.24</td>
<td>2.43</td>
<td>2.10</td>
<td>.884</td>
</tr>
<tr>
<td>Hi K #2/ Interfacial Oxide/ Si</td>
<td>0.58</td>
<td>2.57</td>
<td>1.84</td>
<td>.988</td>
</tr>
<tr>
<td>Hi K #2/ Interfacial Oxide/ Si w/PDA</td>
<td>0.67</td>
<td>2.66</td>
<td>1.93</td>
<td>1.59</td>
</tr>
<tr>
<td>Hi K #1/ Rapid Thermal Oxide #1/ Si</td>
<td>2.49</td>
<td>2.50</td>
<td>1.96</td>
<td>.686</td>
</tr>
<tr>
<td>Hi K #1/ Rapid Thermal Oxide #1/ Si w/PDA</td>
<td>2.49</td>
<td>2.30</td>
<td>2.10</td>
<td>.683</td>
</tr>
<tr>
<td>Hi K #1/ Rapid Thermal Oxide #2/ Si</td>
<td>2.60</td>
<td>2.39</td>
<td>1.96</td>
<td>.686</td>
</tr>
<tr>
<td>Hi K #1/ Rapid Thermal Oxide #2/ Si w/PDA</td>
<td>2.58</td>
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<td>2.18</td>
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<td>.661</td>
</tr>
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<td>Hi K #2/ Rapid Thermal Oxide #1/ Si w/PDA</td>
<td>2.18</td>
<td>2.38</td>
<td>1.93</td>
<td>.660</td>
</tr>
<tr>
<td>Hi K #2/ Rapid Thermal Oxide #2/ Si</td>
<td>2.28</td>
<td>2.57</td>
<td>1.84</td>
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</tr>
<tr>
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</tr>
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</table>

The results of the analysis above indicate SE has significant sensitivity to interfacial layer thickness when measured simultaneously with high K thickness using optimized recipes. However, this type of measurement, as with the two parameter high K material composition and physical thickness measurement, is expected to find limited use in production due to the required complexity and limited sensitivity.

GATE OXIDE ON SOI SUBSTRATE METROLOGY

The advent of silicon on insulator substrates further complicates matters for gate oxide thickness metrology. In this case, instead of needing just a single parameter returned from an ellipsometric measurement—the gate oxide thickness, now the top silicon and buried oxide thickness must also be measured. Thus the measurement must characterize three parameters simultaneously. As in the case of high K/interfacial oxide metrology, additional optical technologies beyond single wavelength laser based ellipsometry are required. The presence of an additional reflection in SE spectra tends to increase gate oxide thickness precision relative to the silicon substrate only. Also, roughness at the buried interfaces can translate into an unavoidable increase of precision in gate oxide thickness. Thus, the SOI substrate must be characterized extremely well, and optical models which account for substrate variability must be employed, while maintaining gate oxide thickness precision. In Fig. 3 we show the ellipsometric parameter Psi data and fit for a ~2nm gate oxide film on a SOI substrate with approximately 50nm top silicon and ~100nm buried oxide. Preliminary results indicate excellent fitting capability is possible [7]. However, the SE approach to gate oxide metrology on SOI must be evaluated in capability studies before an assessment as to whether it will be viable in production can be made.

FIGURE 3. UV-NIR SE data and fit for 2nm thick gate oxide on silicon-on insulator substrate. The SOI top silicon is ~50nm and the buried oxide is ~100nm in thickness.
CONCLUSIONS AND DISCUSSION

The advent of high K gate dielectric stacked films requires metrology for ultra-thin oxide interfacial layers. A UV-NIR spectroscopic ellipsometry based approach has been implemented with limited success to the measurement of ultra-thin oxide and high K gate dielectric films. Enhanced signal to noise in the UV may improve precision in such an approach. The correlation between physical thickness of the gate dielectric and the electrical performance of the gate is also substantially compromised with the advent of new films. Thus the current gate dielectric metrology approach is reaching its fundamental limitations. The advent of SOI silicon on insulator substrates complicates matters further for gate dielectric thickness metrology. In the case of gate oxide on SOI two additional fit parameters are needed. Additionally, as the SOI becomes thinner than ~10nm, the top Si is subject to optical property changes due to confinement of the electronic wavefunction. This is projected to occur at the 65 nm node [8]. The changes include a blueshift of the absorption features and a change in absorption shape [9]. Such features are usually not observable using SE and do not provide additional information about film thickness. However, subtle optical absorption features may strongly correlate to device performance, particularly for new materials such as strained Si [10]. It is also interesting to note the transistor channel is an ultra-thin 2DEG that will exhibit optical signatures of dimensional confinement, although superimposed on the background Si. So the challenge for the future of optical metrology is the implementation of techniques capable of providing sensitivity commensurate with device metrology measurement requirements. Characterization of subtle absorption edge features in ultra-thin semiconducting films appears to require significant improvement in signal to noise of current spectroscopic ellipsometry implementations.

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REFERENCES


