Characterization of Si/SiGe Heterostructures for Strained Si CMOS


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Abstract. CMOS devices fabricated in a strained Si layer grown epitaxially on a strain-relaxed SiGe virtual substrate exhibit enhanced carrier mobility compared to that of devices fabricated in bulk Si. We demonstrate that the thickness and strain state of the Si layer, and the alloy composition and strain state of the SiGe “virtual substrate” are critical parameters for process monitoring. The strengths and limitations of several characterization methods including x-ray diffraction, Raman spectroscopy and spectroscopic ellipsometry for characterization of these layer structures are discussed.

INTRODUCTION

The amazing performance improvements in CMOS circuits during the last 40 years are primarily a result of reductions in the dimensions of the individual transistors by orders of magnitude enabled by advances in photolithography. However, as device dimensions approach <100 nm, scaling becomes increasingly difficult. Therefore, new materials that can improve circuit performance are of interest.

Improved performance due to increased carrier mobility has been reported for CMOS devices fabricated on a strained Si layer [1-11]. Theoretical calculations predict a higher mobility for both electrons and holes in silicon under tensile strain [12-16]. Tensile strain removes the 6-fold degeneracy in the conduction band, lowering the energy of the two Δ valleys having electrons with a lower in-plane effective mass with respect to the four Δ valleys having electrons with a higher in-plane effective mass. This energy splitting reduces intervalley scattering and preferential occupation of the two Δ valleys with lower in-plane effective mass electrons results in higher electron mobility. Tensile strain also removes the valence band degeneracy at the Gamma-point and shifts the spin-orbit band [1-5], thus improving the hole mobility.

Typically a Si layer under tensile strain is achieved by epitaxial growth of Si on a strain-relaxed SiGe buffer layer on a Si substrate. The relaxed SiGe buffer layer serves as a “virtual substrate” for these devices. The electron mobility increases with increasing Ge mole fraction in the SiGe buffer layer, saturating at about 20% Ge [13]. The hole mobility increases more slowly and saturates at about 35% Ge [16]. Therefore structures consisting of strained Si on a relaxed SiGe buffer layer containing 15-35% Ge are of interest for CMOS applications.

Experimentally, the electron mobility of a strained Si device on a SiGe layer having 13% Ge has been demonstrated to be about 70% higher than the universal MOSFET mobility and that of control Si devices and it is 110% higher when the SiGe buffer layer has 28% Ge [7,8]. The mobility enhancement, which persists at high vertical field in the range required for future CMOS generations, cannot be explained entirely by the band structure modifications, indicating that the tensile strain may also reduce the so-called surface roughness scattering [7,8,13]. The peak hole mobility enhancement when the SiGe buffer layer has 28% Ge has been shown to be 45% greater than that of the Si control device; however, this decreases at high effective field.

The observed mobility enhancement is very exciting. However, there are still many materials issues to be addressed. Key to the success of this technology will be the ability to measure the strained Si/relaxed SiGe heterostructures that are required for strained Si CMOS technology. In this paper we discuss the characterization of these structures.
SiGe “VIRTUAL SUBSTRATES” FOR STRAINED Si DEVICES

An essential feature of strained Si CMOS device structures is the strain-relaxed SiGe buffer layer or virtual substrate. The alloy composition and degree of strain relaxation of the SiGe buffer layer determines the magnitude of the strain in the pseudomorphic Si cap layer. Moreover, the defect density in the SiGe buffer layer must be sufficiently low to achieve the necessary yield of devices with good characteristics.

Strain-Relaxed SiGe Buffer Layers

When a strained Si$_{1-x}$Ge$_x$ layer having x<0.5 grown epitaxially on Si(001) exceeds a critical thickness, strain relaxation occurs by the introduction of 60° misfit dislocations near the SiGe/Si interface. Since Si(001) substrates are essentially dislocation free, the critical thickness in this case is that needed for dislocation nucleation; the critical thickness decreases as the Ge mole fraction of the SiGe layer is increased and also depends on the growth temperature [18-20]. A relatively thick SiGe layer may remain fully strained (pseudomorphic) when grown at low temperature; however, strain relaxation occurs when a metastable structure is subsequently heated, e.g. during device fabrication.

Since dislocations must terminate at a free surface, each 60° misfit dislocation nucleated at the initial growth interface or in the epitaxial layer ends with two threading arms that go through the SiGe layer to the wafer surface. Relatively low threading dislocation densities have been achieved by means of compositional grading. The graded buffer typically consists of a compositionally graded SiGe layer followed by a uniform composition SiGe layer. The alloy composition may be linearly graded or step-wise graded. Threading dislocation densities in the range 10$^5$-10$^8$ cm$^{-2}$ have been reported, with the lowest densities occurring for grading rates as slow as 10% Ge per micron of layer thickness [21]; thus graded Si$_{1-x}$Ge$_x$ buffer layers for strained Si CMOS applications may be as thick as 2-4 μm. Because SiGe has a lower thermal conductivity than Si, self-heating effects are observed in strained Si CMOS devices fabricated on step-graded buffer layers [7,8]. Graded buffer layers also have relatively rough surfaces; a cross-hatch surface pattern is created by the surface steps associated with the 60° misfit dislocations. The surface of the relaxed SiGe buffer layer can be planarized prior to the growth of the active device layers using chemical-mechanical polishing methods. However, the polishing step adds to the cost of fabrication, as does the growth of such a thick SiGe buffer layer.

For these reasons, alternative methods to achieve a much thinner relaxed SiGe buffer layer are under investigation [22-27]. One approach, using molecular beam epitaxy (MBE), employs a special low temperature (200°C) growth step [22]. Another approach, also by MBE, uses plasma cleaning prior to growth [23]. Ion-implantation of hydrogen or helium has been used to create dislocation nucleation sources and thus enhance strain relaxation in thin SiGe/Si structures [24-27]. In this method, a pseudomorphic SiGe layer is first grown on Si(001) at low temperature. The SiGe layer must be thin enough that no strain relaxation occurs during the growth, but thick enough that it exceeds the critical thickness for relaxation at higher temperatures. Hydrogen or helium is then implanted at or below the SiGe/Si interface. After annealing, spherical defects (bubbles) were observed at or below the SiGe/Si interface as well as a dense network of misfit dislocations that relieve the strain in the SiGe layer. We have investigated strain relaxation mechanisms in He-implanted SiGe/Si structures and found that, depending on the He dose and implantation energy, i.e. the depth of the He atoms below the SiGe/Si interface, three different strain relaxation mechanisms occur [27]. For certain implant conditions, we observed that large platelets are formed upon annealing rather than bubbles as reported previously. Dislocations nucleate at the platelets by a prismatic punching mechanism and a dense regular misfit dislocation network is formed at the SiGe/Si interface. Threading dislocation densities in the mid 10$^7$ cm$^{-2}$ range have been reported [24-26]. An advantage of these buffer layers is the low surface roughness, which is typically an order of magnitude smoother than for step-graded buffer layers. And, of course, the implanted/annealed SiGe layers are much thinner than step-graded buffer layers.

SiGe-on-Insulator Substrates

The advantages of strained Si can be combined with the advantages of SOI substrates by fabricating SiGe-on-insulator (SGOI) substrates. Several different methods to fabricate SGOI using a relaxed SiGe buffer layer on Si(001) have been implemented. One group fabricated SGOI substrates by means of a SIMOX-like process, i.e. implantation of oxygen below the surface of the SiGe buffer layer and then annealing at high temperature (>1300°C) to form a layer of SiO$_2$ [28,29]. Apparently this method works only for SiGe buffer layers having low (~10%) Ge. Another approach uses dry oxidation at high temperature after deposition of a pseudomorphic SiGe layer with low Ge content [30]. During oxidation, Ge atoms are rejected from the oxide and condensed in the
remaining SiGe layer, which is partially relaxed without introducing a significant number of dislocations. Raman spectroscopy shows that a strained Si cap layer grown on such a structure has about 1% tensile strain.

Wafer bonding and layer transfer is a very promising method to fabricate SGOI substrates with higher Ge content [9,31-33]. The fabrication steps involve implantation of hydrogen into the relaxed SiGe buffer layer, then bonding the implanted wafer to a Si wafer with an SiO2 layer on top, then annealing to split the SiGe layer and strengthen the bonded interface, and finally epitaxial growth of the strained Si device layers on the bonded SGOI substrate. Key process steps also needed are chemical-mechanical polishing to planarize the surface of the relaxed SiGe buffer layer and subsequent cleaning of the polished surface prior to bonding and also after layer splitting before growing the device layers.

Temperature dependent Hall effect measurements performed on modulation-doped structures grown simultaneously on a polished SiGe buffer layer and on a polished SGOI substrate having the same SiGe alloy composition show the presence of a two dimensional electron gas and identical electron mobility, ~2000 cm²/Vs at 300 K [31]. This indicates that the quality of the SiGe layer on the bonded SGOI wafer is the same as that of the relaxed SiGe buffer layer used to fabricate the SGOI wafer. An enhancement of about 50% in the effective electron mobility was observed in strained Si MOSFETs fabricated on a bonded SGOI substrate having 15% Ge [9,32], comparable to the results for strained Si MOSFETs on thick relaxed SiGe buffer layers on Si substrates. Hole mobility enhancements of 15-20% were found at low vertical field [9,32]; at high vertical field, however, there is negligible mobility enhancement, again comparable to results for “bulk” strained Si pFETs.

We note that as device dimensions are reduced it will be interesting to transfer only a thin strained Si layer to form strained Si-on-insulator (SSOI) wafers. Initial experiments show that this can be done [11].

CHARACTERIZATION OF STRAINED Si DEVICE STRUCTURES BY HIGH-RESOLUTION X-RAY DIFFRACTION

As emphasized in the previous sections, the electrical properties of strained Si MOSFETs depend strongly on the degree of strain in the strained Si layer. This is usually determined by the composition and strain state the underlying SiGe layer. Therefore in addition to the thickness and alloy composition of the SiGe buffer layer and the thickness of the strained Si layer, the strain state of these layers must also be evaluated.

High-resolution x-ray diffraction is the usual method to measure both the alloy composition and strain state of the relaxed SiGe buffer layer. The lattice parameter of bulk (cubic) SiGe increases almost linearly as the Ge fraction of the alloy increases. The strain in the epitaxial film can be determined by measuring the difference between the in-plane and out-of-plane lattice parameters. When a SiGe layer is pseudomorphic, i.e. when the defect density is negligible and thus the in-plane lattice parameter of the SiGe layer is equal to that of the Si substrate, the Ge fraction of the alloy is determined from the measurement of the out-of-plane lattice parameter of SiGe layer, i.e. from the angular separation between the SiGe layer peak and that of the Si substrate on the symmetric 004 x-ray rocking curve. The strong thickness fringes that are present on the x-ray rocking curve in this case allow the layer thickness to be determined as well.

When the SiGe layer relaxes, the misfit dislocations that are present result in mosaic broadening of the x-ray diffraction peak and the thickness fringes are washed out. In this case both the in-plane and out-of-plane lattice parameters must be measured and the alloy composition and the strain are determined using both the symmetric 004 rocking curve and an asymmetric rocking curve, typically the grazing exit 224 [34]. The 004 reflection measures the crystal lattice spacing in the direction of the surface normal, i.e. the out-of-plane lattice spacing. The 224 reflection measures the spacing of lattice planes at an angle to the surface normal, i.e. a set of planes whose lattice spacing has both an out-of-plane and an in-plane component. The composition and the strain are calculated from the angular separation between the SiGe layer and the Si substrate peaks in the two measurements [34]. In the case of a graded SiGe buffer layer, it is necessary to use triple-axis x-ray diffraction, i.e. to insert an analyzer crystal in front of the detector to reduce the angular aperture. This suppresses the mosaic broadening of the diffraction peak thus allowing the various different lattice parameters corresponding to the different SiGe layers to be detected. Here again both the symmetric and asymmetric reflections must be measured to determine the alloy composition and the strain of the various SiGe layers.

Measurement of a thin strained Si layer grown on a graded SiGe buffer layer is much more difficult. Even though the strained Si layer is pseudomorphic to the underlying SiGe buffer layer, the mosaic structure of the SiGe layer is replicated in the strained Si layer,
which is typically <30 nm thick. Triple-axis x-ray diffraction measurements were performed at beamline X20 at the National Synchrotron Light Source at Brookhaven National Laboratory [35]. The composition and strain of the uniform Si$_{1-x}$Ge$_x$ layer were determined as described above. Fig. 1(a) shows the 004 data for a 21 nm-thick Si cap layer on a Si$_{0.72}$Ge$_{0.28}$ buffer layer taken at two different regions, one with and one without the strained Si cap layer. Comparing the two scans, the features to the right of the Si substrate peak are from the strained Si cap layer. Although the Si layer thickness can be determined from the solid curve in Fig. 1(a), comparison with the simulation is more precise when the two scans are subtracted. The difference data obtained by subtracting the two scans in Fig. 1(a) is shown in Fig. 1(b), along with a simulated diffraction scan from RADS [36]. The thickness of the Si cap layer determines the spacing of the oscillations and the strain determines their position with respect to the Si substrate peak. The shift of the experimental data from the Si cap layer with respect to the Si substrate peak is clearly visible. With this method of analysis the relaxation in the Si cap layer with respect to the underlying SiGe layer can be determined to within 1 or 2%, depending on the sample.

**Thermal stability of strained Si structures**

Strained Si CMOS devices, implemented by the epitaxial growth of a 10-30 nm-thick strained Si layer on a relaxed Si$_{1-x}$Ge$_x$ buffer layer on Si(001), are typically grown by a variety of epitaxial methods at relatively low temperatures. However, device fabrication includes standard processes, e.g. the activation of ion-implanted dopant atoms and gate oxidation, requiring temperatures as high as 1000°C. When threading dislocations are present in the substrate, an epitaxial strained layer that exceeds the critical thickness for dislocation glide will relax by the formation of misfit dislocations at the Si/SiGe interface [37]. The rate of misfit dislocation formation increases exponentially with temperature. Interdiffusion at the Si/SiGe interface also occurs at this temperature, resulting in a graded interface and effectively reducing the thickness of the strained Si layer. We have investigated these effects by annealing Si/Si$_{1-x}$Ge$_x$ structures, consisting of a strained Si cap layer of varying thickness on a step-graded Si$_{1-x}$Ge$_x$ buffer layer of varying Si$_{1-x}$Ge$_x$ alloy concentration, at 1000°C for 5, 30 and 300 seconds, times which far exceed those normally used for Si CMOS fabrication [35]. The goal of this work was to measure the magnitude of the strain relaxation of the Si layer and the interdiffusion that occurs at the Si/SiGe interface during annealing and to be sure that the measurement methods used could detect changes in these structures.

The x-ray data of Fig. 1(b) are compared with those from annealed pieces of the same wafer in Fig. 2, where the scans are offset along the vertical axis for clarity. Here we see essentially no change after annealing for 5 seconds, but a small shift of the main diffraction peak toward the Si substrate peak is seen after 30 sec and a larger shift is seen after 300 sec. The thickness fringes are more spread out after 30 sec and even more so after 300 sec. These results clearly show that the Si layer becomes thinner with longer annealing times, and also that the strain in the layer decreases as the annealing time is increased.

Similar changes were observed in other samples. The thickness change for several different
samples is summarized in Fig. 3. The change in the Si cap layer thickness showed no dependence on the initial thickness of the Si cap layer or the alloy composition of the SiGe layer over the ranges investigated [35]. Since these samples were annealed in an inert atmosphere, the most likely explanation is that interdiffusion occurs at the Si/Si1-xGex interface, effectively reducing the thickness of the pure Si layer. These changes in thickness are consistent with experimental values for the diffusion coefficients reported for Ge in Si [38-39]. Interdiffusion results in a graded interface rather than the abrupt one achieved during epitaxial growth at low temperature. This is an advantage for the pMOSFETs, since a graded interface reduces the probability of parallel hole conduction in the top of the relaxed Si1-xGex buffer layer [3].

Fig. 4 shows the time dependence of the strain relaxation for two samples. The Si cap layer is 0% relaxed when the in-plane lattice parameter matches that of the underlying Si1-xGex layer and it is fully relaxed when the in-plane lattice parameter has the value of bulk Si. Even in the worst case, very little strain relaxation occurs (~10%). The trends observed are exactly as expected; greater relaxation occurs for higher Ge mole fraction and for thicker Si layers. The x-ray results agree well with the strain relaxation calculated from the misfit dislocation density determined from planar-view transmission electron microscopy (TEM) images, such as the one shown in Fig. 5 [35]. Other TEM images (not shown) clearly show that the misfit segments terminate at threading dislocations in the upper part of the Si1-xGex buffer layer, indicating that strain relaxation occurs by the glide of threading dislocations in the relaxed Si1-xGex layer.

To avoid the formation of misfit dislocations at the strained Si/SiGe interface during device fabrication, the strained Si/SiGe heterostructures must be thermodynamically stable. The SiGe graded buffer layers are essentially fully relaxed and no change in their lattice parameter was detected after annealing. The strained Si layer is stable provided the layer thickness is less than the critical thickness for dislocation glide. If metastable heterostructures are used, device fabrication process conditions must be restricted to temperatures and times for which dislocation motion is negligible. Although the
Fig. 5. Planar view TEM image of a 21 nm-thick strained Si layer on a relaxed Si$_{0.72}$Ge$_{0.28}$ buffer layer annealed for 30 sec at 1000 °C. The scale bar is 0.5 μm. The misfit density is 2.5 μm$^{-1}$. Reprinted with permission from [35].

absolute strain in the Si layer is important for carrier mobility, it is the change in mismatch strain with respect to the underlying SiGe buffer layer that determined the misfit dislocation density at that interface. Therefore it is important to monitor both the SiGe buffer layer and the strained Si cap layer.

OPTICAL CHARACTERIZATION METHODS

While laboratory x-ray methods are useful for routine characterization of strained Si CMOS device wafers, x-ray measurements that require a synchrotron source are not suitable for timely measurements of a large number of wafers. Thus x-ray diffraction can be used to monitor relaxed SiGe buffer layers, but not for monitoring the thin strained Si cap layer. Although the thickness of the strained Si layer can be measured by cross-sectional TEM, the lengthy sample preparation required for TEM measurements makes this method unsuitable for routine characterization. We have therefore investigated optical methods to determine their potential for metrology of these layer structures.

Raman Spectroscopy

Micro-Raman spectroscopy is a useful technique for the analysis of strained Si on relaxed SiGe heterostructures because it is non-destructive, allows high spatial resolution and has high throughput. Depending upon the wavelength of the incident radiation, surface sensitivities in the range of 10 nm to 1000 nm, can also be achieved.

We have previously described Raman analysis using $\lambda = 488$ nm on strained Si on relaxed SiGe heterostructures [40]. Those results showed that no significant strain relaxation occurred in Si/SiGe layers at annealing temperatures up to 1000 °C for 300 sec. We also showed that Ge diffusion into the Si cap could be detected in the Raman spectra by a drop in the intensity of the Si-Si phonon mode arising from the strained Si layer. More recently we showed that the change in the Si thickness extracted from Raman spectra agreed quantitatively with results from high-resolution x-ray diffraction (HRXRD) measurements [35].

Here we describe new measurements using Raman spectroscopy at $\lambda = 442$ nm excitation and compare with our previous results at $\lambda = 488$ nm as well as with SIMS and HRXRD measurements. We show that the shorter wavelength improves the surface sensitivity by a factor of about 2, and therefore allows measurement of thinner Si capping layers. We also discuss the limitations of Raman measurements for determining the changes in the Si cap thickness that result from interdiffusion at the Si/SiGe interface. Finally, we describe the limitations in the accuracy of Raman measurements for determining the strain relaxation in the Si cap layer.

Fig. 6 shows a comparison of Raman spectra on several Si/Si$_{1-x}$Ge$_x$ samples at excitation wavelengths of 488 nm and 442 nm. The thickness, $d$, of the Si surface layer is 12, 21 or 31 nm and the Ge mole fraction, $x$, of the underlying SiGe layer is 23% as determined by HRXRD. In each case, the plots show the Si-Si phonon modes arising from the SiGe layer and the strained Si layer. The plot taken at 442 nm shows a stronger signal arising from the strained Si layer relative to the SiGe layer. The greater surface sensitivity at shorter wavelengths allows samples with thinner caps to be analyzed. At $\lambda = 488$ nm, the strained Si layer is barely visible at $d = 20$ nm, and at $d = 12$ nm, cannot be resolved, even with curve fitting. On the other hand, at $\lambda = 442$ nm, all thickness of the Si cap can be detected.

Our previous analysis showed that the Si cap thickness can be determined using Raman spectroscopy, given a suitable calibration point, and changes in the Si cap thickness (e.g., as a function of annealing time or temperature), can also be determined. We have subsequently performed high-resolution SIMS characterization of these structures and compared the results with Raman spectra taken at 442 nm. We have utilized the following methodology for determining the cap thickness. After subtracting the baseline intensity, the Raman data are fit using a
double Lorentzian line shape in order to the determine the intensity, Raman shift and full-width half-maximum (FWHM) of the peaks arising from the Si-Si vibrational modes in the SiGe buffer layer and the strained Si cap layer. After curve fitting, the ratio of the strained Si peak area, $A_{SS}$, to the total fit area, $A_{SS} + A_{SiGe}$, is used to extract the thickness change of the Si cap, $\Delta d$, as a function of annealing condition, $y$, according to the following formulas:

$$\Delta d(y) = [1 - r(y)/r(0)] d(0),$$  \hspace{1cm} (1)

$$r(y) = \{A_{SS}(y) / [A_{SiGe}(y) + A_{SS}(y)]\}. $$  \hspace{1cm} (2)

Two sets of samples and annealing conditions were utilized. Sample A has $x = 23\%$, $d = 31$ nm, and was annealed at $1000^\circ$C for varying times, and also annealed for 30 sec at various temperatures. Sample B has $x = 30\%$, $d = 18$ nm, and was annealed at $1000^\circ$C for various times. The initial layer thickness was determined using HRXRD as described in previous sections. The thickness change from SIMS was determined as the point at which the Ge concentration dropped by half. The results are shown in Fig. 7, where the change in the Si cap thickness is plotted vs. annealing time in (a) and temperature in (b). The data show good agreement between the SIMS and Raman data, though the accuracy in the cap thickness measurement determined by Raman is still limited to about $\pm 2$ nm.

The analysis described above to determine the Si cap thickness by Raman assumes a simple two-layer system, when it is known that a significant amount of interdiffusion occurs after annealing at high temperature. To test the validity of this assumption, a three-layer system was modeled and simulated spectra were generated. The three-layer system consists of a Si cap layer, with thickness $d_{Si}$, a Si$_{1-x}$Ge$_x$ substrate and an

![Fig. 6(a). Raman spectra with $\lambda = 488$ nm excitation of Si/SiGe samples with different thickness of the strained Si layer.](image)

![Fig. 7(a). Comparison of thickness changes extracted from Raman data and SIMS data as a function of annealing time for two different sample sets.](image)

![Fig. 6(b). Raman spectra of same samples as in (a) using 442 nm excitation.](image)

![Fig. 7(b). Comparison of thickness changes extracted from Raman data and SIMS as a function of annealing temperature.](image)
intermediate Si$_{1-x}$Ge$_x$ region with Ge content linearly graded between 0 and $x$, and thickness $d_{\text{int}}$. The simulated Raman data from this system, was nevertheless fit using a double Lorentzian line shape to determine at what thickness of the interdiffused region the double Lorentzian fit becomes invalid. Since we assume that the Si cap thickness is defined at the point where the Ge concentration decreases by 50%, the Si cap thickness should not change as long as the interdiffusion is symmetric. Also, since no strain relaxation is assumed, the position of the Si-Si peak arising from the Si cap should also remain constant. The results are shown in Fig. 8, which shows the extracted Si cap thickness and strained Si peak position as a function of $d_{\text{int}}/d_{\text{Si}}$. The plot shows that when the thickness of the interdiffused region is over roughly 50% of the original cap thickness, significant error in the peak area and position is seen to occur, setting an upper limit on the validity of the two-layer model. A more sophisticated three-layer model can be used to account for the interdiffusion, but the number of adjustable parameters makes accurate curve fitting difficult. For the results shown in Fig. 7, the interdiffused region is much thinner than the limit described above, indicating that the two-layer fit is a valid assumption for these layers.

Raman spectroscopy is also useful in determining the amount of strain in strained Si on relaxed SiGe layers, and the strain relative to bulk Si can be determined with good accuracy. However, what is perhaps most important for CMOS applications is to determine whether or not the strained Si layer is relaxing via the formation of misfit dislocations at the Si/SiGe interface. These misfit dislocations can possibly lead to yield and reliability problems for devices. Since only a small degree of strain relaxation is needed to cause a significant degree of misfit dislocations, it is important for a characterization method to be extremely sensitive to small variations in the in-plane lattice constants of the two layers. However, due to several uncertainties in the system parameters this is difficult task using Raman spectroscopy. First of all, the strained Si peaks must be compared to a Si control. Secondly, the strained Si peak is sometimes small and can be difficult to fit accurately. As a function of thermal annealing, the strained Si peak position can be shifted due to interdiffusion at the Si/SiGe interface, as shown in Fig. 8. Finally, the SiGe in-plane lattice constant cannot be uniquely determined by solely examining the Si-Si peak arising from the SiGe layer. This is because the peak position is determined not only by the Ge concentration of the SiGe layer, but also by the residual strain in the layer. If the SiGe layer is not fully relaxed, relaxation can occur after annealing, causing greater strain in the Si layer, and counteracting any apparent loss of strain caused by misfit dislocations. Our analysis on Si/Ge layers using Raman spectroscopy has shown that the net relaxation of the Si cap layer, relative to the underlying layer, can only be determined with an accuracy of ±2-4%, and is therefore much less accurate than other methods such as HRXRD and XTEM. Therefore, for routine analysis of non-patterned Si/SiGe layers, Raman spectroscopy is of limited value for determination of the misfit formation and plastic relaxation due to annealing. However, Raman measurements could be useful for analyzing strain relaxation in patterned structures, where much greater relaxation is expected to occur and where other analysis methods do not have sufficient spatial resolution.

**Spectroscopic Ellipsometry**

Film thickness measurements by spectroscopic ellipsometry have become a valuable part of semiconductor metrology. This method relies on analyzing the reflection of polarized light for wavelengths from the UV to near-IR in terms of the Fresnel coefficients of each material in a film stack. For Si$_{1-x}$Ge$_x$ and Si layers, the optical properties of the two materials are sufficiently different, even at relatively low values of the Ge mole fraction $x$, that layers of the two materials are easily distinguished. Graded buffer layers, whether smoothly graded or step-wise graded, are modeled by a series of layers each of fixed composition and thickness, such that the total thickness equals that of the buffer layer. Intermixing at boundaries resulting from heat treatments can be handled the same way. Roughness at the upper surface is handled by modeling as a thin layer comprised of a mixture of native oxide and “void.”
The ellipsometer measures the reflectances \( r_p \) and \( r_s \) of light polarized parallel and perpendicular to the plane of incidence, respectively. The data are usually displayed as \( \tan \Psi \) and cosine \( \Delta \), where

\[
r_p / r_s = \tan \Psi \exp(i \Delta) \quad (3)
\]

As an example, \( \tan \Psi \) and cosine \( \Delta \) for a strained Si/SiGe stack consisting of a native oxide, a 20 nm strained Si layer, and several layers of SiGe with different thickness and composition are shown in Fig. 9. The layer thickness and alloy composition, but not the strain, are readily obtained from such data, provided the correct optical properties are used in the model. Grading in either of the SiGe layers requires a more complicated model. If the SiGe buffer layers are made thicker, more peaks appear in the spectra and the analysis is facilitated by extension of measurement wavelengths farther into the infrared.

In practice, we have found that this method gives good results for some types of Si/SiGe layer structures, including strained Si on SGOI and strained Si on implanted/annealed buffer layers. For example, ellipsometry measured a strained Si layer thickness of 6.5 nm compared to 7.9 nm measured by HRXRD and 7.2 nm by cross-sectional TEM. The difference is within the error of the x-ray measurement. However, ellipsometry results obtained for strained Si on step-graded SiGe buffer layers do not agree well with the values measured by other methods. For the annealed samples discussed above, ellipsometry measurements show comparable thickness changes for the strained Si layer, but the measured thickness values are typically somewhat lower than those determined from x-ray diffraction and the composition of the SiGe layer is a lot lower than that determined from x-ray measurements. This difference may arise because the optical constants for SiGe layers taken from the literature are not accurate for the dislocated SiGe layers in the graded buffer layer structures.

**CONCLUSIONS**

Strained Si CMOS devices fabricated on 200 mm wafers using standard CMOS fabrication processes exhibit increased carrier mobility primarily due to the modified band structure in Si under tensile strain. These devices are fabricated in a strained Si layer grown epitaxially on a strain-relaxed SiGe buffer layer that acts as a “virtual substrate”. The relaxed SiGe layer may also be the thin SiGe layer of an SGOI substrate. High-resolution x-ray diffraction is very useful for evaluating the alloy composition and strain state of the relaxed SiGe buffer layer, but cannot evaluate the strained Si cap layer on these samples unless a synchrotron x-ray source is used. Raman spectroscopy and spectroscopic ellipsometry are interesting for metrology applications. The absolute strain in the Si cap layer can be measured using Raman spectroscopy and the layer thickness can be determined when a suitable calibration is performed. The thickness of the strained Si layer is easily measured by spectroscopic ellipsometry, as is the composition and thickness of the SiGe buffer layer in some types of structures. We note that the measurement error inherent in some of these methods is as large as 3-4 nm, a significant fraction of the thickness of the strained Si cap layer. We also note that x-ray reflectivity is another possible method for measuring the strained Si layer thickness; however, this method can only be used for structures having very flat surfaces and interfaces.

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