Overview of Lithography: Challenges and Metrologies

Harry J. Levinson

Advanced Micro Devices
One AMD Place, MS78
Sunnyvale, CA 94088

Abstract. Semiconductor microlithography is rapidly reaching a point where it becomes exceedingly difficult to shrink features at historical rates. We will no longer be able to increase process windows by going to shorter wavelengths with optical lithography, because we are running out of useable wavelengths. This necessitates either the implementation of processes with very small process windows or a transition to radically new types of lithographic technologies. Either situation presents numerous challenges to lithographers and metrologists. Particularly daunting are the requirements for gate linewidth control for microprocessors. Reducing variation requires improvement in the components of variation, each of which must be smaller than the total result. In order to improve a particular parameter, such as CD variation, metrology must be adequate for identifying improvements in the components of that parameter, not just the total. This places very tight requirements on metrology capability. Departing from optical lithography into the Brave New World of Next Generation Lithography will necessitate new metrology capabilities in several areas, not just the measurement of features on wafers. Creating the capabilities that will be needed in the future requires that funding be available for the requisite development. The need for huge amounts of funding to develop new lithographic technologies will likely necessitate a slowing down in the pace at which we shrink features. It is absolutely essential that a balance is re-established between the prices that purchasers of chips are willing to pay and chip development and manufacturing costs. This will be very challenging with 300 mm wafer fabs coming on-line, since low chip prices have historically been associated with overcapacity in the semiconductor industry, and it is anticipated that new lithographic technologies will be very expensive.

INTRODUCTION

Advances in projection optical lithography have enabled a shrinking of the minimum feature sizes of integrated circuits from several microns to approximately 100 nm today. A major factor that has enabled this shrinking has been the use of shorter wavelengths in the lithography used to define circuit patterns. With 157 nm lithography, we are seeing the shortest possible wavelength that can be used while still referring to the lithographic technology as optical. Without the ability to shrink the wavelength further, controlling lithographic processes will become increasingly difficult. The type of problem that arises will be illustrated by discussing the challenge controlling microprocessor gate lengths. To circumvent the intrinsic problems associated with practicing lithography at the limits of optics, various “next generation” lithographic technologies have been proposed. Such non-evolutionary approaches have their own sets of problems. Regardless of the approach taken, it will be expensive. Every new lithographic technology will require advances in metrology. In this paper, a look is taken at some of the new lithographic technologies that will most likely appear within the next few years, along with some of the new metrology capabilities that will be required to support them.

WHY 157 NM IS THE LAST WAVELENGTH FOR OPTICAL LITHOGRAPHY

To understand why 157 nm is the last wavelength for optical lithography, it is necessary to have a precise definition of what it means for a lithographic technology to be considered “optical.” A lithographic technology is “optical” when all three of the following conditions have been met:
Optical lithography is defined as any lithographic technique that:

1) Uses photons to induce chemical reactions in a photoresist,
2) Involves a transmission photomask, and
3) Has the potential for image reduction using projection optics.

The photomask is what creates the problem with using wavelengths shorter than 157 nm. Fused silica, the material that has been used for photomasks for decades, has many important attributes. Among these is its coefficient of thermal expansion, which is only 0.5 ppm/°C. With such a small coefficient of thermal expansion, geometries separated by 50 nm across the reticle will maintain their registration to within 2.5 nm for a 0.1°C change in temperature. With 4x reduction optics, this registration error, typical of the thermally induced errors that occur during mask fabrication, can be easily absorbed into overlay budgets. (See Table 1.)

### TABLE 1. Overlay requirements from the 2002 update to the International Roadmap for Semiconductors

<table>
<thead>
<tr>
<th>Year of production</th>
<th>2010</th>
<th>2013</th>
<th>2016</th>
</tr>
</thead>
<tbody>
<tr>
<td>DRAM half-pitch (node)</td>
<td>45 nm</td>
<td>32 nm</td>
<td>22 nm</td>
</tr>
<tr>
<td>Overlay requirement</td>
<td>18 nm</td>
<td>13 nm</td>
<td>9 nm</td>
</tr>
</tbody>
</table>

For wavelengths below 157 nm, fused silica loses its transparency, and a different substrate material is required for transmission photomasks. All known materials with good transparency below 157 nm have coefficients of thermal expansion that are at least an order of magnitude larger than that of fused silica. Small changes in mask temperature, which will occur during mask fabrication and usage, will induce registration errors larger than can be tolerated for semiconductor technologies of the future. Thus, 157 nm is the “end of the trail” for optical lithography.

It will be very difficult to continue shrinking features without the ability to use shorter wavelengths. To achieve smaller feature sizes with a fixed wavelength, it will be necessary to develop increasingly complex optical proximity corrections and sophisticated resolution enhancement techniques, which will come with increasing difficulty.

### THE CHALLENGE OF GATE LINEWIDTH CONTROL FOR MICROPROCESSORS

The biggest challenge facing optical lithographers today and in the near future is gate linewidth control for microprocessors. In the International Technology Roadmap for Semiconductors (ITRS), it is assumed that physical gate linewidths will need to be controlled to within ±10% of their nominal widths. In recent years microprocessor gate widths have decreased rapidly (Table 2), to the point where the gate widths found in today’s microprocessors represent a nine year acceleration over the gate widths predicted in the 1994 ITRS. A number of non-lithographic “tricks” have enabled the average gate width to be very short, but it remains necessary to limit variations to ±10% of final gate dimensions. This has meant a nine year acceleration in lithography process control, which has been very challenging.

### TABLE 2. Microprocessor (MPU) gate linewidth requirements from the 2002 update to the International Roadmap for Semiconductors

<table>
<thead>
<tr>
<th>Year of production</th>
<th>2003</th>
<th>2005</th>
<th>2007</th>
</tr>
</thead>
<tbody>
<tr>
<td>DRAM half-pitch (node)</td>
<td>100 nm</td>
<td>80 nm</td>
<td>65 nm</td>
</tr>
<tr>
<td>MPU gate linewidth (in resist)</td>
<td>65 nm</td>
<td>45 nm</td>
<td>35 nm</td>
</tr>
<tr>
<td>MPU gate linewidth (after etch)</td>
<td>45 nm</td>
<td>32 nm</td>
<td>25 nm</td>
</tr>
<tr>
<td>MPU gate linewidth control (nm, 3σ, lithography only)</td>
<td>3.7 nm</td>
<td>2.6 nm</td>
<td>2.0 nm</td>
</tr>
</tbody>
</table>

As the resolution limit of optics is approached, every source of linewidth variation will need to be controlled nearly perfectly to pattern the very small MPU gates and meet the associated linewidth control requirements. Among the sources of variation are:

- Reticles
- Exposure tools
- Lenses
- Focus variation
- Dose control
- Resist processing
- Line edge roughness

Metrology particularly will be challenged, since improvement will be required for each contributor to
variation. Thus, metrology will be required to measure improvement in individual factors, not just the total variation. The required precision/tolerance ratio will need to be based on a fraction of the bottom line of Table 2. Fortunately, improvement in many factors can be determined without measuring linewidths on wafers. For example, reticle linewidths are 4x larger than wafer dimensions, and lens aberrations can be measured by interferometry. On the other hand, line edge roughness is a very small fraction of the total linewidth and precise measurement is required.

FIGURE 1. SEM of resist showing line edge roughness.

To extend optical lithography as far as possible, innovative resolution enhancement approaches are required. Among the techniques that are being used are phase-shifting masks, off-axis illumination, and sub-resolution assist features. Each approach is more complex than simple imaging with a binary, chrome-on-glass mask.

THE LIMITS TO OPTICAL LITHOGRAPHY AND ALTERNATIVES

While optical lithography may be extended through innovations in resolution enhancement methods and skilled application, there are theoretical limits to the resolution capabilities of optics. With phase-shifting, the smallest half-pitch that can be resolved with optics is

$$0.25 \frac{\lambda}{NA},$$

(1)

where $\lambda$ is the wavelength of the light and NA is the numerical aperture of the lens. For imaging in air, the largest that NA can be is just under 1.0. For 157 nm light, this makes $157/4 \approx 40$ nm the absolute limit to optical lithography. This absolute limit is most likely not achievable. More practical limits would be $NA = 0.95$ and a prefactor ($k_1$) of $-0.3$. With these values, the limit of optical lithography is about 50 nm.

To shrink features even further, a significant departure from optical lithography will be needed. While extending optical lithography through the application of resolution enhancement techniques will be difficult, at least lithographers will be following evolutionary technology development. To extend lithography past the limits of optics, a radically different approach will be needed.

Several next-generation lithographic technologies have been proposed, among them Extreme UV (EUV) lithography, ion projection lithography (IPL) and electron projection lithography (EPL). All of these techniques require completely new light sources, mask technology, and projection lenses. Exposures will take place in a vacuum. Implementing radically new technology is always more difficult that pursuing evolutionary approaches. Extending lithography beyond 50 nm half-pitches must necessarily occur at a slower pace than historical rates of change.

One patterning approach that is a measure between conventional optical lithography and next-generation lithographic techniques is immersion lithography. By filling the space between the lens and the wafer with a fluid, the numerical aperture can be increased by the refractive index of the fluid. For example, at a wavelength of 193 nm, water has an index of refraction of $\sim 1.47$. Lenses with numerical apertures as high as 1.3 are being considered. Using 0.3 as the prefactor in Eq. 1, 193 nm lithography could be extended to 45 nm, and 157 nm lithography could produce 35 nm half-pitches, if a suitable fluid can be found for use at that wavelength.

Immersion lithography has certain attractions. For example, conventional mask technology could be used, so at least one part of the lithographic technology would be an evolutionary extension of optical lithography. However, there are obvious technological hurdles that need to be overcome, such as the challenges of transferring wafers into and out of the immersion fluid. Bubbles in the immersion fluid, even with diameters measuring a few tens of nanometers, will be intolerable. It remains to be seen if these technological challenges can be overcome, and exposure tool manufacturers are in the process of evaluating the viability of immersion lithography.
If it is found that immersion lithography cannot be made to work, or if it is desired to extend lithography beyond 35 nm, then a next-generation lithographic technology will indeed be required. The next-generation technology with the most support is EUV lithography.

**EUV Lithography**

EUV lithography represents a significant departure from conventional optical lithography. Because there are no materials with reasonable transparency, all-reflective optics and reflective masks are needed at EUV wavelengths. In order to achieve adequate reflectivity, mirror surfaces are fabricated using film stacks comprised of layers that alternate between low and higher indices of refraction. There are limited film stacks that will work at EUV wavelengths, and a multilayer stack comprised of molybdenum and silicon layers appears to be the film stack of choice for EUV lithography. This film has a maximum reflectance of approximately 70% for wavelengths in the neighborhood of 13.5 nm.

In EUV exposure systems, lenses will need to be all-reflective. This requires that lens makers develop new skills in mirror fabrication. To benefit from short EUV wavelengths, lens aberrations will need to scale with the wavelength. This necessitates extraordinary control of mirror surfaces, to less than 0.3 nm rms. Monolayer contamination of the mirror surfaces will affect light transmission. The system will need to be operated in ultra-high vacuum.

The most widely discussed format for EUV reticles consists of patterned absorbers on a multilayer-reflector. (See Figure 2.) Because multilayers cannot be repaired, it will be necessary to deposit essentially perfect multilayers. EUV mask technology will be very different from today’s optical masks and will be quite challenging. New mask infrastructure will be required.

For example, a parameter that will be critical will be the reflectance of the multilayer following mask fabrication. This will necessitate that mask shops have capabilities for measuring reflectance at EUV wavelengths. (Figure 3.)

The reflective nature of the masks will require that the mask substrates be extremely flat, since small surface curvature will result in an image placement error. (Figure 4.) Mask flatness better than 50 nm will be required. This necessitates improvement in substrate fabrication, and new metrology is required in order to ensure this level of flatness.

As can be seen, EUV masks will require the creation of substantially new infrastructure. Not only will new technology be required, but it must achieve extremely ambitious targets from the very beginning: defect-free multilayer films, well controlled thicknesses of the multilayers, and very flat substrates.

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**FIGURE 2.** Cross section of an EUV mask.

**FIGURE 3.** Reflectance from EUV multilayers.

**FIGURE 4.** Cross section of an EUV mask showing the effects of non-flatness.
The challenges of EUV lithography are daunting, but not insurmountable. However, considerable resources will be required to develop the required capabilities. Can the semiconductor industry afford the development costs?

**LITHOGRAPHY COSTS AND THE LITHOGRAPHY ROADMAP**

Costs are increasing for each new generation of lithographic technology that we develop. This can be seen in the rising prices of exposure tools. (Figure 5.) Historically, exposure tool prices have risen exponentially, with prices doubling approximately every five years. More ominously, the prices of recently introduced tools exceed the historical trend. Tool prices in the past have sometimes been above the historical trend, but the gap between actual and projected tool prices can now represent more than ten million dollars.

Lithography tool costs must be assessed relative to the productivity that can achieved. A metric of exposure tool productivity is the cost to pattern a unit area of silicon exposed per hour. In the past, increases in exposure tool prices have been offset by increasing in productivity. (Figure 6.) This increased productivity has come from two sources, larger diameter wafers and greater throughput, as measured in wafers per hour.

The newest exposure tools, ArF (193 nm), F$_2$ (157nm), and EUV all have, or are expected to have, lower throughput and considerably higher prices than current advanced KrF (248 nm) systems. This combination of reduced throughput and much higher tool prices leads to higher cost-of-ownership. Unless there are significant breakthroughs in throughput for F$_2$ and EUV exposure systems, or much lower prices, there will be an unprecedented increase in lithography cost-of-ownership.

Development costs are also straining the semiconductor industry financially. The development of each new generation of lithographic technology requires a large amount of money. The semiconductor industry is currently pursuing several new technologies, with large efforts ongoing in F$_2$ (157 nm) and EUV lithography, and with smaller efforts in electron projection lithography (EPL) and maskless lithography. Immersion lithography, if seen to be promising, will require significant investments to make production worthy. Moreover, these developments are being attempted at a time when the semiconductor industry, as a whole, is not profitable. Without the necessary financial resources, the pace of development must necessarily slow down, and thus the pace at which the roadmap is traveled will also slow down.

The semiconductor industry is currently hard-pressed to find the financial resources needed to fund the R&D of future lithographic technologies, because few companies are currently profitable. The outlook for profitability is unclear. The semiconductor industry has historically suffered financial loses when supply greatly exceeds demand and chip prices fall. Larger wafers, such as 300 mm, mean that large capacity can be quickly installed. This can lead to a prolonged
period of excess capacity in semiconductor manufacturing.

**SUMMARY**

Lithography is becoming increasingly challenging. There are both financial and economic challenges to producing smaller features. The weight of these challenges will cause a slowing down of the roadmap. This is not necessarily a bad thing.

**REFERENCES**

5 Private communication from Dr. Donald Sweeney, Lawrence Livermore National Laboratory.