The Transition to Optical Wafer Flatness Metrology

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Abstract. As optical lithography requirements drive wafer flatness toward increasing levels of perfection, the industry is faced with a need to transition from current standard practice. In this paper we present a historical perspective on starting material dimensional metrology, leading to the current standard for wafer manufacturing quality control, capacitance-based wafer flatness metrology. We then investigate the market and technical factors that compel a transition to optical flatness metrology. Comparative data (from advanced 300mm wafers) between capacitive and optical flatness measurement tools permits us to conclude that the industry transition to optical dimensional metrology can occur without disruption of accepted manufacturing baselines.

INTRODUCTION

Advanced semiconductor device manufacturing will continue using optical lithography for several more generations of ever smaller critical dimension (CD). A lithography system’s resolution scales as the illumination wavelength (λ) divided by numerical aperture (NA). Opportunities for easily reducing the illumination wavelength, in order to achieve a smaller CD, are neither obvious nor inexpensive. So the prospect of higher NA projection lenses is a near certainty.

But this solution to printing CDs significantly shorter than λ also has its issues. Lens design and lens material quality become hypercritical, while lithography depth-of-focus (DOF) scales as λ/NA². Thus higher NA lithography, to achieve finer resolution, increases the pace at which the DOF budget must be reduced. Tighter constraints on incoming wafer flatness tolerance (T) are one important aspect of this DOF budget reduction.

To economically scale the production of flatter wafers a commensurate improvement in the wafer flatness metrology precision (P) is required. That is, P/T must remain under control for metrology to affordably avoid misclassification errors. In the work that follows we introduce the technology and metrics of production wafer flatness metrology from a historical perspective, including evolution to present times. We conclude by demonstrating optical wafer flatness metrology that enables advanced and next generation wafer manufacturing with excellent precision and correlation to established baseline wafer flatness measurements.

WAFFER FLATNESS MEASUREMENT

Wafer flatness is a term that people in semiconductor manufacturing would say they understand well. In reality, many of these people use the term “flatness” when discussing a wide range of wafer dimensional issues, especially “shape” or unclamped flatness. In this paper we consider only flatness in a clamped state. The statement, “That wafer is not flat because I can see bow in the reflection” sounds reasonable. However, true wafer flatness does not preclude bow of any amount.

Thickness-Based Flatness

The ultimate question concerning a wafer’s suitability for lithography is “Will this wafer present a flat surface over the projection system field-of-view for all required fields-of-view?” This question has no simple answer, as we will see. However, the industry...
has devised a methodology to enable high volume manufacturing of wafers with predictable printability.

One of the keys to this methodology is understanding the relationship between a wafer’s dimensional properties and how that wafer presents in the lithography tool. Another key is performing the appropriate wafer dimensional measurements without introducing measurement artifacts or interferences.

The model presented in Fig. 1 permits two common wafer flatness measurement paradigms. One is called chucked flatness, where the topography of the wafer front surface is measured after chucking. Unfortunately, neither chucks nor chucking are perfect so the measurement includes possible artifacts such as chuck imperfections, and possible interferences such as contamination forcing a gap between the chuck and wafer backside. Combined with the potential for wafer backside damage during chucked measurement, it is easy to understand why the silicon wafer industry has adopted the second paradigm.

The second paradigm is to measure the wafer thickness variation in an unchucked state. Modern wafer dimensional metrology measures thickness variation, and assumes perfect chucks (C(x,y) = constant) and chucking (G(x,y) = 0). In this paradigm the important shape parameters, such as bow and warp, can easily be measured simultaneously with flatness. Shape is a measurement of the wafer’s natural (unchucked) non-planarity and is completely independent of flatness (thickness variation). SEMI Standard M1 (and references therein) is a valuable source of information regarding both wafer flatness and shape. This definition of flatness being solely a function of thickness variation rather than a wafer’s shape may seem non-intuitive. However, it enables predicting wafer printability based solely on the wafer’s dimensional properties.

There are today some parties suggesting that chucked wafer flatness is the most important flatness to measure. This sentiment has a strong foundation in that wafers are chucked in actual use. However, chucked flatness denies practical implementation due to technical and business reasons. Technical reasons include contamination and damage during chucking while business reasons for choosing thickness-based flatness likely dominate the decision.

Since wafer manufacturers have no control over how their product is chucked, they can only optimize wafer thickness variation and wafer shape. The present industry paradigm of wafer makers being responsible for their product, lithography tool suppliers being responsible for chucks and chucking,
and device makers responsible for the successful integration of wafers and lithography tools is based on clear ownership of responsibilities. This paradigm and its basis of ownership is not broken and should be continued.

**Capacitive Wafer Flatness Measurement**

Geometric properties of early silicon wafers were measured with common mechanical tools such as micrometers or dial indicators. Wafer thickness was the primary concern, mostly to facilitate manufacturing processes such as lapping and polishing where thickness uniformity contributed to productivity.

It quickly became evident that mechanical thickness-measuring tools would damage the front surface of the wafer. Non-contact thickness measurement tools emerged, based on technologies as varied as electrical capacitance, air pressure and sound wave reflection. A common feature of almost all the non-contact tools used in wafer production was the embodiment of a two-sided measurement technique. That is, thickness could be measured independently of the precise position of the wafer within the measurement fixture (see Figure 2).

**FIGURE 2.** Thickness, $T$, is equal to the calibrated probe gap spacing, $PG$, minus the measured Probe A and Probe B to wafer distances, $D_A$ and $D_B$, respectively ($T = PG - D_A - D_B$). Note that in-situ mastering is used to monitor $PG$ over time and environmental changes.

This two-sided measurement technique represented a great step forward since it was very difficult to fixture the wafer to the desired level of precision (of the order of 25 $\mu$m). The capacitance technology became dominant for factors including precision, robustness, and throughput. It is based on the simple and exact physical relationship between probe-to-wafer distance, $d$, and measured capacitance, $C = \varepsilon A/d$, where $\varepsilon$ is the permittivity of the space between probe and wafer and $A$ is the area of the probe. This analytical relationship allows for precise calibration with high dynamic range and linearity, repeatability and stability. Fig. 3 shows an early capacitance-based thickness gage, the ADE MicoSense$^\text{®}$ 6033T system. Some of these early models are still in use today.
Fundamental to the robust performance of these capacitive tools was their immunity to vibration. As wafer size scaled and data density increased the wafer was scanned between front and back probes at ever higher speeds. This led to significant wafer vibration with respect to the thickness variation being measured. Probe signals from front and back surface signals are therefore combined such that vibration induced displacement cancels in the thickness measurement.

Capacitive wafer flatness measurement has dominated silicon wafer manufacturing for 25+ years. Capacitive tools that are currently in production worldwide, such as the AFS-3200 Advanced Flatness System™ shown in Figure 4 with its optical counterpart, WaferSight™, enabled the transition to 300mm wafers. These tools are already qualified by advanced device manufacturers to certify incoming substrates for 90 nm node production lines.
Optical Wafer Flatness Measurement

Two fundamental and significant reasons lead to the conclusion that optical wafer flatness metrology will someday supplant capacitive. First, wafer flatness requirements have become so stringent that back surfaces must now be either fully or partially polished (double-sided polish, DSP or advanced single-sided polish, ASSP, respectively). This fact enables direct interferometric measurement of both wafer surfaces.

A key limitation of capacitance-based metrology is the inability to acquire data in a massively parallel fashion. High-performance capacitive probes cannot be easily manufactured in arrays. Therefore the system must sequentially scan every measured point on the wafer. Until current generations spatial resolution requirements permitted using probes with relatively large dimensions. For spatial resolution below 2 mm the additional time to scan with a finer sized probe would be prohibitive. The alternative of surface sub-sampling with a finer sized probe, rather than complete surface mapping at reduced pitch, is not production worthy in that details can be too easily missed.

In contrast, optical interferometry lends itself to an imaging approach using CCD detector arrays. Modern CCD cameras allow millions of data points to be collected and processed at high speed. These detector arrays are relatively low cost due to significant commercial interest in their development for purposes such as digital cameras and video recorders.

At this time equipment decisions for next generation wafer manufacturing lines (130 nm node and below) are being made. The optical wafer flatness tool, WaferSight™ is emerging as the preferred technology in these decisions, when customers choose optical, for reasons we explore below.

Figure 5 presents a model of the WaferSight™ measurement technology. Dual-opposing Fizeau interferometers are used to simultaneously measure both front and back wafer surface topography. These measurements use advanced phase-shifting interferometry to enable sub-nanometer resolution, direct-height topography acquisition over the entire wafer surface (200mm or 300mm).

Fizeau interferometry is used to minimize the non-common path in the interferometer while permitting full-aperture acquisition. The minimization of the non-common path reduces most phase-noise terms in the interferometer design. As all advanced wafers that require high precision metrology have strong specular reflection at normal incidence, the Fizeau design is preferred.

Some alternative optical tools use grazing incidence interferometer designs. Such designs enable measurement of higher roughness surfaces at the expense of several important technical trade-offs. These include increased noise due to long non-common path, reduced sensitivity due to longer effective wavelength, and non-normal surface imaging issues that produce extremely elongated surface sample elements. In that advanced polishing
techniques produce wafer surfaces that exhibit specular reflection at normal incidence, the issues with grazing incidence interferometry can be easily avoided using the WaferSight™ design. For rougher surfaces, such as those encountered during the early stages of the wafer making process or on older generation SSP wafers, advanced capacitive tools continue to provide precision data with required spatial resolution.

OPTICAL MEASUREMENT CORRELATION TO CAPACITIVE BASELINE

The semiconductor industry manufactures excruciatingly complex products in high volume. Thus metrology is used in statistical process control (SPC) mode. In some sense, absolute measurement accuracy is not nearly so important as attributes such as precision, stability, and tool-to-tool matching. That is to say, a measurement can be biased from the truth (inaccurate) and still be useful in manufacturing. Measurements that are not precise or that are not stable will not be used in manufacturing.

Matching systems within a factory or around the globe is an advanced metrology tool requirement. Matching can be achieved with constant bias, but it is generally achieved through accuracy. In the case of the highly evolved capacitive wafer flatness measurement, accuracy enables matching. Accuracy in turn also enables optical systems to correlate to these industry baseline measurements if the optical measurements are also accurate.

In Figure 6 below the thickness variation of two wafers is presented for measurements from both the AFS and WaferSight™ measurement tools. The detailed correspondence of these thickness variation maps is clear. All four maps are presented with 2 mm edge exclusions. Figure 7 presents the scatter-plot of AFS vs. WaferSight™ SFQR measurements for 25 wafers using all sites (full and partial) with site size of 26 x 8 mm². SFQR is the Site flatness, referenced to the Front surface, using the site least-squares best-fit plane removal (Q), with the data Range reported. The correlation coefficient between WaferSight and AFS is > 95%.
FIGURE 6. Thickness maps for two wafers are presented using two different measuring tools, the AFS capacitive tool (left) and the WaferSight™ optical tool (right). Both maps are presented with 2 mm edge exclusion and their SFQR data is included in Fig. 7 below. The wafer shown on top has extremely small total thickness variation.
FIGURE 7. Correlation for SFQR on 25 wafers, all sites (full and partial), is shown. Site size was 26 x 8 mm² with no offset and 2 mm edge exclusion. A total of 8064 data points are fit with an $R^2$ of 97%. As expected, the higher resolution optical WaferSight™ measurement gives slightly higher SFQR values.

CONCLUSION

Wafer flatness metrology is likely to transition to optical interferometric techniques in the coming years for advanced wafer manufacturing capacity growth. Both wafer manufacturers and semiconductor device manufacturers are now running demonstrations on both capacitive and optical tools to decide their future direction of choice. Given the commercial market drivers of two-dimensional optical detector arrays in conjunction with the mirror-like back surfaces of advanced wafers, we believe that transition is already happening. The optical WaferSight™ tool makes this transition simple by combining the production experience of ADE, correlation to AFS industry baseline measurements, and world-class phase-shift interference surface topography precision.

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