Study of oxide quality for scanning capacitance microscope measurements

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Abstract. Although the capability of scanning capacitance microscopy (SCM) for pn junction imaging has been qualitatively demonstrated, quantification of dopant profiles in two-dimensions for pn junctions has proven to be a challenging problem. One reason is that the SCM result is seldom reproducible and this is generally believed to be due to sample preparation technique. In the first part of this work, we made a detailed study of sample preparation methods for SCM measurements. The purpose of the study was to establish an optimum sample preparation technique. Experiments were performed on two known dopant profiles: n type and p type staircase structures with concentration ranging from $10^{14}$ to $10^{19} \text{cm}^{-3}$. These two samples were cross-sectioned and prepared using different oxidation techniques, which caused variations of interface states and oxide quality. We studied the effect of wet oxidation, thermal oxidation, as well as combined wet and thermal oxidation. Experimental parameters: temperature, baking duration and oxidation methods were studied in detail. To evaluate the oxide quality, we measured the flat band voltage change $\Delta V_{FB}$ by sweeping $dC/dV$ vs. voltage in forward and reverse direction (from accumulation to depletion & vice versa). $\Delta V_{FB}$ represents the amount of the oxide trap charge. Since the staircase structure sample has a large doping range, the contrast reversal effect was obvious. We could minimize this effect by using the optimum experimental condition. In the second part, we investigated samples prepared under this optimum experimental condition.

INTRODUCTION

Scanning Capacitance Microscopy (SCM) is a promising scanning probe technique for two-dimensional (2D) doping profiling of semiconductor devices [1]. Although commercial SCM has been developed for several years, it is still not a routine technique for failure analysis and characterization. One of the underlying problems is that the SCM data is always not reproducible. The results are found to vary from time to time even when the same sets of SCM operating parameters were employed. As SCM is very sensitive to the surface conditions (charges, roughness, & etc.), this problem was believed to be have an intimate relationship with the sample preparation technique [2]. Another unavoidable issue is the contrast reversal phenomenon [3][7], where the signal response is non-monotonic with respect to the doping concentration. This is a serious problem with SCM when it is used as a quantitative tool. The contrast reversal phenomenon could be minimized by using an appropriate sample preparation technique.

In sample preparation technique, there are two key aspects: smooth surface finish [5] and the formation of a thin oxide at low temperature. In this study, we investigated various oxidation methods in detail. Parameters studied included time, temperature and oxidation methods. The objective of this study is to establish an optimum oxidation method which produces a stable & homogeneous oxide ideal for SCM scanning.

For gate dielectrics in MOS transistors, the parameter to describe the oxide quality is the trap charge density. An ideal oxide for SCM should also have minimum trap charge and display stable GV
behavior. To evaluate the oxide quality, we used the flat band change $\Delta V_{FB}$ by sweeping $dC/dV$ vs. voltage in forward and reverse direction (from accumulation to depletion & vice versa). The hysteresis behavior indicates charge injection and charge trapping and the amount of flatband shift $\Delta V_{FB}$ can be treated as a measure of the trapped charge density. The trapped charge was believed to have close relationship with electric field, temperature, oxide thickness and sample preparation [4]. In addition to $\Delta V_{FB}$, we also studied the amount of interface trap charge by comparing the full width at half maximum (FWHM) values of the $dC/dV$ versus $V$ curve.

**EXPERIMENTAL**

All the experiments were carried out using a Veeco Digital Instrument Dimension 3000 SPM system. The SCM probes used were commercially available Pt/Ir coated tips. Conventional cross section methods are carried out for all the samples. Pt was sputtered at the backside of the samples to ensure good ohmic contact. The final stage of polishing was done with 0.05 $\mu$m colloidal silica. All the finished samples were obtained with a surface rms roughness of <0.2 nm, and a thin native oxide was expected to be present due to slow oxidation effect of water [6]. Although HF dip was the common method to remove this native oxide, we found that HF dip will cause surface roughening and degradation of SCM signal, especially when high concentration solution (>5 %) is used. And if the sample is an actual device, HF dip will etch away oxide and expose the metal lines, thus introducing unwanted particles. Thus, for all the experiments carried out we did not apply HF dip to the samples.

The SCM measurements were performed at 0.5 Hz and the frequency of ac bias was maintained at 90 kHz. The ac bias value was adjusted to achieve the maximum contrast. Constant $\Delta V$ mode was applied during the scanning. All the $\Delta V_{FB}$ values reported were the average of three readings. The results were obtained across wide doping range.

In the first part of our experiment, we used n and p-type staircase structures manufactured by IMEC. The staircase structure samples are epitaxially grown layers with wide concentration range (p-type concentration ranged from $10^{15}$ to $10^{19}$ cm$^{-3}$ and n type concentration $10^{14}$ – $10^{19}$ cm$^{-3}$). Each concentration step was 5 $\mu$m wide with a 1 $\mu$m buffer layer in between. The two samples were glued together by epoxy to insure the experimental condition is the same for both p and n type samples. We studied the effect of wet oxidation, thermal oxidation, as well as combined wet and thermal oxidation. For thermal oxidation, the samples were baked at 250 °C for 10, 15, 30 minutes and 1 hour under ultraviolet (UV) light irradiation (method A to D). The UV lamp used in the experiment is a high intensity UV light and the wavelength of the UV light is 365 nm. For wet oxidation, samples were immersed in hydrogen peroxide solution at 90 °C for 10 minutes (method E), mixture of hydrogen peroxide and concentrated sulphuric acid solution at 90 °C for 10 minutes (method F) and hydrogen peroxide for 20 minutes at room temperature (method G). In the case of combine wet and thermal oxidation method, sample was immersed in H$_2$O$_2$ at room temperature, followed by baking at 250 °C for 15 minutes with UV irradiation (method H).

In the second part of this study, we prepared a boron implanted sample and an actual MOSFET device using the optimum oxidation method. A large area SCM scan of a transistor was also shown.

**RESULTS AND DISCUSSION**

Figure 1 shows the typical $dC/dV$ curves measured in forward and reverse sweeps, where the probe is held at a fixed point and the sample bias is swept from +5 V to -5 V. A common method adopted to evaluate the SCM oxide quality is to compare the compensating dc flatband offset value [6]. The selection of dc flatband bias is to compensate the influence of the oxide charges. However, the absolute flatband voltage value might not be a good indicator as the value obtained was not stable and not reproducible.

![Figure 1. $dC/dV$ curves measured in forward and reverse sweeps for p type staircase structure at doping concentration $3 \times 10^{16}$ cm$^{-3}$ for (a) method G and (b) method C.](image)
FIGURE 2. $|\Delta V_{FB}|$ obtained for different oxidation methods, A: bake at 250 °C for 1 hr with UV, B : bake at 250 °C for 30 minutes with UV, C : bake at 250 °C for 15 minutes with UV, D: bake at 250 °C for 10 minutes with UV, E: immerse in $H_2O_2$ at 90 °C for 10 minutes, F: immerse in $H_2O_2$ and concentrated $H_2SO_4$ at 90 °C for 10 minutes, G: immerse in $H_2O_2$ for 20 minutes at room temperature, H: first immerse in $H_2O_2$ for 20 minutes then bake for 15 minutes

from day to day [2]. Besides, the dc bias may not reflect the true charge distribution. The ultimate aim of this study is to prepare an oxide layer with minimum oxide trap charge and interface trap charge so that these unwanted charges will not contribute to the SCM signal. Figure 2 shows the $|\Delta V_{FB}|$ obtained for various oxidation methods for different doping range. For dry thermal oxidation, method C ( baking at 250 °C for 15 minutes with UV ) in general has the lowest and relatively stable $|\Delta V_{FB}|$ as compared to method A, B, and D. The selection takes into consideration of both n & p type samples. Thermal oxidation under UV is one of the most common SCM sample preparation technique used and different groups adopted different temperature and baking duration [2][9]. Our experiments showed that although longer baking duration will increase the oxide thickness, it may not necessarily improve the trap charge density. For wet oxidation, method G (20 minutes immersion in $H_2O_2$ at room temperature) has relatively low $|\Delta V_{FB}|$ value as compared to method E & F. Increase temperature and addition of another oxidizing agent may enhance the oxidation, however they do not necessarily produce low and stable $|\Delta V_{FB}|$ value. Combine wet and thermal oxidation ( method H ) was not able to produce an oxide which exhibits low and stable $|\Delta V_{FB}|$ value.

Figure 3 shows the one dimensional SCM signals obtained for the p and n type staircase structures treated with method C & G. For method C, the compensating dc bias value was found to be +0.5 V for p type and ~1 V for n type. Although both oxides produce monotonic response, wet oxidation was found to contain more interface trap charge than dry thermal oxidation method, as shown in Figure 1. Wet oxidation exhibits broader peak shape as compared to thermal oxidation. According to fundamental MOS theory [8], interface trapped charges broaden the peak and smear out the $dC/dV$ curve. Broader peak shape implies higher interface traps.

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FIGURE 3. SCM ID signal obtained for both p and n type samples by using thermal (solid line) and wet oxidation (dash line).

FIGURE 4. Cross sectional TEM Image of the oxide prepared by method C.
thickness of the oxide was measured to be 1.4 nm. Another merit of thermal oxidation is the ease of sample preparation. Wet oxidation will inevitably introduce more contamination as compared to dry thermal oxidation.

In the last part of this article, we demonstrated a few samples prepared by method C. Figure 5 shows the comparison of SCM & secondary ion mass spectroscopy (SIMS) quantitative measurements of a boron implanted sample. The SCM signal was converted into dopant concentration by using the software FASTC2D developed by NIST [10]. The SCM result is in good agreement with the SIMS profile. The missing peak at 0.06 μm in the SCM plot could be attributed to the inactivation of dopants. Figure 6 and 7 show the SCM scan on actual devices prepared by method C. Figure 6 shows the large area

**FIGURE 6.** A general SCM scan of a device prepared by method C. SCM scanning parameters : $V_{ac} = 1$ V, $V_{dc} = 0.5$ V.

**FIGURE 7.** SCM image of 80 nm gate length n-channel MOSFET. SCM scanning parameters : $V_{ac} = 1$ V, $V_{dc} = 0.5$ V.

SCM scan of a transistor. N well region and transistor structures were clearly observed. The image demonstrated that the oxide prepared by method C was homogeneous over a large area scan. Figure 7 shows a magnified view of a 80 nm gate length n channel MOSFET sample. Important features such as source and drain were clearly delineated in the image. The effective channel length was measured to be approximately 29 nm.

**SUMMARY**

In this work, various oxidation methods were evaluated using flatband voltage shift as indicator of oxide quality. The results were compared across wide doping range. Dry thermal oxidation at 250 °C under UV irradiation was chosen to be the optimum oxidation method in terms of low compensating dc bias, minimum oxide trap charges and interface states as well as ease of preparation. We illustrated two samples : one boron implanted sample and one MOSFET device prepared using this oxidation method. To demonstrate the homogeneity of the oxide, a large area SCM scan of a transistor was shown.

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