Development of Metrology at NIST for the Semiconductor Industry

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Abstract. The National Institute of Standards and Technology metrology development for the semiconductor industry and its supporting infrastructure is a broad set of programs directed at many of the critical metrology needs. This paper will give examples of specific projects addressing needs in lithography, critical dimension and overlay, gate dielectric characterization, interconnect materials, and manufacturing support. The paper will emphasize the role collaboration with industry plays in project selection, project success, and transfer to industry.

INTRODUCTION

The National Institute of Standards and Technology, formerly the National Bureau of Standards, has been active in research and development of critical metrology for the semiconductor manufacturing industry and its supporting infrastructure industries since shortly after the invention of the transistor. Early work in the 1960s included determining the nature of second breakdown in bipolar transistors [1], the development of the four-probe resistivity measurement technique [2], and critical metrology for reliable wire bonding [3]. During the 1970s and 1980s the activities expanded to a broad range of metrology developments supporting the semiconductor manufacturing industry.

In 1992 the United States Congress, recognizing the critical role of this industry for the United States economy, created the National Semiconductor Metrology Program (NSMP) initiative to accelerate semiconductor metrology development at NIST. The NSMP is currently funded at $12.5M, and leverages approximately an equivalent dollar value of funds from other sources.

The NSMP is administered by the Office of Microelectronics Programs (OMP), which was established to identify projects of high impact to the semiconductor manufacturing industry, to fund those projects, and to monitor the progress. A further function of the OMP is to serve as broker between the industry and NIST, insuring timely transfer of achievements, and to gather critical industry metrology needs to continuously reprioritize NIST projects.

The NSMP projects are grouped into program clusters; (1) Lithography Metrology, providing critical optical measurements on materials for next generation lithography (NGL) solutions, calibration of NGL sources, and characterization of NGL resist materials; (2) Critical Dimension and Overlay Metrology, delivering measurement techniques and artifacts for length measurements and positioning in the plane of the semiconductor wafer; (3) Thin Film and Junction Metrology, developing vertical dimension metrology, film and junction characterization and artifacts; (4) Interconnect and Packaging Metrology, reflecting the blurring of back-end-of-wafer interconnect processing and packaging processing, this program explores the materials properties, reliability and mutual compatibilities used, (5) Wafer Characterization and Process Metrology, advancing and refining measurement techniques for the ever tightening requirements for wafer processing; (6) Test Metrology, investigating novel techniques for improving high frequency and non-linear circuit testing, and (7) Manufacturing Support, contributing to the necessary infrastructure and standards for manufacturing productivity improvement.
This paper will discuss examples of collaborative activities in several of the program clusters that have yielded significant advances in the knowledge base necessary for the continuing advances in semiconductor manufacturing productivity.

**LITHOGRAPHY METROLOGY**

The continuing aggressive shrinking of device features demands steady improvements in lithography. To date and for the foreseeable future this has been largely accomplished by reducing the wavelength of the exposure radiation, Figure 1. Each succeeding lithography generation presents challenges in characterizing the optical materials, the new resists, and the radiation sources and detectors.

![Figure 1. Moore's Law and Optical Lithography](image)

Two significant collaborations and their outcomes are described below.

**Deep Ultraviolet Lithography**

Beginning in late 1995 a collaborative effort between NIST and MIT Lincoln Labs focused on evaluating the optical properties of the materials for lenses, fused silica and CaF$_2$, and detectors for the 193 nm lithography technology then under early development. Much of this work was funded by SEMATECH, now International SEMATECH (ISMT). MIT Lincoln Labs efforts focused on damage studies to the fused silica, while NIST measured the dispersion and temperature dependence of the index for both fused silica and CaF$_2$. [4] Additionally, detector sensitivity and damage susceptibility were evaluated. Finally, a 193 nm calorimeter was constructed and calibration services were established. [5]

After 193 nm lithography transitioned into advanced development the collaborators moved on to 157 nm lithography issues. Again, NIST contributions included measurements of dispersion and temperature dependence of the index at 157 nm, detector sensitivity and damage, and laser calorimetry. [6,7]

One task requested of the NIST team by ISMT was the measurement of the stress optic coefficients of CaF$_2$. As a precursor to this John Burnett et al. made the significant albeit unanticipated discovery that the intrinsic birefringences of CaF$_2$ and other cubic materials potentially useful for 157 nm optics at the wavelength of interest are large, Figure 2. [8] This discovery has forced major corrections to potential system designs, but was accomplished in time to save equipment manufacturers from costly errors.

![Figure 2. Unit cell of CaF$_2$ showing lobes of intrinsic birefringence](image)

**Extreme Ultraviolet Lithography**

In an activity supporting another Next Generation Lithography technology, NIST has partnered with the EUV LLC and ISMT to support the development of critical metrology for Extreme Ultraviolet (EUV) Lithography. Leveraging its unique calibrated light source, the Synchrotron Ultraviolet Radiation Facility (SURF III), that covers the wavelengths of interest, ~10nm to ~20nm, NIST is performing reflectometry on lenses for EUV and detector sensitivity measurements. [9, 10] An example of preliminary reflectivity measurements at different radii of an
aspheric lens for the EUV Engineering Test System is shown in Figure 3. Note that the peak reflectivities of about 0.2 nm.

**FIGURE 3.** Reflectivity versus wavelength for different radii on an aspheric lens for the EUV Engineering Test System.

One of the significant technical challenges is to protect the EUV lenses from degradation during use. Figure 4 shows early results of degradation of a lens with a silicon-capping layer under various two different pressure water vapor exposures.

**FIGURE 4.** Reflectivity degradation during use of an experimental multiplayer mirror after different exposures to low pressure water vapor.

**CRITICAL DIMENSION AND OVERLAY METROLOGY**

Measurements of features such as gate lengths, conductor widths and pitches, and via hole diameters are critical for successful integrated circuit manufacture. Equally important and challenging is the accurate alignment of successive mask levels, “overlay.” NIST has been and continues to be collaborating with a number of industrial partners on a variety of metrology developments in this area. Three such efforts are outlined below.

**Scanning Electron Microscope-Based Metrology**

**Development Of Nanotip Electron Sources For Critical Dimension Scanning Electron Microscopes**

A significant limitation to the performance of scanning electron microscopes used for critical dimension metrology, CD SEMs, is the size of the electron illumination source. A collaborative effort Hitachi, ISMT, Professor David Joy from the University of Tennessee, and NIST targeted the development of a nanotip with a goal of having a single atom at the tip as the electron emitter source. Early work has produced a method for mounting such tips in working CD SEMs. [11] One such tip is illustrated in Figure 5A. Also shown, in Figure 5B, is an image of the tip taken with a field ion microscope, showing single atom emitter characteristics.

**FIGURE 5A.** SEM image of nanotip end (upper left); optical microscope image of whole nanotip (upper right), nanotip and assembly (bottom).
Another serious limitation of using CD SEMs for imaging objects with insulated regions, such as photomasks in particular, is charging of the portions of the object being imaged. This leads to distortions in the image and can lead to damage through arcing of the object being imaged. A collaborative exploration using an environmental SEM is being pursued by NIST with FEI, ISMT, Texas Instruments and IBM as partners. [12, 13, 14]. The concept is to use a background partial pressure of water vapor in the SEM chamber to neutralize the surface charging with positive ions created by the electron beam interacting with water molecule. Figure 6 illustrates mask images obtained in this manner.

Development of Single Crystal Artifact for Electrical-Based Critical Dimension Metrology

Calibration of critical dimension measuring instruments, such as CD-SEMs and atomic force microscopes (AFMs), is essential for process control. One approach being developed by NIST, with extensive collaboration by VLSI Standards Sandia National Laboratories, and International SEMATECH, is to create single crystal silicon artifacts that can be measured electrically so as to extract electrical linewidths and can be calibrated with high accuracy using high-resolution transmission electron microscopy [15]. The use of lattice plane selective etching results in highly planar vertical features. Figure 7 shows a schematic of the artifact structure, and Figures 8A and 8B shows a cross section of a single crystal structure for measuring the actual width using HRTEM at low magnification and high magnification, respectively. Under high magnification it is possible to count the lattice planes across the artifact, and from the known lattice constant of the silicon, obtain an accurate measure of the width.
FIGURE 8A. Low magnification TEM image of cross section of a single crystal artifact for measurement by HRTEM.

Palladium (encapsulate for HRTEM) SiO$_2$ Silicon Lattice (note presence of fringes)

FIGURE 8B. High resolution HRTEM of edge of structure in Figure 8A, showing lattice planes of single crystal.

Figure 9 is a plot of the electrical linewidths of features plotted versus the physical linewidths based on HRTEM measurements. Currently artifacts with widths as narrow as 60 nm with uncertainty in width of 2.5 nm can be fabricated. Additional work is underway to reduce the uncertainty.

FIGURE 9. Electrical linewidth versus physical linewidth obtained using HRTEM.

THIN FILM AND SHALLOW JUNCTION METROLOGY

Metrology in the vertical dimension is just as critical as metrology in the surface plane of the semiconductor wafer for successful integrated circuit manufacture.

Gate Dielectric Metrology

Early work at NIST led to the fabrication of Standard Reference Material, SRM™, films of SiO$_2$ on silicon [16]. More recently NIST has collaborated with a number of organizations in developing the necessary metrology for fabricating advanced gate dielectrics. The Front End Processing Center, established in 1998, received funding from the Semiconductor Research Corporation, and ISMT. The funding supported advanced gate dielectric research at a number of universities. NIST participated by providing metrology development and measurements. One example of metrology development is a comparison study for different gate dielectric thickness measurement techniques, Figures 10 and 11. [17]

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1 Now International SEMATECH.
FIGURE 10. Thickness value comparison for High Resolution Transmission Microscope, Scanning Transmission Microscope, and Capacitance-Voltage techniques on nominal 2nm SiO$_2$ films.

FIGURE 11. Thickness values from Spectroscopic Ellipsometry measurements and various analysis models and Capacitance-Voltage measurements.

An example of materials systems being investigated for next generation gate dielectrics is the Tauc plot analysis for hafnium aluminum oxide films of various compositions shown in Figure 12. The Tauc plot is a measure of the amorphous material band-gap. The kinks in the plots indicate at high absorption indicate the presence of higher energy band transitions. [18].

FIGURE 12. Tauc plots for determining band-gaps of HfAlO films with different compositions from analysis of ellipsometrically determined dielectric function.

INTERCONNECT AND PACKAGING METROLOGY

Interconnect Low-k Dielectric Metrology

A significant issue in the International Technology Roadmap for Semiconductors a few years ago was a concern that the dielectric constants of the low-k materials being considered for interconnect could be frequency dependent in the frequencies of interest. A collaborative activity between NIST and ISMT evaluated a number of low k materials and determined that frequency dependence of the dielectric constants is not a problem. NIST designed strip line test structures, Figure 13, and ISMT fabricated the structures using low-k materials from a variety of sources. NIST then performed the measurements in the frequency range of 1GHz to 40GHz, Figure 14 [19].

2 A Tauc plot is (absorption coefficient x photon energy)$^{1/2}$ versus photon energy.
There are approximately 40 projects at NIST supporting metrology for the semiconductor manufacturing industry and its supporting infrastructure industries. Almost all of these projects involve collaborative work with industrial, academic, or consortia partners. Collaborations allow NIST researchers critical information on relevant problems, access to exploratory materials, fabrication of metrology artifacts, and robust communication channels to the industry customers. For up to date information on ongoing metrology projects supporting the semiconductor manufacturing industry the following website is useful.

http://www.eeel.nist.gov/omp/

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