Low Frequency Noise sensitivity to technology induced mechanical stress in MOSFETs

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Abstract. A detailed experimental investigation of 1/f noise in MOSFET devices as a function of technology-induced mechanical stress is presented. Strain in the channel region is obtained by the Shallow Trench Isolation (STI) technique. Both n- and p-MOS have been considered inside the present study. An increasing of 1/f noise intensity with the increasing intensity of mechanical stress has been detected for p-channel transistor. A tentative explanation of this experimental finding has been proposed.

Keywords: 1/f noise, MOSFET, strain, and mechanical stress.

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INTRODUCTION

The possibility to rule the inter-atomic distance in the silicon lattice constituting the “habitat” for the MOSFET channel represents a key element for next generation CMOS technologies. In fact, it has been shown that strained-silicon can significantly improve the MOSFET driving capability. Hereof, today’s technology challenge plays on the capability to introduce the desired mechanical stress in the channel of device considering low-cost process modifications. With reference to the present work, a built-in biaxial compressive stress is induced on the device active area by the Shallow Trench Isolation (STI) technique that became a must for the CMOS technology scaling down below the 0.25µm node. Hereto, variations in MOSFETs electrical behavior are observed when channel width and length are maintained constant and only the distance from STI oxide is modified. Therefore, the transistor electrical performances show a layout dependence that was ignored in LSI technologies and new layout parameters (Sa and Sb in Fig.1) in addition to W and L must be introduced in order to describe the MOSFET electrical behavior.

The main electrical parameter changing with the mechanical stress of the device active area is the low-field mobility together other ones related with: $g_m$, $I_{DSAT}$, $R_{ON}$...

A dichotomy in the low-field mobility trend as a function of mechanical stress intensity has been observed between N- and P-MOSFETs: it decreases in the first one, while in the second ones it increases with higher stress [2]. The variation ranges observed in the examined technology are around -10% for N-MOS and 25% for P-MOS between the more stressed and more relaxed structure.
Our paper deals with the question if also 1/f noise intensity could show any layout dependence. Some spot studies have just been presented [3]. However, up to date, any complete dedicated work about the layout dependence of 1/f noise is lacked at the knowledge of authors. Later on, we discuss the question with the support of a number of experimental data on both N- and P-channel MOSFETs fabricated in 90nm Flash Memory Technology.

**EXPERIMENTAL DATA**

In figure 2, we show the experimental values of the normalized Noise Current Power Spectral Density @ 1Hz as a function of the drain current for P-MOSFET structures with \( SA=SB=0.3\, \mu m \) and \( SA=SB=3.6\, \mu m \). Measurements of noise drain current power spectral density have been carried out at wafer level by using an EG&G 5182 low noise amplifier and a HP 35665A Dynamical Signal Analyzer, while the dc MOSFETs characterization has been performed by means of a HP 4155 Parameter Analyzer. MOSFETs were biased in linear region with \( V_D=50mV \). The frequency range we have considered was from 1 Hz to 1 KHz and the nominal MOSFET geometry was \( W=10\, \mu m \) and \( L=0.18\, \mu m \). With a so wide device the measured noise spectra normally showed a 1/f\(^a\) noise spectrum with \( \alpha \) in the 0.8-1.2 range. Degradation in low-frequency noise device performance has been found in the overall gate bias range for device with the minimum \( Sa \) value (maximum mechanical stress). This can be observed, in particular, in the region close to MOSFET threshold (\( I_D@V_{TH} \)) where the correlated number fluctuations are the main low frequency noise source, but also at higher drain current where the correlated mobility fluctuations play an important role. Beneath it has been recently reported a dependence of \( P_b \) interface defects density by the applied mechanical stress [4], we have just noticed that in our case no interface traps density variation is induced by mechanical stress since we did not observe any modulation in the subthreshold slope [5]. Also a qualitative analysis
FIGURE 2. Normalized Current Power Spectral Density as a function of drain current for both the P-MOSFETs with minimum active area size (SA=0.3µm) and the larger one (SA=3.6µm).

Since our experimental data exclude any justification in terms of interfacial effects as reason of the observed difference in 1/f noise intensity, we look for a possible explanation in the modification of the silicon electronic properties as a function of mechanical stress. The lift of the twofold degeneracy in Γ point of the valence band and the energy shift of the bottom of conduction band are the main consequences of mechanical stress. The physical parameter that is responsible for the low-field mobility modulation with strain, at least at small stress intensity, as it occurs in our devices, is the effective mass variation due to the strain-altered band structure [6]. The effective mass variation can affect the noise fluctuations produced by the trapping-detrapping of carriers. To clarify this point, let us recall that a potential fluctuation extends typically in the Debye screening length range, which can be approximated for a 2D-electron gas with the expression [7]:

\[ \text{PSD } S_{I_D}^2 [1/\text{Hz}] \]
\[ L_s = \sqrt{2} \frac{\varepsilon_s kT}{qQ_s} \sim \frac{1}{m} \]

where \( \varepsilon_s \) is the dielectric constant, \( k \) the Boltzmann constant, \( T \) the temperature, \( q \) the electron charge, \( Q_s \) the charge density in the transistor channel and \( m^* \) the effective mass.

We note that \( L_s \) depends on the electronic properties of material through the static dielectric constant: \( \varepsilon_s \). This quantity increases with a hyperbolic trend when \( m^* \) decreases. So, we suggest that the observed noise increasing in P-MOS devices with stress could be ascribed to the dielectric properties modification of the p-channel inducing a stronger response of carriers to the trapping-detrapping events. On the contrary, the low-field mobility variation in N-MOS devices is associated to the conduction band repopulation without any energetic dispersion curve modification. This could be a further reason justifying why we did not observe any noise intensity modulation with stress in N-MOS devices.

**CONCLUSIONS**

We have investigated the effect of mechanical stress on 1/f spectra of MOSFET devices. Mechanical stress modulates the intimate electronic properties of silicon changing its own band structure. An interpretative key that correlates the variations of 1/f noise intensity with the strain-induced electronic band modifications has been proposed. Summarizing, we suggest that the analysis of low frequency noise on MOSFETs, beyond the obvious interaction between carriers and SiO\(_2\) traps, is also linked to the deeper semiconductor properties. In this scenario, the effective mass lowering in next generation strained silicon is expected to produce an increasing contribution to low frequency noise.

**REFERENCES**