Can 1/f noise in MOSFETs be reduced by gate oxide and channel optimization?

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Abstract. This contribution addresses several important topics about 1/f noise in MOSFETs for the 65 nm node. We show that a plasma nitridation technique can significantly improve the 1/f noise performances of the device providing that the insulator is thick enough. This result is explained by correlating the 1/f noise magnitude and the nitrogen concentration profile within the gate oxide. In a second time we investigate the effect of dopant dose and species in the substrate as well as the influence of channel orientation (110) and (100).

Keywords: MOSFET, 1/f noise, nitridation, substrate orientation

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INTRODUCTION

Many innovations are required to meet the increasingly aggressive ITRS specifications for sub-100 nm MOS technologies. The introduction of high-κ dielectrics or new device architectures are up to the 65 nm node postponed with the use of optimized oxynitride, stress engineering or alternative substrate orientations. Unfortunately some of these technological novelties, mainly used to enhance the “digital” Ion/Ioff figure of merit, are not suited for some analog parameters like Low Frequency Noise (LFN) or even for reliability issues. A good example is the well-known degradation of the 1/f noise and NBTI (Negative Bias Temperature Instability) observed with nitrided oxide devices [1], [2]. In this paper we first discuss the potential benefit in matters of noise of a plasma-based nitridation technique over a conventional thermal method. In a second time we investigate the effect of dopant dose and species in the substrate for both n and p-MOSFETs devices. Finally, we will compare the noise performances of transistors processed with different channel orientations, (110) versus (100).

EXPERIMENTAL

All experiments were performed on n and p-MOS devices issued from a 65 nm CMOS technology. DC characteristics were obtained with a HP4155A semiconductor analyzer and low frequency noise measurements were done directly on wafer using an FFT Dynamic Signal Analyzer (HP35670A) and a low noise current-to-voltage

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amplifier (EG&G 5182). The Device Under Test (D.U.T) was biased using 12V filtered batteries in order to avoid any external perturbations.

All the measurements were systematically corrected from the noise and gain of the I/V amplifier. Only large geometry devices were investigated (W/L = 10/5 or 10/3 µm) so as not to be disturb with generation-recombination or even RTS noise. Some experimental drain current noise Power Spectral Densities (PSD) are illustrated in FIGURE 1 between 10 Hz and 100 kHz for p-MOS devices with different gate-to-source voltages.

RESULTS AND DISCUSSION

We shall first discuss the gate oxide nitridation influence. Usually, the nitrogen atoms are incorporated within the insulating layer of the MOS device via a thermal anneal under an NO ambient. However, a plasma-based method has recently shown several advantages over the classical thermal technique both in terms of gate leakage current and reliability [3]. We have compared the noise performances of n and p-MOS transistors processed with these two nitridation methods. Their relative 1/f noise level at f = 10 Hz is plotted in FIGURE 2.

We can observe a drastic impact on the 1/f noise level of both n and p-MOS transistors. This result can be explained considering that, on the one hand, nitrided oxide device are reportedly noisier than pure oxide device. Given that the 1/f noise is linked to the oxide trap density near the SiO₂/Si interface, nitrogen must induce extra
traps. On the other hand, the nitrogen concentration profiles obtained with the two techniques are quite different [4]. With a plasma process most of the nitrogen is segregated closed to the top interface between the poly and the oxide while in the case of a thermal process N atoms pill up at the SiO₂/Si interface (see FIGURE 3, left plot). For a given oxide thickness, a plasma nitridation will result in a lower nitrogen dose at the interface with the channel, and then in a lower 1/f noise level.

![FIGURE 3: Nitrogen profile for plasma (DPN) and thermal (RTN) nitridation [left plot] - Hooge constant for plasma nitrided p-MOS transistors with different oxide thickness [right plot].](image)

The benefit of such technique should then be as much appreciable as the gate oxide is thick since the nitrogen dose at the interface will decay. This assumption is confirmed in FIGURE 3 (right plot) where we have reported the Hooge constant of plasma nitrided p-MOS transistors with different oxide thickness. The noise obtained with a 5 nm oxide is comparable to what has been measured on a pure SiO₂ device. This result is of particular interest for analog circuits which are designed with the thickest oxide transistors of a given technology platform.

We have also investigated the substrate optimization influence in two ways. First, we have compared the 1/f noise of transistors processed with different dopant dose and species (Indium/Boron for n-MOS and Arsenic/Phosphorus for p-MOS) as described in the next table.

| TABLE 1 : Substrate dopant and associated dose (x10⁻¹² cm⁻²) |
|-----------------|----------------|
|                 | n-MOS          | p-MOS           |
| Boron 3 / Indium 5 | Arsenic 7 / Phosphorus 10 |
| Boron 4 / Indium 3 | Arsenic 8 / Phosphorus 6 |
| No Boron / Indium 5 | Arsenic 10 / No Phosphorus |

In a second time we studied the noise of devices with two distinct channel orientations, (110) and also (100). The latter leads to an enhancement of the drive current (~15%) for p-MOS devices leaving unchanged the n-MOS performances [5]. This particular orientation is obtained by a 45 degrees rotation of the wafer notch from its usual position. All results are reported on the following FIGURE 4 and FIGURE 5 respectively from weak to strong inversion.
FIGURE 4: Normalized 1/f noise level at $f = 10$ Hz for n and p-MOS transistors ($t_{ox} = 5$ nm) with various bulk dopant concentrations.

FIGURE 5: Normalized 1/f noise level at $f = 10$ Hz for n and p-MOS transistors ($t_{ox} = 5$ nm) with (110) and (100) channel orientation.

We can observe that there is no significant impact neither of the dopant dose tuning nor of the channel orientation for both kinds of MOS transistors. Concerning the substrate doping, this result is rather consistent with the number fluctuation model or even with the correlated model. Concerning the results about the channel orientation, one could argue that the interface states should be different. However, the density of slow states lying a few nanometers from the interface and which are of interest for 1/f noise, might not vary significantly.

**CONCLUSION**

We mainly demonstrated that shifting away the nitrogen peak from the Si/SiO₂ interface can substantially lower the 1/f noise level of n and p-MOS devices. On the contrary, the channel orientation or doping has no appreciable influence.

**REFERENCES**