Gate and drain low frequency noise in HfO2 NMOSFETs

T. Nguyen1, M. Valenza1, F. Martinez1, G. Neau2, J.C. Vildeuil2, G. Ribes2, V. Cosnier2, T. Skotnicki2, M. Müller3

1CEM2 – UNIVERSITE MONTPELLIER II – UMR CNRS 5507
Place E. Bataillon, 34095 Montpellier Cedex 5, France
2ST Microelectronics, 850 rue Jean Monnet, F-38926 Crolles Cedex
3Philips Semiconductors, 850 rue Jean Monnet, F-38926 Crolles Cedex

Abstract. Gate and drain current noise investigations are performed on nMOS transistors with HfO2 gate oxides. The drain noise magnitude allows extraction of the slow oxide trap density $N_t(E_F)$ ranging from 3 to 7 $10^{19}$ eV$^{-1}$ cm$^{-3}$. These values are about 50 times higher than for SiO2 dielectrics. The 1/f gate current noise component is a quadratic function of the gate leakage current. The gate noise parameter $K_{GC}$ is about $2 \times 10^{-17}$ m$^2$, whereas, for SiO2 dielectrics this gate noise figure of merit is about $10^{-19}$ m$^2$.

Keywords: NMOSFETs, high–k, 1/f noise, drain noise, gate noise.

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INTRODUCTION

The improvement of speed and chip shrinkage of integrated circuits are achieved by scaling down the thickness of the SiO2 gate dielectric. However, as oxide thickness is reduced, SiO2 reaches its ultimate scaling limit such as high tunnelling current and reliability concerns. In order to attenuate this gate current, high-k dielectrics are candidates to replace SiO2. Various high-k dielectrics have been reported such as HfO2, ZrO2, Al2O3, Ta2O5. HfO2 gated transistors have shown very encouraging gate leakage reduction, but they present a degraded mobility when non strained Si MOSFETs with a high-k dielectric are achieved [1]. Moreover, instabilities of threshold voltage due to lack of oxygen are observed. The low mobility value is often linked to a high density of traps located in the bulk or at the interface. The interface trap density can be extracted by charge pumping analysis or by 1/f noise measurements. However, the involved traps are not the same. In the first case, fast trap density is extracted, whereas in the second case, slow trap density is extracted. In this contribution, we present gate and drain current noise investigations performed on nMOS transistors with HfO2 gate oxide and low EOT value.

DEVICES UNDER TEST

The high-K stack consists of a 8Å-thick HfSiOx capping layer on a 30Å thick HfO2 deposited on 10Å interfacial oxide giving a 14Å EOT. A NH3 post deposition...
anneal at 800°C has been used to suppress the interfacial layer growth during the process. The gate electrode is poly-silicon. The transistors have individual gate and drain electrodes. Devices under test had a width $W = 10 \, \mu m$ and a length $L$ between 0.18 to 10 µm.

As shown figure 1, high-k oxide allows reduction of the gate leakage current of 3 decades with respect to the SiO$_2$ reference with same EOT. However, the mobility is degraded, partly explained by the nitrogen incorporation into the High-K and interfacial oxides layers, the obtained mobility is around 55 cm$^2$V$^{-1}$s$^{-1}$, while for the SiO$_2$ reference the mobility is around 190 cm$^2$V$^{-1}$s$^{-1}$.

**NOISE INVESTIGATIONS AND DISCUSSION**

Gate current and drain current noise measurements have been performed. Concerning drain noise spectra, the main component was 1/f noise, whereas concerning gate noise spectra Lorentzian component associated to Random Telegraph Signal (R.T.S) fluctuations and 1/f component were observed. In this paper we focus our investigations on 1/f noise.

**Drain Current noise**

To deduce noise figure of merit drain current noise measurements have been performed at $V_{DS} = 25$ mV and $V_{GS}$ varying up to 1.2 V, i.e. from weak to strong inversion. Figure 2 shows the variations of the normalised drain current noise $W_{eff}^{L_{eff}} S_{ID} / I_{D}^2$ at $f=1$ Hz as a function of $I_D$ for different gate lengths. The normalised noise level is found to level off in weak inversion and decrease as $I_D^{-2}$ in strong inversion. This is in good agreement with carrier number fluctuation theory $\Delta n$ [2,3]. Moreover, correct scaling of the area normalised noise magnitude is obtained compared with the theoretical variation, that is, $S_{ID} / I_{D}^2 \propto (W_{eff}^{L_{eff}})^{-1}$ [2,3]. In figure 2, we have also reported the evolutions of normalised drain current noise obtained in SiO$_2$ reference n-MOS devices with same EOT. It appears clearly that high-k devices are more noisy. The slow oxide trap density, which is used as figure of merit, has been extracted. We obtain $N_t(E_F)$ between 3 and $7 \times 10^{19}$ eV$^{-1}$cm$^{-3}$ which is about 50 times higher than for SiO$_2$ dielectrics (see figure 3), but in the same range than results found by Simoen et al.[4] in HfO$_2$ devices with EOT of 2 nm. Simoen et al. [5] have reported a correlation between the increase of trap density and mobility degradation. Our results confirm that the low mobility values obtained for high-K devices is linked to the high magnitude of trap density.

**Gate Current noise**

Gate current noise measurements have been performed at $V_{DS} = 25$ mV and 1V for different $V_{GS}$ values. The associated typical spectra are reported figures 4 and 5,
respectively. An accurate I-V study shown that at V_DS=25 mV, the gate current is predominantly a leakage current flowing between gate and channel, I_g. Whereas, at V_DS=1 V, the gate current is predominantly leakage current flowing between drain overlap and gate (I_{gd0}) for V_GS<0.6V and gate to channel current for V_GS>0.6 V (see figure 6). As shown figure 4, at V_DS=25 mV, the low frequency noise is mainly 1/f. Whereas, at V_DS=1 V and V_GS<0.6V we observe mainly Lorentzian components associated to R.T.S fluctuations (see figure 5).

Concerning gate to channel current noise, the 1/f component is a quadratic function of the gate leakage current following the law : S_{IG} (f) = \frac{K_{GC}}{f} \frac{I_G^2}{W_{eff} L_{eff}}. We obtain K_{GC} about 2 10^{-17} m^2 for high-k, whereas for SiO2 reference with same EOT this gate noise figure of merit is about 10^{-19} m^2.

Concerning measurements at V_DS=1 V, it appears clearly that the noise associated to off-gate current (V_GS=0V) is two decade higher than the one associated to on-gate current (V_GS=1.2V) (figure 5). The on-gate current noise is always lower than gate to drain overlap current noise, even when this gate to drain overlap current is lower than on-gate current (figures 5 and 6).

CONCLUSIONS

Gate current noise and drain current noise in HfO2 gated nMOS transistors have been studied.

Drain noise measurements were performed at V_DS=25 mV from weak to strong inversion. Noise levels variations agree with the carrier number fluctuation theory. The oxide trap density N_t(E_F) was found 50 times higher than for SiO2 dielectrics.

Gate noise measurements were performed at V_DS=25 mV and 1 V. Two paths are well drawn. One between the gate and the channel and one between the gate and the drain region. For gate to channel current 1/f noise is observed, and noise levels variations follow a quadratic current variation inversely proportional to the gate area, characterised by flicker noise parameter K_{GC}. This parameter was found to be in the order of 2 10^{-17} m^2 which is two order of magnitude higher than for SiO2 dielectrics. For gate to drain overlap current mainly R.T.S noise is observed. The gate noise at I_{off} state(V_GS=0V,V_DS=1V) was higher than the gate noise at I_{on} state (V_GS=1V,V_DS=1V).

REFERENCES


**FIGURE 1.** Gate current density versus $V_{GS}$ for SiO2 and HfO2 dielectrics for nMOSFETs.

**FIGURE 2.** Normalised drain current noise versus $V_{GS}$ for SiO2 (black dot) and HfO2 dielectrics for nMOSFETs.

**FIGURE 3.** Oxide trap densities $N_{t}(E_F)$ in n-MOS devices for different technologies; open symbols for pure oxide and solid symbols for nitrided oxide.

**FIGURE 4.** Gate current spectral density as a function of the frequency at various gate biases for an high-k device W/L=10/0.4 at $V_{DS}=25$ mV.

**FIGURE 5.** Gate current spectral density as a function of the frequency at various gate biases for an high-k device W/L=10/0.4 at $V_{DS}=1$ V.

**FIGURE 6.** Drain, source gate and substrate currents versus gate voltage for an high-k device W/L=10/0.4 at $V_{DS}=1$ V.