Nonlinear Noise in SiGe Bipolar Devices and its Impact on Radio-Frequency Amplifier Phase Noise

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Abstract. The nonlinear behavior of different microwave SiGe bipolar transistors has been studied and models have been extracted. The phase noise of an amplifier is computed, taking into account the microwave additive noise floor and the up-converted 1/f noise. The simulation technique is a combination of different approaches available in a commercial CAD software. Theoretical results are then compared to the experiment.

Keywords: nonlinear modeling, phase noise, SiGe HBT, transistor oscillator  
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INTRODUCTION

Amplifier phase noise is the main cause of phase noise in microwave oscillators. Inside the cavity bandwidth, the amplifier phase noise is simply converted into oscillator frequency noise [1]. Two mechanisms are responsible for the amplifier phase fluctuations: the conversion of the transistor low frequency (LF) noise by device nonlinearities, generally of 1/f shape; and addition of high frequency (HF) noise [4]. Improving amplifier phase noise directly improves the oscillator frequency noise. Firstly, amplifier’s noise is easier to simulate an open loop circuit than a closed loop circuit. Secondly, the amplifier phase noise measurement is possible from the linear behaviour up to strong compression, whereas the oscillator can only be measured in compression. Studying phase noise on a large input power range is the best way, to check the validity of a modeling approach [2] and thus to understand the noise conversion mechanisms. Moreover an amplifier is free of the phase loop effect.

This paper focus on the phase noise modeling of different commercially available microwave silicon-germanium (SiGe) bipolar transistors (TB1 and TB2). The transistors have first been modeled using a conventional large signal model extraction technique. Then the noise sources have been added to the nonlinear device model and the phase noise has been simulated. The interest of an original two stages amplifier topology to get simultaneously low phase noise and high gain performance is finally pointed out.
NONLINEAR MODELLING AND NOISE MODELLING

Our models are based on the classical Gummel-Poon model [3]. They are extracted from DC characterization and S parameters measurements. Nonlinear validation is performed using output power versus input power data at different harmonic frequencies. The good agreement between the measured and the simulated values allows us to go further in complexity, adding the noise parameters to the model.

Phase noise in a transistor, or an amplifier, is managed by two different processes [4]. The first one is the conversion close to the carrier of the device LF noise. The second one is the addition of the HF noise. These two processes have fundamentally different behaviors. The LF noise conversion is a multiplicative process, which means that the noise level follows the signal level. The HF noise is additive, and has thus a minimum impact on phase noise at the high signal level. Both noise processes have to be taken into account in order to accurately simulate an amplifier phase noise. It is therefore essential to be able to model these two phase noise contributions in a device, and also to minimize one or the other noise, according to the application goal. The HF noise addition is probably easier to describe than the LF noise conversion. At low input power, it can be calculated using equation (1).

\[ S_n(f) = \frac{FkT}{P_{in}} \]  

where F is the amplifier noise figure, k the Boltzmann constant, T the absolute temperature and Pin the amplifier input power. However, some problems appear at high input power. A nonlinear noise figure must be defined because of device compression [4].

Identifying and locating the LF noise sources in a transistor, is a more difficult task. Moreover, the noise source itself can be affected by the RF large signal. In other words, the noise does not depend only on the transistor DC conditions [5]. How to take into account this effect in an equivalent circuit approach is still a debated subject. Each noise source can be associated to a nonlinear element of the equivalent circuit [2], or considered itself as nonlinear [6]. However, an equivalent model is by no means an accurate representation of devices physics which can only be fully described using physical modeling [5] or microscopic models. Unfortunately, these models cannot be used directly to compute the noise in a complex system like an oscillator.

Our approach of the problem is a little different. It uses an extrinsic LF noise source approach, but the dependence of this noise source on the large signal amplitude is taken into account. To this purpose, the device LF noise is measured under large signal conditions and varying the RF power. Even if this approach is not totally rigorous, it has already proven its efficiency [7]. Two extrinsic noise sources are generally considered in a classical bipolar transistor model: the base voltage noise source and the base-emitter current noise source, the latter having a very strong contribution on phase noise. However, this contribution can be minimized using a low impedance bias network [7]. The current noise being cancelled in this way, the characterization is made on the base voltage noise source only. The measured data and the LF noise model for a SiGe bipolar device are shown in FIGURE 1. A sudden increase of the noise is observed when the device enters into compression.
The following equation has been used to model this behavior:

\[
S_v(P_{in}) = S_v^{1/f}(P_{in}) + k_1(P_{in})S_v^{\text{floor}}(P_{in}) + k_2(P_{in})
\]

(2)

\(S_v^{1/f}\) and \(S_v^{\text{floor}}\) being the spectral power densities (respectively 1/f and noise floor) measured on the quiescent device and \(k_1(P_{in})\), \(k_2(P_{in})\) two empirical functions of the microwave power \(P_{in}\) (FIGURE 2).

Adding this RF power dependent noise source to the transistor nonlinear electrical model allows us to simulate both amplifier and oscillator phase noise at strong compression levels.

**PHASE NOISE SIMULATION AND OPTIMIZATION**

The above described model is implemented on a commercial software: Agilent ADS. Various approaches may be used on ADS to simulate phase noise. However, many of these tools are restricted to oscillator simulation ("pnmx" and "pnfm") and special techniques must be implemented to simulate amplifier phase noise (particularly the 1/f contribution). A simple but efficient one is the quasi-static perturbation technique, which consists in introducing a small static voltage (or current) shift to evaluate the effect of a LF voltage (or current) noise on the phase of the microwave signal through the amplifier. The conversion noise has been simulated using this technique and the ADS nonlinear noise tool has been used to compute the additive HF noise floor. FIGURE 3a and 3b demonstrate that a good agreement between measurements and simulation has been obtained. The device residual phase noise is measured using previously described techniques [4] [7]. The relative increase of the phase noise floor at low carrier level is typical of an additive noise. The 1/f phase noise is almost constant at high power level, and increases at very low input power. With such a modeling approach, it is possible not only to predict an oscillator phase noise, but also to optimize both the amplifier phase noise and the oscillator phase noise. Considering a 6 dB losses coupling \(Q_L = Q_0/2\), which is an optimum coupling both for additive phase noise [8] or conversion phase noise [7] contributions in a single stage amplifier oscillator, the necessary amplifier small signal gain should be about 9 dB to take into account circuit losses. This gain requirement is easy to
fulfills in the low microwave range, but becomes more difficult to reach at higher frequencies (10 GHz). The transistor small signal gain matching is indeed one of the worse loading conditions to get a low amplifier phase noise [9]. Another important application is the one of cryogenic sapphire oscillators. In this case, the resonator is reached through long cables, inducing extra losses, and the use of an amplifier featuring a small signal gain of at least 14 dB becomes mandatory. We found that, both for 10 GHz applications and for cryogenic 5 GHz to 7 GHz applications, it was impossible to get phase noise optimized results staying on a single stage amplifier design. Therefore, a low phase noise two stages amplifier has been designed and features very promising performances [10].

**FIGURE 3 (3A & 3B)**: Measured (left) and simulated (right) @3.5 GHz phase noise of a bipolar transistor (TB2) loaded onto 50 Ω, input power levels from -20 dBm up to 0 dBm

**CONCLUSION**

A modeling technique, dedicated to microwave amplifier phase noise calculation, has been presented. Different issues to CAD calculation of the two main noise contributors to phase noise in silicon bipolar transistor amplifiers have been presented. The nonlinear effects, which change both the device 1/f converted LF noise and the device HF noise figure are taken into account in our model. This model compares well to the experiment on various single stage microwave amplifiers. It is also used to optimize a two stages amplifier dedicated to cryogenic sapphire oscillator applications.

**REFERENCES**