CMOS ADC & DAC Principles

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ADC & DAC

Output code

Analog output (wrt $V_{ref}$)

Ideal

Analog input (with respect to $V_{ref}$)

Ideal

Input code

Willy Sansen 10-05 203
DACs Resolution

Analog output (wrt $V_{\text{ref}}$)

$$V_{\text{OUT}} = V_{\text{REF}} B_{\text{IN}}$$

$$= V_{\text{REF}} \left( \frac{b_1}{2^1} + \frac{b_2}{2^2} + \frac{b_3}{2^3} + \cdots + \frac{b_N}{2^N} \right)$$

$$V_{\text{LSB}} = \frac{V_{\text{REF}}}{2^N}$$

Resolution N

$b_1$ is Most Significant bit (MSB)

$b_N$ is Least Significant bit (LSB)

Input code: 000, 001, 010, 011, 100, 101, 110, 111

D to A converter

Ideal

0

1
The quantisation error of a DAC

\[ P_{\text{Noise}} = \frac{1}{\Delta} \int_{-\Delta/2}^{\Delta/2} \varepsilon^2 \, d\varepsilon = \frac{\Delta^2}{12} \]

\[ V_{\text{ptp}} = 2^N \Delta \]

\[ P_{\text{Signal}} = \frac{V_{\text{ptp}}^2}{8} \]

\[ \text{SNR} = \frac{3}{2} \cdot 2^{2N} \]

\[ \text{SNR} = 6N + 1.76 \text{ dB} \]
Static specs: INL & DNL

Differential Nonlinearity: \( \text{DNL} = Y_{\text{OUT}}(B) - Y_{\text{OUT}}(B-1) - 1 \text{ LSB} \)
Integral Nonlinearity: \( \text{INL} = Y_{\text{OUT}}(B) - Y_{\text{OUT},\text{id}}(B) \)
Dynamic specifications

- Glitch
- Clock-feedthrough
- Slew rate
- Settling time
- DNL

Y_out vs. Time

Ideal response vs. Non-ideal response
Spectral content: Spurious free dynamic range

dB

Frequency (Hz)
Output SNR versus input Signal

Limited by distortion
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Resistor string DAC

For 10 bit:
1023 resistors and 1024 switches !!

Resistive matching !!
Binary weighted resistor DAC

One Resistor and Switch per bit
No guaranteed monotonicity (glitches !)
R-2R DAC

Smaller area in Resistors!
3-bit charge redistribution DAC

Better capacitive matching!

Phase $\Phi_1$
4-bit Current steering DAC

Resolution limited by Mismatch in the Current sources!

Glitches!
The Binary and thermometer codes

<table>
<thead>
<tr>
<th>Decimal</th>
<th>Binary</th>
<th>Thermometer Code</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$b_1$ $b_2$ $b_3$ $d_1$ $d_2$ $d_3$ $d_4$ $d_5$ $d_6$ $d_7$</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>0 0 0 0 0 0 0 0 0 0</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>0 0 1 0 0 0 0 0 0 1</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>0 1 0 0 0 0 0 0 1 1</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>0 1 1 0 0 0 0 1 1 1</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>1 0 0 0 0 0 1 1 1 1</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>1 0 1 0 0 1 1 1 1 1</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>1 1 0 0 1 1 1 1 1 1</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>1 1 1 1 1 1 1 1 1 1</td>
<td></td>
</tr>
</tbody>
</table>

Monotonicity guaranteed!
Thermometer-code Current steering DAC

All current sources are of equal value.
Binary, unary, segmented DAC

\[ \sigma (\Delta I) = \]

- **Binary**
  \[ \sqrt{2^N - 1} \frac{\sigma(I)}{I} \text{ LSB} \]

- **Unary**
  \[ \frac{\sigma(I)}{I} \text{ LSB} \]

- **Segmented**
  \[ \sqrt{2^{B+1} - 1} \frac{\sigma(I)}{I} \text{ LSB} \]

Van den Bosch, ..., Kluwer 2004
\[ \frac{\sigma(I)}{I} = \frac{1}{2C \sqrt{2^N}} \]

\( C \approx 6.2 \times 10^{-4} \)

for INL\_yield = 90%

Yield =

- 10 %
- 50 %
- 90 %
- 99.7 %

Van den Bosch, .., Kluwer 2004
Switching schemes

is centroide!

Van den Bosch, .., Kluwer 2004
Miki, JSSC Dec.86, 983-988
INL error for different switching schemes

Hierarchical symmetrical scheme (type A)
DAC Design: Static Accuracy

INL\_yield = percentage of functional D/A converters with an INL specification smaller than half an LSB.

\[
\text{INL\_yield} = f \left( \text{mismatch} \right) = f \left( \frac{\sigma(I)}{I} \right)
\]

\[
WL = \frac{1}{2 \left( \frac{\sigma(I)}{I} \right)^2} \left[ A_\beta^2 + \frac{4A_{VT}^2}{(V_{GS}-V_T)^2} \right]
\]

High yield \[\Downarrow\] small \[
\frac{\sigma(I)}{I}
\]

Large current source area

\[
\frac{\sigma(I)}{I} \leq \frac{1}{2 \, C \sqrt{2^N}} \quad \Rightarrow \quad \sigma \left( \frac{l_{\text{unit}}}{l_{\text{unit}}} \right) = 0.25 \%
\]
DAC Design: Calculation W and L

\[
\frac{W}{L} = \frac{I_{\text{LSB}}}{K' (V_{\text{GS}}-V_{\text{T}})^2}
\]

\[
WL = \frac{1}{2 \left( \frac{\sigma(I)\mu m}{I} \right)^2} \left[ A_\beta^2 + \frac{4A_{VT}^2}{(V_{\text{GS}}-V_{\text{T}})^2} \right]
\]

\[
\sigma(I)/I = 0.0025
\]

\[V_{\text{GS}} - V_T = 1 \text{ V}\]

For 0.35 \(\mu \text{m}\) CMOS, \(A_\beta \approx 2 \% \mu \text{m}\)

\[A_{VT} \approx 7 \text{ mV} \mu \text{m}\]

\[
W = 1.8 \, \mu \text{m}
\]

\[
L = 30 \, \mu \text{m}
\]
Floorplan 10-bit segmented DAC

Van den Bosch, ..,
JSSC March 01, 315-324
Required output impedance versus resolution

\[
\begin{array}{|c|c|}
\hline
A_{VT} & 8.94 \text{ mV} \mu \text{m} \\
A_\beta & 1.9 \% \mu \text{m} \\
\sigma(I)/I & 0.5 \% \\
(V_{GS} - V_T)_{cs} & 1 \text{ V} \\
I_{FS} & 20 \text{ mA} \\
\text{segmentation} & 5-5 \\
(W/L)_{cs} & 2 \mu \text{m}/8 \mu \text{m} \\
(W/L)_{sw} & 1 \mu \text{m}/0.7 \mu \text{m} \\
(W/L)_{cas} & 0.5 \mu \text{m}/0.35 \mu \text{m} \\
\hline
\end{array}
\]

10 bit 1GB/s
INL = 99.7 \%
requires \(\sigma(I)/I < 0.5 \%\):
\(W = 2 \mu \text{m} & L = 8 \mu \text{m}\)

Van den Bosch, .., Kluwer 2004
JSSC March 01, 315-324
10-bit 1 GS/s Nyquist Current steering CMOS DAC

Current steering DAC
10-bit
1 GS/s
0.35 μm CMOS
110 mW

Van den Bosch, .., JSSC, March 01, 315-324
SFDR (dB) versus relative signal frequency

\[ \frac{f_{\text{signal}}}{f_{\text{clock}}} \]
FOM (MHz/mW) vs inverse area

FOM = \frac{2^N \cdot f_s(-6\text{dB})}{P}

2^N/\text{area (mm}^2\text{)}
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**Speed Resolution Limits ADC**

\[
FOM = \frac{4kT \times BW \times DR}{P}
\]

\[
2^N \times 2BW \quad P
\]
Dual-slope (integrating) ADC

Time 1 is constant: \( T_1 = 2^N T_{\text{clk}} \)

\[ V_x = \frac{V_{\text{in}}}{R_1C_1} T_1 \]

Time 2: \( V_x \) decreases with constant slope:

\[ V_x = \frac{V_{\text{ref}}}{R_1C_1} T_2 \]

\[ T_2 = T_1 \frac{V_{\text{in}}}{V_{\text{ref}}} \]

\[ B_{\text{out}} = \frac{V_{\text{in}}}{V_{\text{ref}}} \]

Johns, Martin, Wiley 1997
Operation of integrating ADC

Time 1: $V_x = \frac{V_{in}}{R_1C_1} T_1$

Time 2: $V_x = \frac{V_{ref}}{R_1C_1} T_2$

$T_2 = T_1 \frac{V_{in}}{V_{ref}}$
Integrating ADC

Advantages:
High resolution
High linearity
Low circuit complexity
Mainly for voltmeters, …
Eliminates mains supply 50 Hz if T1 is n x 20 ms

Disadvantages:
Very slow :
Worst case for $V_{in} = V_{ref}$ : $2^{2n+1}$ clock cycli required !
Ex. For n = 16 bit (64000) and $F_{clock} = 1$ MHz :
7.6 s conversion time
Mainly for voltmeters, …
Divide interval by 2; Determine bit:

- $< 1$ : $0$ $b_1 = \text{MSB}$
- $< 0.5$ : $0$ $b_2$
- $> 0.25$ : $1$ $b_3$
- $> 0.375$ : $1$ $b_4$
- $< 0.4375$ : $0$ $b_5$

---

Johns, Martin, Wiley 1997
5-bit Charge redistribution ADC

\[ \sum = 2^N C \]

\[ V_x \approx 0 \]

1. Sample Mode

Accuracy limited by capacitive matching to 10-12 bit

Speed limited by \( R_{\text{switch}} C \) time constants

McCreary, JSSC
Dec 75, 371-379

Johns, Martin, Wiley 1997
5-bit Charge redistribution ADC

\[ V_x = -V_{in} \]

2. Hold mode

Bottom plate C to \( V_{ref} \)
5-bit Charge redistribution ADC

\[ V_x = -V_{in} + \frac{V_{ref}}{2} \]

3. Bit cycling

- If \( V_{in} > \frac{V_{ref}}{2} \) 
  - SAR \( \rightarrow 1 \) 
  - Leave \( C_{b1} \) to \( V_{ref} \) 
  - Try \( C_{b2} \)

- If \( V_{in} < \frac{V_{ref}}{2} \) 
  - SAR \( \rightarrow 0 \) 
  - Leave \( C_{b1} \) to Gnd 
  - Try \( C_{b2} \)

Bottom plate C to \( V_{ref} \)

Willy Sansen 10-05 2037
Charge redistribution ADC halves $V_{\text{ref}}$ in each cycle.
Algorithmic ADC doubles $V_{\text{error}}$ in each cycle.
Algorithmic (or cyclic) ADC

Advantage: small amount of analog circuitry
Difficulty: accuracy x2 Gain amplifier
(fully diff.; $C_{par}$ insensitive)

Johns, Martin, Wiley, 2003
Flash converter

3-bit flash ADC:
- fastest
- $2^3$ comparators
- input cap. $\sim 2^3$
- limited to 6 bit
  - (1 ... 2 GS/s)
Evolution in ADC’s

![Graph showing ADC speed versus year of publication](image)

**Uyttenhove, KULeuven, 2003**
Subranging (or two-step) ADC

8-bit two-step ADC:
- less comparators
- introduces latency

2^8 = 256 comp. → now 32!
- All circuits: 8b accurate
- Digital correction required!

Johns, Martin, Wiley 1997
Interpolating saves amplifiers

Input amplifiers which saturate

Van de Grift, JSSC Dec. 87, 944-953; Steyaert CICC 1993
Interpolating ADC

4-bit interpolating ADC
Resistive interpolation

leave out 3 out of 4 amps
Less power consumption
Less input capacitance

Johns, Martin, Wiley 1997
Transfer curves

Resistors generate the intermediate outputs
Resistors average out offsets, etc.
Add series resistors to latch inputs to equalize delay times

Gain ~ 10

Only the zero crossings carry info
Averaging with output currents

\[ I_{2a} = \frac{2}{3} I_1 + \frac{1}{3} I_2 \]

\[ I_{2b} = \frac{1}{3} I_1 + \frac{2}{3} I_2 \]

Interpolating by 3
between output currents \( I_1 \) & \( I_2 \)
Requires 1/3 input amps.: \( C_{in}/3 \)

Steyaert CICC 93
Interpolating/Averaging ADC - 1st amp

Current mirror interpolator

Steyaert CICC 93
Roovers JSSC July 96, 938-944
Interpolating: limitations

\( C_{\text{mirror}} \text{ (fF)} \)

\( f_{-3dB} \text{ (MHz)} \)

Number of transistors
Folding ADC Analog preprocessing

Vin

folding circuit

folded signal

fine ADC

LSBs

coarse ADC

MSBs

folded signal

1 2 3 4 5 6 7 8

V_{in}

Folding rate 8
Less comparators
Same input capacitance
4-bit Folding ADC

Vin starts
from 0 to 1/4:
0001
0011
0111
1111
from 1/4 to 1/2:
1110
1100
1000
0000

4-bit flash: 16 comp.
folding: 8 comp.

Johns, Martin, Wiley 1997

Willy Sansen 10-05 2050
Folding block realization

Folding rate of 4

Differential pairs in parallel!

Large $C_{in}$!

Output at higher freq. = $f_{in} \times$ folding rate

Johns, Martin, Wiley 1997
Folding + interpolation

Folding rate of 4
Interpolate by 2

Lower $C_{\text{in}}$!
Pipelined ADC: $n_k$ and single bit per stage

Algorithmic conversion in pipeline!

$n_k$ bit per stage

Latency of N clock periods

Limited to 12 bit by amp.

Digital error correction

1 bit per stage

Johns, Martin, Wiley 1997
Pipelined ADC block diagram

New sample each clock cycle

Johns, Martin, Wiley 1997
**Multiplying DAC**

DAC + Gain Are merged in one building block:

**Multiplying DAC**

- $V_{res(i)}$ + $\sum$ - $V_{DAC}$
- $G$ 
- $V_{res(i+1)}$
Multiplying DAC : Phase 1

\[ V_{\text{res}(i+1)} = V_{\text{res}(i)} + V_{\text{DAC}} \]

\[ V_{\text{res}(i+1)} = V_{\text{res}(i)} + V_{\text{DAC}} \]

\[ \Phi_1 \]
Multiplying DAC: Phase 2

\[ V_{\text{res}(i+1)} = V_{\text{res}(i)} + \frac{V_{\text{res}(i)} - V_{\text{DAC}}}{C_f} \]

\[ G = 1 + \frac{C_s}{C_f} = 2 \quad \text{if} \quad C_s = C_f \]
Non-idealities versus Cs

0.25 μm CMOS

$f_s = 400$ MHz

Uyttenhove, Kuleuven, 2003
Comparison ADCs

Resolution (bits)

- Flash, Pipeline $t=1$
- Successive Approximation $t=n$
- 2nd order Sigma-delta
  - 1-bit $t=2^{(0.4n+1)}$
- Serial $t=2^n$

Clock cycles Per output sample
Impact of device mismatch on resolution/power

Two transistors: \( \sigma^2(\text{Error}) \sim \frac{1}{WL} \)

(Accuracy) \( ^2 \sim WL \)

By design: increasing \( W \) increases \( I_{DS} \) and Power

decreasing \( L \) increases the speed

\[ \text{Speed} \times \text{(Accuracy)} = \text{Technol. constant} \]

\[ \text{Power} \]

Ref. Kinget, ...“Analog VLSI ..”

Power and mismatch/noise

Accuracy

\[ \frac{1}{\sigma^2(V_{os})} \sim \text{Area} / \text{A}_{VT} \]

Dynamic range

\[ \text{DR} = \frac{V_{sRMS}}{(3 \sigma(V_{os}))} \]

Capacitance

\[ C \sim C_{ox} \text{Area} \]

Power

\[ P = 8 f C V_{sRMS}^2 \]

Mismatch:

\[ P = 24 C_{ox} A_{VT}^2 f DR^2 \]

Noise:

\[ P = 8 kT f DR^2 \]
Noise vs mismatch for DR

Ref. P. Kinget, ... 
"Analog VLSI .." 
page 67, 
ADC limitations

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