
Preface

In Igor Stravinsky's ballet "The Firebird", Prince Ivan captures the exotic Firebird in the magic garden of the sorcerer Kashchei. The prince releases Firebird when she gives him a feather which can be used to summon her in times of danger. The Prince falls in love with a princess held by the evil Kashchei, and eventually defeats the sorcerer and wins the princess' freedom with the Firebird's help.

It is fitting that much of this text was written to the music of this ballet. At once elegant, graceful, coordinated; and disjointed, unexpected, and misunderstood, "The Firebird" all too closely resembles the nuances of Silicon-on-Insulator technology.

As we complete this textbook, it is finally becoming clear that our industry no longer regards silicon-on-insulator technology as being in the same category as gravity-powered shoe air-conditioners and jet-powered surfboards¹. SOI has been incubating for perhaps 20 years. Although the pressures of scaling have increased the urgency of its development, there are those who argue that it's behavior remains too unpredictable to be accurately modeled. Suffice it to say that SOI's potential performance rewards for enduring this complexity are substantial. There is no question that SOI is not an easy technology to learn and design with; using the technology requires a thorough, fundamental comprehension, and demands considerably more designer mental energy than its bulk CMOS predecessor did. The reader must remember, however, that

1. See "The Gallery of Obscure Patents" at <http://www.patents.ibm.com/gallery> on the World Wide Web.

although SOI might be difficult, conventional CMOS was also originally referred to as the S.O.B. (Silicon-On-Bulk, of course!) technology when first introduced.

Chapter 1 provides the reader with a brief review of how CMOS technology has been scaled through multiple lithography generations, and describes the device physics which threaten conventional CMOS' future. The case for SOI is built as a means to continue improvement in density, performance, power and integration.

Chapter 2 introduces the basic SOI physical device structure, and how it differs from its bulk CMOS predecessor. Manufacturing considerations and materials properties are highlighted in this section.

Chapter 3 addresses the fundamental electrical properties associated with the SOI device, and how the structures described in the previous chapter give rise to these properties. If the reader wishes to "cut to the chase," this chapter and the following two provide the most essential of SOI core concepts.

Chapter 4 explores the response of static circuits to SOI technology and offers guidance on static design practice.

Similarly, Chapter 5 provides an introduction to the issues associated with dynamic circuits in SOI, and includes design practices disclosed in the recent literature which mitigate many of the undesirable dynamic problems.

SRAM and cache arrays are probably the hardest designs to move into SOI. Chapter 6 is entirely devoted to addressing the issues surrounding SOI SRAMs. A few suggestions are offered on how to get around some of these problems.

In addition to the SRAM, selected other special function circuits require some finesse when migrated into SOI, and are described in Chapter 7. Off-chip-drivers, phase-locked-loops, and Electro-static Discharge devices are among these unique structures.

Chapter 8 addresses global design considerations which are unique to SOI. Power distribution, clock branching, and noise is discussed.

Finally, Chapter 9 offers a glimpse into some of the future leverage SOI may offer. Rather than designing to avoid SOI's idiosyncrasies, the true benefit of the technology may be realized when these features are exploited.



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