

# Contents

<b>1. An Introduction to Memory Chip Design</b>	<b>1</b>
1.1 Introduction	1
1.2 The Internal Organization of Memory Chips	3
1.2.1 The Memory Cell Array	3
1.2.2 The Peripheral Circuit	5
1.2.3 The I/O Interface Circuit	6
1.3 Categories of Memory Chip	6
1.4 General Trends in DRAM Design and Technology	11
1.4.1 The History of Memory-Cell Development	11
1.4.2 The Basic Operation of The 1-T Cell	15
1.4.3 Advances in DRAM Design and Technology	19
1.5 General Trends in SRAM Design and Technology	24
1.5.1 The History of Memory-Cell Development	24
1.5.2 The Basic Operation of a SRAM Cell	26
1.5.3 Advances in SRAM Design and Technology	29
1.6 General Trends in Non-Volatile Memory Design and Technology	31
1.6.1 The History of Memory-Cell Development	31
1.6.2 The Basic Operation of Flash Memory Cells	34
1.6.3 Advances in Flash-Memory Design and Technology	46
<b>2. The Basics of RAM Design and Technology</b>	<b>49</b>
2.1 Introduction	49
2.2 Devices	49
2.2.1 MOSFETs	49
2.2.2 Capacitors	57
2.2.3 Resistors	60
2.2.4 Wiring and Wiring Materials	61
2.2.5 Silicon Substrates and CMOS Latch-Up	65
2.2.6 Other Devices	67
2.3 NMOS Static Circuits	67
2.3.1 The dc Characteristics of an Inverter	68
2.3.2 The ac Characteristics of an Inverter	70
2.3.3 The Improved NMOS Static Inverter	74

2.4	NMOS Dynamic Circuits .....	76
2.4.1	The Dynamic Inverter .....	76
2.4.2	The Bootstrap Driver .....	77
2.5	CMOS Circuits .....	79
2.5.1	The dc Characteristics .....	80
2.5.2	The ac Characteristics .....	82
2.6	Basic Memory Circuits .....	83
2.6.1	The Inverter and the Basic Logic Gate .....	83
2.6.2	The Current Mirror .....	83
2.6.3	The Differential Amplifier .....	83
2.6.4	The Voltage Booster .....	87
2.6.5	The Level Shifter .....	88
2.6.6	The Ring Oscillator .....	88
2.6.7	The Counter .....	89
2.7	The Scaling Law .....	90
2.7.1	Constant Electric-Field Scaling .....	90
2.7.2	Constant Operation-Voltage Scaling .....	92
2.7.3	Combined Scaling .....	92
2.8	Lithography .....	93
2.9	Packaging .....	94
<b>3.</b>	<b>DRAM Circuits .....</b>	<b>97</b>
3.1	Introduction .....	97
3.1.1	High-Density Technology .....	98
3.1.2	High-Performance Circuits .....	100
3.2	The catalog Specifications of the Standard DRAM .....	102
3.2.1	Operational Conditions .....	102
3.2.2	Modes of Operation and Timing Specifications .....	105
3.3	The Basic Configuration and Operation of the DRAM Chip ..	110
3.3.1	Chip Configuration .....	110
3.3.2	Address Multiplexing .....	111
3.4	Fundamental Chip Technologies .....	113
3.4.1	A Larger Memory Capacity and Scaled-Down Devices ..	113
3.4.2	High S/N Ratio Circuits .....	116
3.4.3	Low Power Circuits .....	117
3.4.4	High-Speed Circuits .....	123
3.4.5	The Multidivision of a Memory Array .....	128
3.5	The Multidivided Data Line and Word Line .....	131
3.5.1	The Multidivided Data Line .....	132
3.5.2	The Multidivided Word Line .....	139
3.6	Read and Relevant Circuits .....	141
3.6.1	The Address Buffer .....	141
3.6.2	The Address Decoder .....	144
3.6.3	The Word Driver .....	147
3.6.4	The Sensing Circuit .....	157

3.6.5	The Common I/O-Line Relevant Circuit .....	167
3.6.6	The Data-Output Buffer .....	172
3.7	Write and Relevant Circuits .....	174
3.8	Refresh-Relevant Circuits .....	175
3.8.1	Refresh Schemes .....	175
3.8.2	The Extension of Data-Retention Time in Active Mode .....	176
3.8.3	Current Reduction Circuits in Data-Retention Mode ..	176
3.9	Redundancy Techniques .....	178
3.9.1	Issues for Large-Memory-Capacity Chips .....	184
3.9.2	Intra-Subarray Replacement Redundancy .....	185
3.9.3	Inter-Subarray Replacement Redundancy .....	189
3.9.4	The Repair of dc-Characteristics Faults .....	191
3.10	On-Chip Testing Circuits .....	192
<b>4.</b>	<b>High Signal-to-Noise Ratio</b>	
	<b>DRAM Design and Technology .....</b>	<b>195</b>
4.1	Introduction .....	195
4.2	Trends in High S/N Ratio Design .....	195
4.2.1	The Signal Charge .....	197
4.2.2	Leakage Charge .....	204
4.2.3	The Soft-Error Critical Charge .....	208
4.2.4	The Data-Line Noise Charge .....	210
4.3	Data-Line Noise Reduction .....	210
4.3.1	Noise Sources and Their Reduction .....	210
4.3.2	Word-Line Drive Noise .....	213
4.3.3	Data-Line and Sense-Amplifier Imbalances .....	217
4.3.4	Word-Line to Data-Line Coupling Noise .....	230
4.3.5	Data-Line Interference Noise .....	237
4.3.6	Power-Supply Voltage Bounce .....	240
4.3.7	Variation in the Reference Voltage .....	241
4.3.8	Other Noises .....	244
4.4	Summary .....	247
<b>5.</b>	<b>On-Chip Voltage Generators .....</b>	<b>249</b>
5.1	Introduction .....	249
5.2	The Substrate-Bias Voltage ( $V_{BB}$ ) Generator .....	251
5.2.1	The Roles of the $V_{BB}$ generator .....	251
5.2.2	Basic Operation and Design Issues .....	256
5.2.3	Power-On Characteristics .....	258
5.2.4	Characteristics in the High- $V_{DD}$ Region .....	264
5.2.5	The $V_{BB}$ Bump .....	266
5.2.6	Substrate-Current Generation .....	269
5.2.7	Triple-Well Structures .....	272
5.2.8	Low-Power $V_{BB}$ Generators .....	273

5.3	The Voltage Up-Converter .....	276
5.3.1	The Roles of the Voltage Up-Converter .....	276
5.3.2	Design Approaches and Issues .....	278
5.3.3	High Boost-Ratio Converters .....	283
5.3.4	Low-Power, High Supply Current Converters .....	285
5.4	The Voltage Down-Converter .....	290
5.4.1	The Roles of the Voltage Down-Converter .....	290
5.4.2	The Negative-Feedback Converter and Design Issues ..	293
5.4.3	Optimum Design .....	297
5.4.4	Phase Compensation .....	301
5.4.5	Reference-Voltage Generators .....	316
5.4.6	Burn-In Test Circuits .....	323
5.4.7	Voltage Trimming .....	327
5.4.8	Low-Power Circuits .....	329
5.5	The Half- $V_{DD}$ Generator .....	332
5.6	Examples of Advanced On-Chip Voltage Generators .....	333
<b>6.</b>	<b>High-Performance Subsystem Memories .....</b>	<b>339</b>
6.1	Introduction .....	339
6.2	Hierarchical Memory Systems .....	341
6.2.1	Memory Hierarchy .....	341
6.2.2	Improvements in Memory-Subsystem Performance ...	344
6.2.3	Memory-Chip Performance .....	349
6.3	Memory-Subsystem Technologies .....	354
6.3.1	Wide-Bit I/O Chip Configurations .....	354
6.3.2	Parallel Operation of Multidivided Arrays .....	354
6.3.3	Multibank Interleaving .....	357
6.3.4	Synchronous Operation .....	358
6.3.5	Pipeline/Prefetch Operations .....	362
6.3.6	High-Speed Clocking Schemes .....	363
6.3.7	Terminated I/O Interfaces .....	363
6.3.8	High-Density Packaging .....	364
6.4	High-Performance Standard DRAMs .....	365
6.4.1	Trends in Chip Development .....	365
6.4.2	Synchronous DRAM .....	368
6.4.3	Rambus DRAM .....	380
6.5	Embedded Memories .....	383
<b>7.</b>	<b>Low-Power Memory Circuits .....</b>	<b>389</b>
7.1	Introduction .....	389
7.2	Sources and Reduction of Power Dissipation in a RAM Subsystem .....	392
7.2.1	Wide-Bit I/O Chip Configuration .....	393
7.2.2	Small Package .....	394
7.2.3	The Low-Voltage Data-Bus Interface .....	396

7.3	Sources of Power Dissipation in the RAM Chip .....	402
7.3.1	Active Power Sources .....	402
7.3.2	Data-Retention Power Sources .....	405
7.4	Low-Power DRAM Circuits .....	406
7.4.1	Active Power Reduction .....	406
7.4.2	Data-Retention Power Reduction .....	412
7.5	Low-Power SRAM Circuits .....	413
7.5.1	Active Power Reduction .....	413
7.5.2	Data-Retention Power Reduction .....	423
<b>8.</b>	<b>Ultra-Low-Voltage Memory Circuits .....</b>	<b>425</b>
8.1	Introduction .....	425
8.2	Design Issues for Ultra-Low-Voltage RAM Circuits .....	426
8.2.1	Reduction of the Subthreshold Current .....	426
8.2.2	Stable Memory-Cell Operation .....	432
8.2.3	Suppression of, or Compensation for, Design Parameter Variations .....	433
8.2.4	Power-Supply Standardization .....	435
8.3	Ultra-Low-Voltage DRAM Circuits .....	437
8.3.1	Gate Boosting Circuit .....	439
8.3.2	The Multi- $V_T$ Circuit .....	440
8.3.3	The Gate-Source Back-Biasing Circuit .....	442
8.3.4	The Well Control Circuit .....	456
8.3.5	The Source Control Circuit .....	461
8.3.6	The Well and Source Control Circuit .....	462
8.4	Ultra-Low-Voltage SRAM Circuits .....	463
8.5	Ultra-Low-Voltage SOI Circuits .....	466
	<b>References .....</b>	<b>473</b>
	<b>Index .....</b>	<b>489</b>





<http://www.springer.com/978-3-540-67820-5>

VLSI Memory Chip Design

Itoh, K.

2001, XI, 495 p., Hardcover

ISBN: 978-3-540-67820-5