Chapter 2

# SINEWAVE TEST SETUP

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## 1. Test Setup description

All the dynamic test methods using sinewaves described in this book make use of a test setup of the type described in figure 2.1. A distinct advantage of sinewave testing is that it is relatively easy to evaluate the purity of a sinewave, for instance using a spectrum analyzer, and it is also easy to improve this purity by suitable filtering. In addition, high quality sinewave synthesizers are available on the market.

The ADC under test is stimulated with the sinewave provided by a high purity sinewave generator. Generally, the spectral purity of the generator alone is not adequate to the purpose of testing. In that case, a bandpass filter has to be inserted between the source and the ADC in order to reduce noise and/or harmonic distortion. In some cases, level adapters and unbalanced to balanced signal converters have to be added. All this extra electronics is preferably placed between the source and the bandpass filter, so that its contributions to distortion and noise are filtered out. Finally, an impedance matching network is frequently required between the bandpass filter and the ADC.

For intermodulation distortion (IMD) testing, figure 2.2 describes the test setup for two-tone measurements. If additional tones are needed, the same



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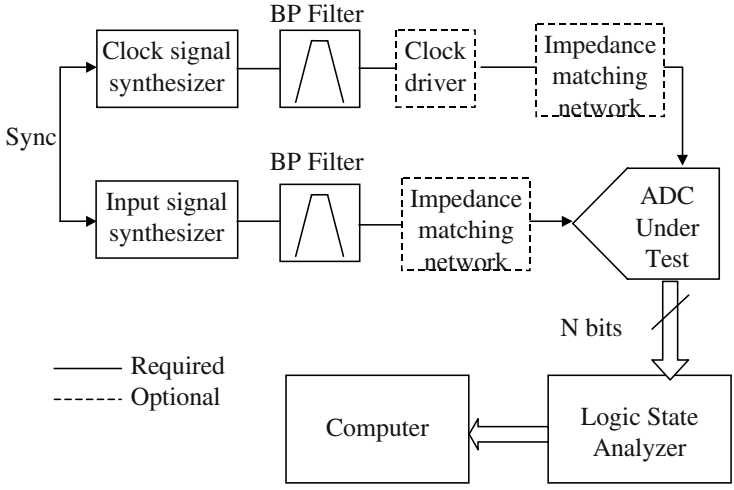


*Figure 2.1.* Test Setup for Sine Wave Testing.

type of setup can be used by combining the output of the required number of sinewave synthesizers. For IMD testing, an additional bandpass filter may be required after the combination of the tones in order to reduce the IMD of the input signal. As for single tone testing, an impedance matching network is frequently required between the bandpass filter and the ADC. The sampling clock is preferably derived from a second sinewave synthesizer: if this is indeed the case, the two synthesizers can be phase-locked, to guarantee that the sampling instants are placed in precise phase relationship with the input sinewave. This offers several advantages for the subsequent processing of the data, in particular by eliminating beat patterns which may render the measurement results unreliable.

The filter before the comparator/driver has the purpose of removing additive noise superposed to the sinewave, so as to reduce jitter at the output of the clock driver. A relevant advantage of using a sinewave generator to deliver the clock signal is related to the quieter EMC environment of the test bench: the high frequency harmonic contents related to the presence of a digital clock signal are confined to a small portion of the test board, between the comparator/clock driver and the ADC under test. Frequently it may be advisable to smooth the edges of the clock signal, to avoid leakages to other sensitive parts of the test board.

Note that an external frequency divider may be inserted in the clock chain, with the aim of achieving more closely the desired frequency ratio and/or reducing the phase noise of the sampling signal.

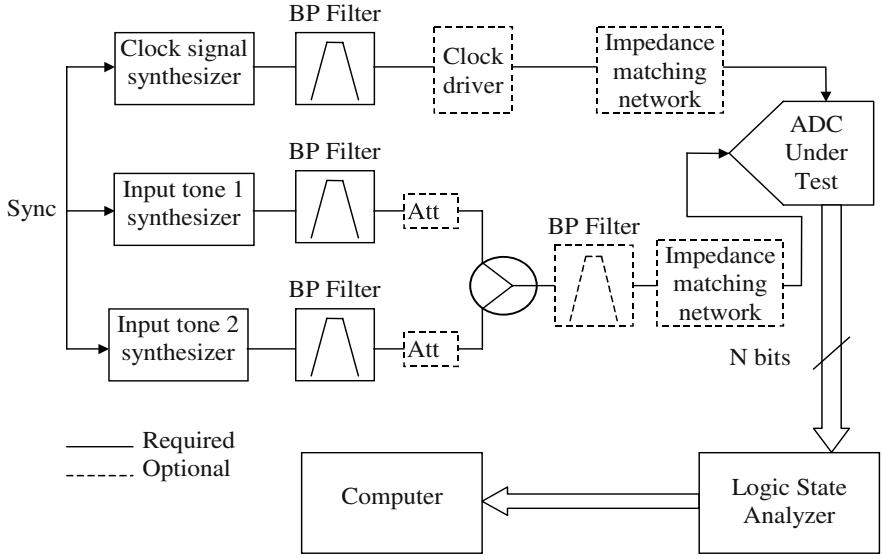


*Figure 2.2.* Test Setup for two-tone IMD Testing.

# 2. Specification of the clock and input signal

## 2.1 Harmonic distortion considerations

**2.1.1 THD measurements.** The harmonic distortion of the input sinewave must be related to the THD of the ADC under test in order to minimize the errors in the measurements of the THD and also of the SINAD and/or of the SFDR.

In the worst case, the THD of the ADC under test and the input sinewave distortion are dominated by the same harmonic component (same frequency and same phase). In the case of one dominant harmonic component, the THD of the ADC can be approximated by

$$\begin{aligned} THD_{ADC} &= \frac{A_{H_{ADC}}}{A} \\ THD_{ADC_{dB}} &= 20log\frac{A_{H_{ADC}}}{A} \end{aligned} \tag{2.1}$$

where $A_{H_{ADC}}$ is the amplitude of the dominant harmonic component created by the ADC and $A$ is the amplitude of the fundamental component.

The THD of the input sinewave can be defined by

$$\begin{aligned} THD_{input} &= \frac{A_{H_{input}}}{A} \\ THD_{input_{dB}} &= 20log\frac{A_{H_{input}}}{A} \end{aligned} \tag{2.2}$$

where $A_{H_{input}}$ is the dominant harmonic component of the input sinewave and $A$ is the amplitude of the input sinewave.

As the dominant harmonic component created by the ADC and the input harmonic distortion have the same frequency and the same phase, the measured THD is

$$\begin{aligned} THD_{measured_{dB}} &= 20log\frac{A_{H_{ADC}} + A_{H_{input}}}{A} \\ &= 20log\left[\frac{A_{H_{ADC}}}{A}\left(1 + \frac{A_{H_{input}}}{A_{H_{ADC}}}\right)\right] \\ &= THD_{ADC_{dB}} + 20log\left(1 + \frac{THD_{input}}{THD_{ADC}}\right) \end{aligned} \tag{2.3}$$

In that case, the error on the measurement of the THD is

$$20log\left(1 + \frac{THD_{input}}{THD_{ADC}}\right)$$

For an error lower than 0.5 dB on the measurement of the THD, the harmonic distortion of the input sinewave must be at least 25 dB better than the THD of the ADC.

In all the other cases, the THD of the ADC as well as the distortion of the input sinewave result from a distortion over many harmonic components. These components have not necessary the same frequency and/or the same phase. In that case, the THD of the ADC is defined by

$$\begin{aligned} THD_{ADC} &= \frac{\sqrt{\sum_i A^2_{H_{i_{ADC}}}}}{A} \\ THD_{ADC_{dB}} &= 20log\frac{\sqrt{\sum_i A^2_{H_{i_{ADC}}}}}{A} \end{aligned} \tag{2.4}$$

where $A^2_{H_{i_{ADC}}}$ is the power of the $i^th$ harmonic component created by the ADC and $A$ is the amplitude of the fundamental component.

The THD of the input sinewave can be defined by

$$\begin{aligned} THD_{input} &= \frac{\sqrt{\sum_i A^2_{H_{i_{input}}}}}{A} \\ THD_{input_{dB}} &= 20log\frac{\sqrt{\sum_i A^2_{H_{i_{input}}}}}{A} \end{aligned} \tag{2.5}$$

where $A^2_{H_{i_{input}}}$ and $A$ are respectively the power of the $i^th$ harmonic component and the amplitude of the fundamental component of the input sinewave.

In that case, the powers of the harmonic components must be added and the measured THD is

$$\begin{aligned} THD_{measured_{dB}} &= 20log\frac{\sqrt{\sum_i A^2_{H_{i_{ADC}}} + \sum_i A^2_{H_{i_{input}}}}}{A} \\ &= 10log\left[\frac{\sum_i A^2_{H_{i_{ADC}}}}{A^2}\left(1 + \frac{\sum_i A^2_{H_{i_{input}}}}{\sum_i A^2_{H_{i_{ADC}}}}\right)\right] \\ &= THD_{ADC_{dB}} + 20log\sqrt{1 + \frac{THD^2_{input}}{THD^2_{ADC}}} \end{aligned} \tag{2.6}$$

In the cases where the THD of the ADC and the distortion of the input sinewave result from a distortion over many harmonic components, the error on the measurement of the THD is

$$20log\sqrt{1 + \frac{THD^2_{input}}{THD^2_{ADC}}}$$

For an error lower than 0.5 dB on the measurement of the THD, the harmonic distortion of the input sinewave must be at least 9 dB better than the THD of the ADC.

Given the case considered and knowing the harmonic distortion of the input sinewave synthesizer, the rejection of the bandpass filter inserted between the source and the ADC can be calculated.

**2.1.2 IMD measurements.** If the IMD of the ADC and the IMD of the input signal are dominated by the same intermodulation tone (IM tone) (same frequency and same phase), the same reasoning than the one used for the worst case THD measurement leads to an error on the measured IMD equal to

$$\epsilon_{IMD} = -20log\left(1 + \frac{IMD_{ADC}}{IMD_{input}}\right) \tag{2.7}$$

Where

$$IMD_{ADC} = \frac{A}{A_{IMtone_{ADC}}} \tag{2.8}$$

and

$$IMD_{input} = \frac{A}{A_{IMtone_{input}}} \tag{2.9}$$

with $A_{IMtone_{ADC}}$ is the amplitude of the dominant IM tone created by the ADC, $A$ the amplitude of the lower input tone, and $A_{IMtone_{input}}$ the amplitude of the dominant IM tone of the input signal.

For an error lower than 0.5 dB on the measurement of the IMD, the intermodulation distortion of the input signal must be at least 25 dB better than the one of the ADC.

If the IMD of the ADC and the IMD of the input signal are not dominated by the same IM tone, the difference between the IMD of the input signal and the one of the ADC can be lower than 25 dB for an error of 0.5 dB on the measurement of the IMD of the ADC. This difference depends on the configuration of the IM tones at the input of the ADC and on the configuration of the IM tones created by the ADC, that is why it is impossible to give a general rule in that case. Nevertheless, the error given in (2.7) is a worst case one and for a given value of the error, the ratio between the IMD of the input signal and the IMD of the ADC calculated from this equation will ensure that, in any case, the IMD is always measured with the accuracy wanted.

## 2.2 Jitter considerations

The phase noise of the signal and clock sources produce errors for many dynamic test methods. The phase noise of a signal source is usually described by the SSB phase noise spectral power density $\mathcal{L}(f_o)$ (measured in dBc/Hz) as a function of the offset $f_o$ from the carrier (in Hz), see figure 2.3. The variance (power) of the phase noise is calculated by[1]

$$\sigma_\theta^2 = 2\int_{f_L}^{f_H} \mathcal{L}(f_o)df_o \tag{2.10}$$

where $f_L$ and $f_H$ depend of the application in which the generator is used.

In the setup described in figure 2.1, a selective bandpass filter is placed between the ADC and the generator for the signal and the clock sources. If the filters' 3 dB bandwidth are $BW_{f_{in}}$ for the input signal and $BW_{f_s}$ for the clock signal, the upper bound of the integral in (2.10) is $f_H = \frac{BW_{f_{in}}}{2}$ for the input signal and $f_H = \frac{BW_{f_s}}{2}$ for the clock signal.

[1] see equations (22.9) and (22.10) in [38].

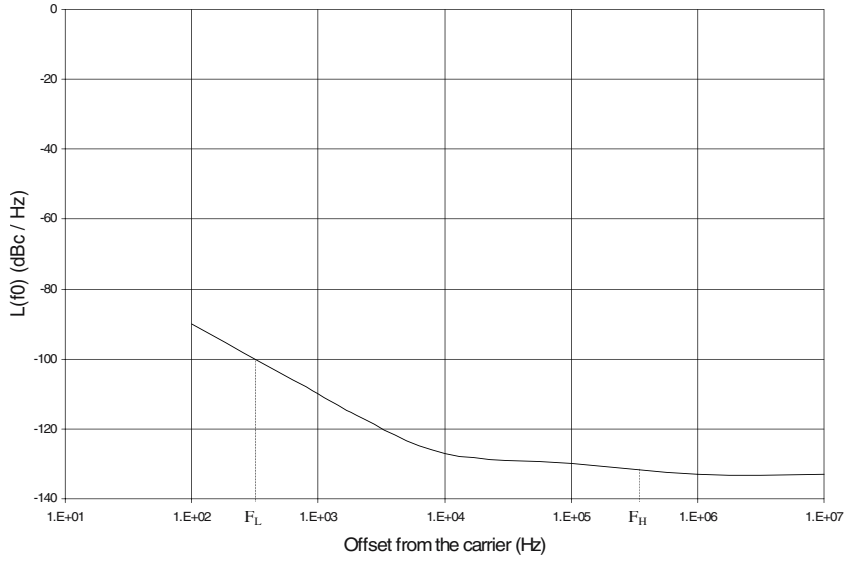


*Figure 2.3.* Typical SSB phase noise power density of a sinewave generator.

If we consider the acquisition of $M$ samples at the sampling frequency $f_s$, the lower bound of the integral in (2.10) is $f_L = \frac{f_s}{M}$ for both signals.

So for the test setup described in figure 2.1, the variances of the phase noise of the input signal and of the clock signal can be calculated by

$$\begin{aligned} \sigma^2_{\theta_{sig}} &= 2\int_{\frac{f_s}{M}}^{\frac{BW_{f_{in}}}{2}} \mathcal{L}_{sig}(f_o)df_o \\ \sigma^2_{\theta_{clk}} &= 2\int_{\frac{f_s}{M}}^{\frac{BW_{f_s}}{2}} \mathcal{L}_{clk}(f_o)df_o \end{aligned} \tag{2.11}$$

Note that if $\frac{BW_{f_{in}}}{2}$ (respectively $\frac{BW_{f_s}}{2}$) is lower than or equal to $\frac{f_s}{M}$, no phase noise is added to the input (respectively clock) signal.

The timing jitter variance is related to the phase noise variance by

$$\begin{aligned} \sigma^2_{T_{sig}} &= \frac{\sigma^2_{\theta_{sig}}}{(2\pi f_{in})^2} \\ \sigma^2_{T_{clk}} &= \frac{\sigma^2_{\theta_{clk}}}{(2\pi f_s)^2} \end{aligned} \tag{2.12}$$

*Table 2.1.* Error (in dB) on SNR measurement due to timing jitter(1/2)

| $\mathbf{N} \downarrow \setminus \mathbf{f_{in}}\sigma_\mathbf{T} \rightarrow$ | *5E-4* | *1E-4* | *5E-5* | *1E-5* | *5E-6* | *1E-6* |
|---|---|---|---|---|---|---|
| **6** | 0.3 | $< 0.1$ | $< 0.1$ | $< 0.1$ | $< 0.1$ | $< 0.1$ |
| **7** | 0.9 | $< 0.1$ | $< 0.1$ | $< 0.1$ | $< 0.1$ | $< 0.1$ |
| **8** | 2.9 | 0.2 | $< 0.1$ | $< 0.1$ | $< 0.1$ | $< 0.1$ |
| **9** | 6.9 | 0.6 | 0.2 | $< 0.1$ | $< 0.1$ | $< 0.1$ |
| **10** | $> 10$ | 2.1 | 0.6 | $< 0.1$ | $< 0.1$ | $< 0.1$ |
| **11** | $> 10$ | 5.4 | 2.1 | 0.1 | $< 0.1$ | $< 0.1$ |
| **12** | $> 10$ | $> 10$ | 5.4 | 0.4 | 0.1 | $< 0.1$ |
| **13** | $> 10$ | $> 10$ | $> 10$ | 1.5 | 0.4 | $< 0.1$ |
| **14** | $> 10$ | $> 10$ | $> 10$ | 4.1 | 1.5 | 0.1 |
| **15** | $> 10$ | $> 10$ | $> 10$ | 8.7 | 4.1 | 0.3 |
| **16** | $> 10$ | $> 10$ | $> 10$ | $> 10$ | 8.7 | 1.0 |
| **17** | $> 10$ | $> 10$ | $> 10$ | $> 10$ | $> 10$ | 3.0 |
| **18** | $> 10$ | $> 10$ | $> 10$ | $> 10$ | $> 10$ | 7.0 |

The variance of the total timing jitter of the test setup is

$$\sigma_T^2 = \sigma_{T_{sig}}^2 + \sigma_{T_{clk}}^2 \tag{2.13}$$

Note that the contribution of the clock driver to the total timing jitter has been neglected in (2.13). For most high speed ADCs, no external clock driver is required and (2.13) is valid. When an external clock driver is required, the phase noise of the clock signal must be measured after the clock driver in order to take into account its effects on the phase noise of the clock signal. In that case, $\sigma_{T_{clk}}^2$ is replaced by $\sigma_{T_{clk+driver}}^2$ in (2.13). Nevertheless, the contribution of the external clock driver to the total timing jitter is often negligible and (2.13) can be used.

The total timing jitter, causes a non-uniform sampling of the input signal, which results in an error on the measurement of dynamic parameters like SNR, SINAD, DNL, and INL.

For an ideal N-bit ADC, the SNR is

$$SNR_{ideal} = 10log(2^{2N-1} \times 3) = 6.02N + 1.76 \tag{2.14}$$

If the SNR of this N-bit ideal ADC is measured with a non-ideal test setup, the presence of timing jitter leads the measured value to be lower than the value calculated by (2.14). An expression of the measured SNR in presence of a timing jitter with a variance $\sigma_T^2$ is found in [130]

$$SNR_{measured} = -10log\left(\frac{1}{3 \times 2^{2N-1}} + (2\pi f_{in}\sigma_T)^2\right) \tag{2.15}$$

*Table 2.2.* Error (in dB) on the SNR measurement due to timing jitter (2/2)

| $\mathbf{N} \downarrow \setminus \mathbf{f_{in}}\sigma_\mathbf{T} \rightarrow$ | *5E-7* | *1E-7* | *5E-8* | *1E-8* | *5E-9* | *1E-9* |
|---|---|---|---|---|---|---|
| **15** | 0.1 | $< 0.1$ | $< 0.1$ | $< 0.1$ | $< 0.1$ | $< 0.1$ |
| **16** | 0.3 | $< 0.1$ | $< 0.1$ | $< 0.1$ | $< 0.1$ | $< 0.1$ |
| **17** | 1.0 | $< 0.1$ | $< 0.1$ | $< 0.1$ | $< 0.1$ | $< 0.1$ |
| **18** | 3.0 | 0.2 | $< 0.1$ | $< 0.1$ | $< 0.1$ | $< 0.1$ |
| **19** | 7.0 | 0.7 | 0.2 | $< 0.1$ | $< 0.1$ | $< 0.1$ |
| **20** | $> 10$ | 2.2 | 0.7 | $< 0.1$ | $< 0.1$ | $< 0.1$ |
| **21** | $> 10$ | 5.6 | 2.2 | 0.1 | $< 0.1$ | $< 0.1$ |
| **22** | $> 10$ | $> 10$ | 5.6 | 0.4 | 0.1 | $< 0.1$ |
| **23** | $> 10$ | $> 10$ | $> 10$ | 1.5 | 0.4 | $< 0.1$ |
| **24** | $> 10$ | $> 10$ | $> 10$ | 4.3 | 1.5 | 0.1 |

The error on the SNR measurement due to the timing jitter of the test setup is

$$\epsilon_{SNR} = 6.02N + 1.76 + 10log\left(\frac{1}{3 \times 2^{2N-1}} + (2\pi f_{in}\sigma_T)^2\right) \tag{2.16}$$

The SNR error measurement expressed in dB is listed in Tables 2.1 and 2.2, for diferent error ranges, as a function of $N$ and $f_{in}\sigma_T$. It can be seen that very large errors can occur when the timing jitter of the test setup is not low enough.

The error calculated in the tables can also be expressed as

$$\epsilon_{SNR} = 6.02N + 1.76 + 10log\left(\frac{1}{3 \times 2^{2N-1}} + \sigma^2_{\phi_{sig}} + \left(\frac{f_{in}}{f_s}\right)^2 \sigma^2_{\phi_{clk}}\right) \tag{2.17}$$

For a given ADC, the only way to reduce this error is to lower the variance of the phase noise of the input signal and of the clock signal. In (2.17) the variance of the clock phase noise is multiplied by $\left(\frac{f_{in}}{f_s}\right)^2$. That reduces the effect of the clock phase noise for the measurements performed with an input signal in the 2 first Nyquist zones and increases its effect otherwise.

The value of the variance of the phase noise results from the integration of the SSB phase noise spectral power density of the generator (see (2.11)). The lower bound of the integral ($\frac{f_s}{M}$) is defined by the ADC under test. The upper one is half the bandwidth of the bandpass filter, that is why very narrow bandpass filters allow the power of the phase noise to be reduced.

Knowing the SSB phase noise spectral power density of generators and the input and clock frequencies, the bandwidth of the filters of the setup described in figure 2.1 can be specified in order to measure the SNR of the ADC with the accuracy wanted.

Using filters with a bandwidth such that $\frac{BW_{fs}}{2} \leq \frac{f_s}{M}$ and $\frac{BW_{f_{in}}}{2} \leq \frac{f_s}{M}$ provides a reduced timing jitter test setup which does not affect SNR measurement errors. Unfortunately, it is often impossible to reach such a narrow bandwidth or it requires very expensive filters. However, thanks to the performances of the high purity sinewave generators available on the market, it is often not necessary to use bandpass filters with such narrow bandwidths.

For a given ADC, in order to reach the required accuracy on the SNR measurement, the maximum tolerable total timing jitter value is given in Tables 2.1 and 2.2. After that value, the generator's SSB phase noise spectral power density, and input and clock frequencies, the clock and signal bandwidths (($BW_{clk}$) and $BW_{sig}$) can be determined. It is very important to specify precisely the filters' bandwidths and not to overestimate them, because they often determine the filters' technology and thus there cost.

## 3. Example of filter specification

Let's consider a 12-bit 50 MS/s ADC to be measured with an accuracy of 0.1 dB on the SNR and 0.5 dB on the THD. The typical value of the SNR given by the manufacturer is 68 dBFS for $f_{in} = 10MHz$, the typical THD at the same frequency is -80 dBFS. The record size for the characterization is 16384 samples. The synthesizers used for the clock and input signals are identical and their SSB phase noise power density is given in table 2.3.

*Table 2.3.* SSB phase noise power density of the clock and signal generators.

| *Offset from the carrier (Hz)* | $\mathcal{L}(f_o)$ *(dBc/Hz)* |
|---|---|
| 1 | -78 |
| 10 | -108 |
| 100 | -126 |
| 1000 | -132 |
| 3000 | -135 |
| 5000 | -138 |
| 10000 | -138 |
| 100000 | -139 |

The highest harmonic generated by the synthesizer is the second one and its amplitude is 30 dB below the carrier. Let's consider that the THD of the ADC is also determined by the second harmonic. As described in 2.1, the THD of the input signal, being $\text{THD}_{ADC}$=-80 dBFS, must be at least -105 dB to reach the desired accuracy. That leads to specify the minimum rejection of the signal BP filter to -75 dB at 20 MHz. To get a maximum SNR measurement error of 0.1

dB with this ADC (68 dBFS), line N=12 of table 2.1 gives a maximum value for $f_{in}\sigma_T$ of $5.10^{-6}$, that is to say a maximum timing jitter of $\sigma_T \leq 0.5ps$.

The bandwidth of the clock and signal band-pass filters must then be specified to limit the total jitter to $0.5ps$. As the signal synthesizers are the same for the clock and input signals, and as the clock frequency is five times the input signal frequency, the bandwidth of the clock filter can be wider than the one of the signal filter. Even if there are many bandwidth combinations that can lead to the correct setup, the more apropriate combinations of filter bandwidths are the ones that allow the lowest cost filters to be used. In this case, assuming that the timing jitter induced by the signal is 0.92 ps and the jitter induced by the clock is 0.4 ps ($sqrt(0.92^2 + 0.4^2) = 1$), a good bandwidth specification could be, according 2.11 and 2.12,

- 3 dB BW of the signal filter — $BW_{f_{in}} = 56,2\ kHz\ (0.6\%)$
- 3 dB BW of the clock filter — $BW_{f_s} = 711\ kHz\ (1.4\%)$

The percentage figures between brackets give the ratio between the bandwidth of the filter and its central frequency, which is sometimes called the relative bandwidth of the filter. When specified as described above, the two filters can be manufactured with a low cost technology (LC).

Another filters' combination still limiting jitter to 0.5 ps could be

- 3 dB BW of the signal filter — $BW_{f_{in}} = 24\ kHz\ (0.24\%)$
- 3 dB BW of the clock filter — $BW_{f_s} = 1520\ kHz\ (3\%)$

Now, the timing jitter induced by the signal is 0.24 ps and the clock induced jitter is 0.44 ps. This filters' specification leads to a much narrower signal filter, which might not be the best choice in terms of filters' costs.

## 4. Filter selection

The explanations and tables given in section 2 allow the value of the rejection and of the bandwidth of the bandpass filters to be calculated. From these values, the feasibility and the technology adopted to design the filters can be determined. Table 2.4 lists the narrowest 3 dB bandwidths and the highest reachable rejections for filter technologies suitable for the frequencies commonly used in the dynamic testing of ADCs.

The relative 3 dB BW is the value of the 3 dB BW divided by the central frequency and the rejection is the difference between the stopband attenuation and the insertion loss.

The values in table 2.4 define rather standard filters for most of the very narrow and very high selectivity bandpass filter manufacturers. Nevertheless, some manufacturers can design specific filters with higher performances.

*Table 2.4.* Filters performances

| *Technology* | *Center Frequency* | *Relative 3 dB BW* | *Rejection* |
|---|---|---|---|
| L, C | DC → 1 GHz | 1 % | 70 dB |
| Quartz | 10 kHz → 100 MHz | 0.01 % | 90 dB |
| Surface Acoustic Wave (SAW) | 10 MHz → 2 GHz | 0.02 % | 60 dB |
| Tubular | 50 MHz → 6 GHz | 2 % | 70 dB |
| Printed line | 50 MHz → 18 GHz | 3 % | 60 dB |
| Dielectric Resonator | 400 MHz → 3 GHz | 1 % | 60 dB |

## 4.1 LC filters design

For the dynamic testing of ADC using sinewaves, band-pass filters are used in order to filter the noise and/or the harmonics. Generally, the parameters required for the filters used in sinewave test setups are a narrow 3 dB bandwidth and a high stop-band rejection. The most suitable filters to provide these characteristics are Chebyshev filters. Moreover, for sinewave testing, the ripple of that kind of filter is not a problem as it can be for wide-band signal testing.

The harmonic distortion and jitter considerations allow the value of the stop-band width, the stop-band attenuation and the 3 dB bandwidth to be determined. To design the filter, the input and the output impedances must also be known. Most of the time, with LC filters, these impedances equal 50 Ω and a impedance matching network is used to match the filter impedance to the ADC impedance.

Knowing the stop-band width and the stop-band attenuation, the order of the filter can be determined as shown in figure 2.4. The curves of figure 2.4 are reproduced from [150] and show the pass-band and stop-band attenuation as a function of the frequency normalized to the 3 dB bandwidth. Once the order of the filter is determined, [150] gives the normalized value of the inductors and capacitors to use to build the filter. The last step is to denormalize these coefficients using the central frequency, the 3 dB bandwidth and the input and the output impedances in order to get the real values of the components to use.

Today, this analysis is performed automatically with the filter synthesis softwares available on the market. Moreover, these softwares can take into account the quality factors of the inductors and capacitors and thus simulate the exact response curve of the filters that will be manufactured.

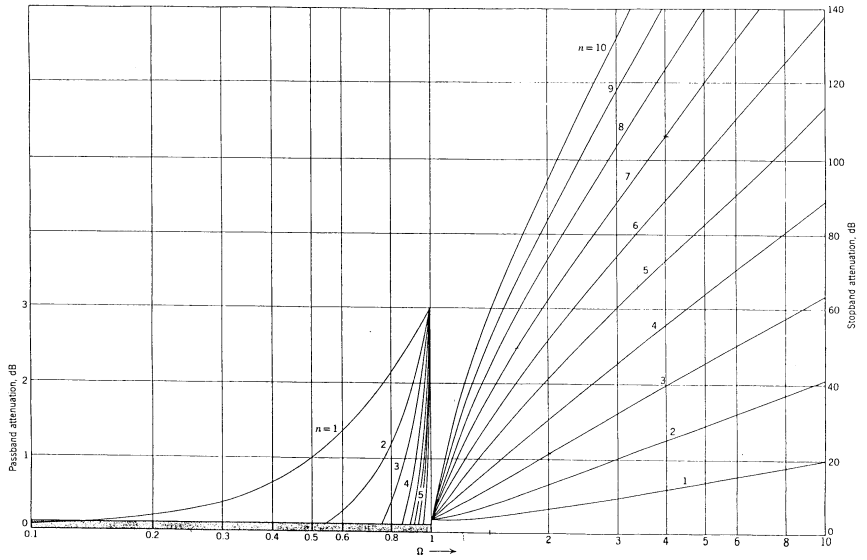


*Figure 2.4.* Attenuation characteristics for Chebychev filter with 0.1 dB ripple.

## 5. Taking a record of data

A record of data is a sequential series of samples acquired by the logic state analyzer (or embedded processing element in the case of built-in self test) interfaced to the ADC. Once acquired, the record of data is transferred to a computer for analysis.

### 5.1 Use of Output Decimation in Taking a Record of Data

In the case of ADCs with very high sampling rate, it may become impractical to store in real time all the samples acquired by the ADC. In this case, it is still possible to operate the ADC at the high sampling rate, while storing only one sample out of D acquired in sequence (1/D output decimation). The set of samples thus collected takes the name of decimated record.

In order to acquire a decimated record, the ADC sampling clock is also used to drive a divide-by-$d$ counter, whose output triggers the acquisition of the sample by the logic analyzer (or by the equivalent hardware).

In the case of output decimation, the decimated sample rate, $f_s/D$, shall be used in all the equations relating the sampling rate to the input frequency (e.g., for equivalent time sampling), but the actual ADC sampling rate $f_s$ shall be quoted as the sampling rate in the test report. When a decimator factor D

is applied, this implies a test time multiplied by D. So, in that case, the lower bound of the integrals used in (2.11) must be changed to $\frac{f_s}{M.D}$.

Output decimation may also be used for tests that do not require waveform reconstruction, such as histogram tests, or for servo-loop tests. In general, it should be remembered that decimation involves a loss of information, which may occasionally hide relevant phenomena, such as hysteresis effects.

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