

# LEPECVD – A Production Technique for SiGe MOSFETs and MODFETs

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## Introduction

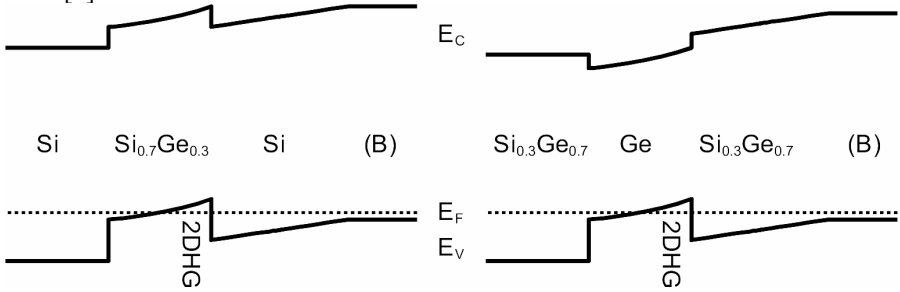
Crystalline silicon germanium alloys greatly extend the potential of silicon-based electronics. Both electron and hole conduction can be enhanced through control of strain, Ge content, and band-gap engineering [1, 2].

Compressive strain results if  $\text{Si}_{1-x}\text{Ge}_x$  is deposited epitaxially on  $\text{Si}_{1-y}\text{Ge}_y$  when  $x > y$ , due to the 4.17% mismatch between Ge and Si lattice constants. A compressively strained  $\text{Si}_{1-x}\text{Ge}_x$  layer forms a quantum well for holes, as shown in the left-hand panel of Figure 1.  $\text{Si}_{1-x}\text{Ge}_x$  layers with  $x$  up to about 0.5 can be grown pseudomorphically (without relaxing the strain imposed by the substrate) on Si, in thicknesses which are useful for electronic applications. However, pure Ge ( $x=1$ ) cannot generally be deposited directly on a Si substrate ( $y=0$ ) without a strain-induced transition to a three-dimensional growth (Stranski–Krastanow) mode after a few monolayers [3]. Furthermore, even in the case of two-dimensional (Frank-van der Merwe) growth there is a limit to how much strain can build up before the strained layer relaxes [4].

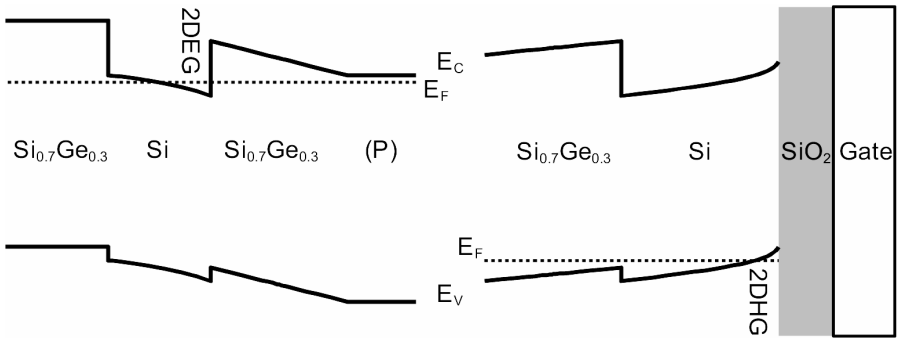
Therefore, the epitaxial two-dimensional growth of a strained Ge-rich layer ( $x \sim 1$ ) of useful thickness directly on a Si substrate is not possible. However, such a layer can be grown on a relaxed  $\text{Si}_{1-y}\text{Ge}_y$  buffer layer, with  $0.5 \leq y < 1.0$ . The band profile in this case is shown in the right-hand panel of Figure 1. The Si substrate plus a relaxed buffer forms a virtual substrate (VS). A VS also allows the growth of a layer under tensile strain ( $x < y$ ) which creates a quantum well for electrons, as shown in the left-hand panel of Figure 2 [2, 5]. Furthermore, tensile-strained Si surfaces are smoother than unstrained Si surfaces because tension increases the surface step energy [6].

Silicon germanium has become a commercially successful technology. Its most mature manifestation is the heterojunction bipolar transistor (HBT), which has the advantages that it is only a minor modification of the Si bipolar transistor and is easily integrated into standard complementary metal-oxide-semiconductor (CMOS) processes. This is known as BiCMOS. A thin layer of SiGe is deposited

pseudomorphically to act as the base of the transistor, and as such this technology is easy to implement. Modern SiGe HBTs can now operate at frequencies above 300 GHz and are used in both radio frequency wireless and cable communications [2].



**Figure 1.** Band profiles of two compressively-strained systems. Left panel: a strained SiGe channel grown pseudomorphically on Si. Right panel: a strained Ge channel grown on a SiGe VS. The growth direction is from left to right, so in both cases, boron doping (B) is above the channel. Holes diffuse into the channel and an electric field is set up between the two-dimensional hole gas (2DHG) and ionized dopant atoms. The dashed line is the Fermi level  $E_F$ , and  $E_C$  and  $E_V$  are the conduction and valence bands, respectively. Band offsets and other parameters can be found in Ref. [5].



**Figure 2.** Band profiles of Si under tensile strain on a relaxed SiGe VS. Left panel: Si under tensile strain forms a quantum well for electrons, so electrons from a phosphorus-doped region (P) diffuse into the Si and a two-dimensional electron gas (2DEG) forms. Right panel: a strained Si surface channel can be biased with a gate, to induce a 2DHG [2, 5].

Strained Si on a VS on the other hand requires the VS to have low surface roughness, a high degree of relaxation, and low defect densities [1]. There exist two fundamentally different approaches for realizing VSs with acceptable properties. A well-established solution to this problem is the graded buffer. The basic concept of grading Si<sub>1-x</sub>Ge<sub>x</sub> alloy layers to some final composition  $x$ , either linearly or step-wise, has proven to be highly successful [7].

Si or Ge quantum wells grown on VSs with thick graded buffers have been demonstrated to have excellent electrical properties [8–10], but there are disadvantages of thick buffers. Firstly, SiGe alloys are poor thermal conductors, leading to

problems of heat dissipation for highly integrated circuits. Secondly, long range surface roughness (with  $\sim 1 \mu\text{m}$  correlation length) due to the so-called “cross-hatch” [11] may cause problems during device processing, and the large step height between regions covered by virtual substrates and bare Si regions hampers integration. Also, a large amount of precursor material is consumed, and in most MBE or CVD systems the growth time is at least a few hours.

For these reasons a second solution is being pursued, which involves thin constant-composition layers. Several concepts have been tried over the past few years to achieve highly relaxed SiGe layers as thin as a hundred nanometers [12, 13]. These methods fall into two categories.

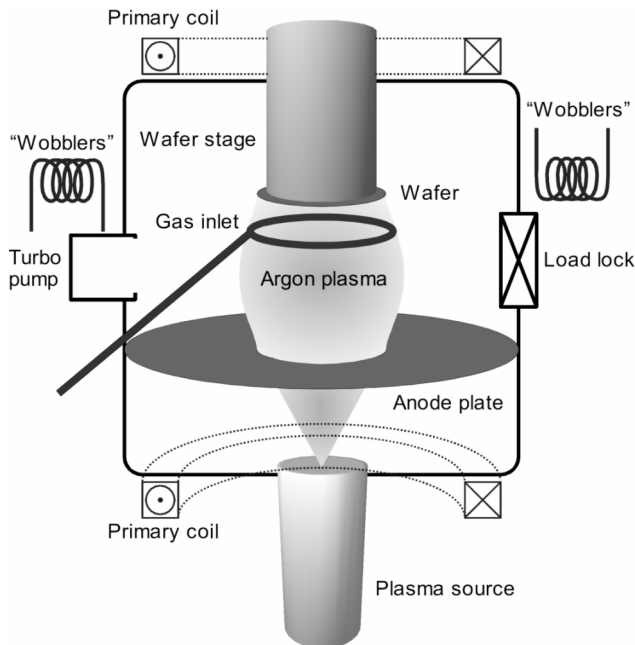
The first involves growth of a Si buffer layer at unusually low substrate temperatures  $T_s$  (around  $400^\circ\text{C}$ ) before the actual SiGe buffer is deposited at higher  $T_s$  [14-16]. This so-called low-temperature Si (LT-Si) layer contains a large number of point defects, the accumulation of which is believed to promote relaxation [17]. Alternatively, the SiGe buffer layer itself may be grown at very low  $T_s$  (below  $200^\circ\text{C}$ ) with essentially a similar effect [18]. The disadvantage here is that long periods of thermal cycling may be needed to achieve a stable state of relaxation. Also, such low-temperature growth cannot be realized by chemical vapor deposition (CVD) since growth rates decrease exponentially as  $T_s$  is reduced. Most work in this field has therefore been carried out with molecular-beam epitaxy (MBE) which is not suitable for high volume Si or SiGe production.

The second approach is based on ion implantation of H or He into a strained SiGe layer, and subsequent thermal treatment [19, 20]. This leads to bubble formation, facilitating dislocation loop nucleation close to the Si/SiGe interface. Except for the extra processing steps, this method appears very attractive, but seems to be limited to buffers with Ge content below 30% [20-22]. In a variation of this, Ar ions can be implanted into the Si substrate before SiGe growth [23].

In this chapter we shall discuss an alternative method suitable for high-volume production of both thick graded buffers and thin buffers. This method is called low-energy plasma-enhanced chemical vapor deposition (LEPECVD) [24].

## LEPECVD

The basic LEPECVD system is shown schematically in Figure 3. A Ta filament in a plasma source attached to the deposition chamber is current-heated to the point of thermionic emission. Ar gas is passed through the source into the chamber, and a high-intensity direct current arc is struck between the source and the chamber. The arc current is of the order of 20-80A but the arc voltage is less than 30 V due to the electron-rich conditions. The plasma is focused onto the substrate with magnetic fields, while the substrate is heated from behind with a graphite heater. Precursor gases are introduced through a ring just below the substrate:  $\text{SiH}_4$  and  $\text{GeH}_4$  are used for SiGe growth, and  $\text{PH}_3$  and  $\text{B}_2\text{H}_6$  (both diluted in Ar) are used for doping;  $\text{H}_2$  can also be used to fine-tune the surface mobility of adatoms.



**Figure 3.** The low-energy plasma-enhanced chemical vapor deposition (LEPECVD) system. A low-voltage high-current dc discharge is sustained between the source and the anode plate. The substrate is exposed to the plasma, but the ion energies are too low to cause any damage.

Epitaxial growth rates for  $\text{Si}_{1-x}\text{Ge}_x$  of any composition can be varied arbitrarily from  $1 \text{ \AA s}^{-1}$  to almost  $10 \text{ nm s}^{-1}$ , at substrate temperatures of  $450\text{--}750^\circ\text{C}$ . The growth rate is controlled both by varying the precursor gas flows and by changing the plasma arc current and the strength of the magnetic confinement field. The growth rate and film composition are effectively independent of substrate temperature. Around 20% of the precursor material is incorporated into the sample under plasma conditions optimized for high growth rates.

The development of LEPECVD was motivated by the need for relaxed SiGe alloy buffer layers epitaxially grown on Si wafers. In the case of chemical vapor deposition (CVD) without plasma, the gaseous precursors decompose on the growing surface. For Si growth at substrate temperatures below  $\sim 800^\circ\text{C}$ , the growth rate is limited by H desorption from the growing surface [25]. In fact, there is an exponential dependence of growth rate on substrate temperature with an activation energy of around  $200 \text{ kJ mol}^{-1}$ . The activation energy for desorption of H from a Ge surface is significantly lower, and this leads to a  $\text{Si}_{1-x}\text{Ge}_x$  growth rate that is strongly dependent on  $x$  as well as temperature, in a non-trivial way. Typical growth rates are  $10\text{--}100 \text{ nm min}^{-1}$  and less than 1% of the silicon and germanium precursor gases is deposited.

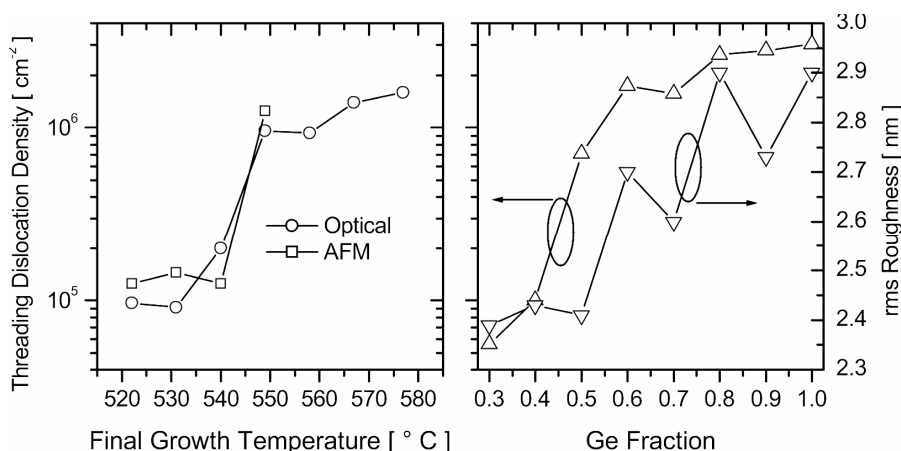
The low energy plasma improves matters in two ways. Firstly, the precursor gases are efficiently decomposed in the plasma column. Secondly, H is desorbed

from the growing surface by ion bombardment. The energy of the ions is however too low ( $\sim 10$  eV) to cause any damage to the crystalline structure of the substrate.

MBE does not suffer from the problem of growth rate dependence on substrate temperature, but since it is a solid-source process it is unsuitable for the industrial growth of thick layers. Typically, the growth chamber vacuum needs to be broken to replenish the sources after  $\sim 5$ -10 VSs have been grown. SiGe MBE growth rates are also usually of the order of  $10$ - $20$  nmmin $^{-1}$  unless special techniques are used [26].

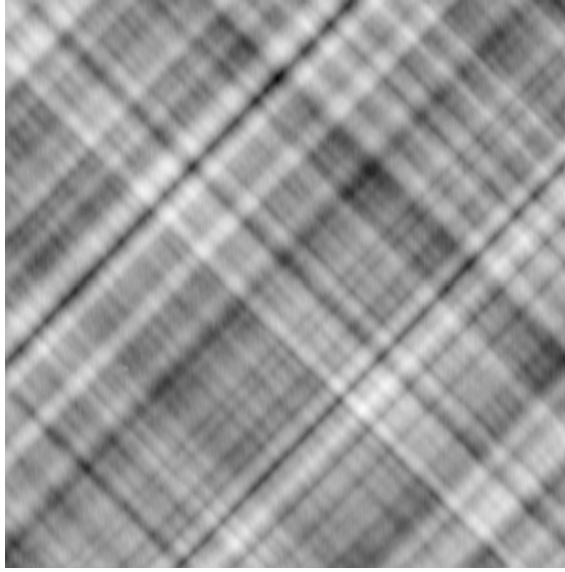
## Applications

### Virtual Substrates



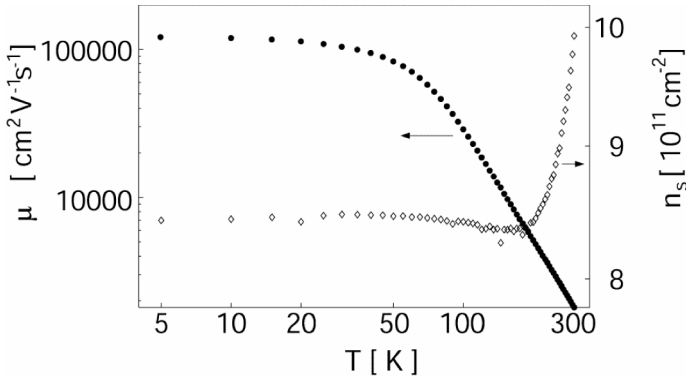
**Figure 4.** Left panel: Threading dislocation density on thick graded ( $x=0.4$ ) VSs grown by LEPECVD as a function of final growth temperature. The grading rate was 7% per micron and the constant composition cap is 1  $\mu$ m thick. Etch pits were counted either with an optical microscope or an AFM. Right panel: Surface roughness and threading dislocation density on thick graded VSs grown by LEPECVD, with optimized temperature profiles.

Growth rates in LEPECVD are not strongly dependent on substrate temperature, so the temperature profile during the growth of a thick VS can be varied to optimize the defect density, as shown in the left-hand panel of Figure 4 for thick VSs graded at 7% per micron to a final Ge content of 40%. Generally, the growth temperature should be reduced as the Ge content increases; it can be seen that with a suitably low final temperature, the threading dislocation density can be reduced to less than  $10^5$  cm $^{-2}$ . The right-hand panel of Figure 4 shows how the roughness and dislocation density of a VS tend to increase as a function of Ge content, up to  $3 \times 10^6$  cm $^{-2}$  for pure Ge. An atomic force microscopy (AFM) image of a thick graded VS (with a final Ge content of 30%) is shown in Figure 5. The rms roughness is 2.6 nm. For comparison, a 50% graded VS grown by UHVCVD has an rms roughness of 37 nm [29].



**Figure 5.** Atomic force microscopy (AFM) image of a 6  $\mu\text{m}$  thick VS graded from 0 to 30% (sample 7208). The image size is  $25 \times 25 \mu\text{m}$ . Root mean square (rms) roughness is 2.6 nm and the total height range is 15.6 nm.

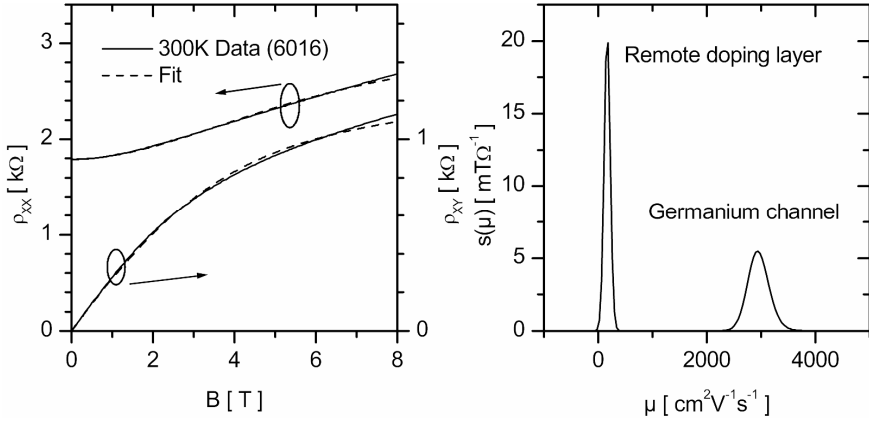
LEPECVD has also been used to grow thin buffers which are suitable for n-MODFETs [13, 30, 31]. At 500nm, the buffers are 5-10 times thinner than standard graded buffers. The buffers are grown in one step, at a high growth rate and a low substrate temperature. Neither complicated thermal cycling nor ion implantation is required. Chemical-mechanical polishing is also unnecessary.



**Figure 6.** Hall mobility (filled symbols) and hole sheet density (open symbols) of a strained Ge p-MODQW structure on a relaxed linearly-graded SiGe buffer (sample 6745).

The combination of high growth rate and low substrate temperature allows a high degree of strain to accumulate in the  $\text{Si}_{1-x}\text{Ge}_x$  layer during growth, and this

may lead to a higher dislocation glide velocity which facilitates a high degree of relaxation. Molecular dynamics simulations suggest that the nature of the dislocation core is strain dependent [32], with more mobile cores forming under high strain.

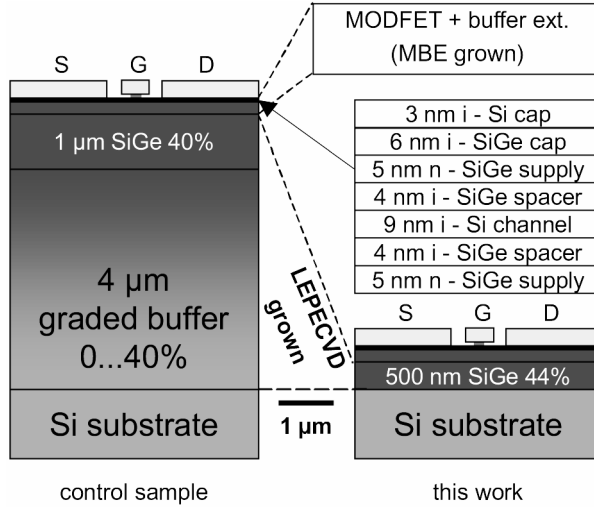


**Figure 7.** Left panel: Longitudinal and transverse magnetoresistance measured at 300K on a strained Ge p-MODQW structure, together with fit from a calculated mobility spectrum [27, 28] shown on the right. Right panel: Mobility spectrum obtained for sample 6016 at 300 K from the magnetoresistance shown on the left. Channel mobility is 2940 cm<sup>2</sup>V<sup>-1</sup>s<sup>-1</sup> at a hole density of  $5.7 \times 10^{11}$  cm<sup>-2</sup>.

### Hole Mobility Enhancement

Traditionally, the speed of CMOS has been limited by the poor hole mobility of Si, relative to the electron mobility. Since Ge has one of the highest hole mobilities of any semiconductor, SiGe is an obvious choice for p-channel devices. A complete p-HMOSFET (heterostructure-MOSFET) layer structure with a Ge-rich channel has been grown by LEPECVD [33]. Transistors fabricated on this material demonstrate effective hole mobilities at room temperature which approach the Si electron mobility.

Alloy scattering means that the best hole mobilities should be seen in pure Ge channels [34, 35]. Modulation-doped p-channel quantum wells (p-MODQWs) grown by LEPECVD, with strained Ge channels on Si<sub>0.3</sub>Ge<sub>0.7</sub> VSSs, have a maximum low-temperature (2 K) mobility (Figure 6) of 120,000 cm<sup>2</sup>V<sup>-1</sup>s<sup>-1</sup> at a sheet density of  $8.5 \times 10^{11}$  cm<sup>-2</sup>. These structures were front-side doped (with the dopant above the channel). Optimization of the growth temperature and use of hydrogen means that the upper heterointerface was very smooth. The mobility is a factor of two greater than the best p-type Ge channel mobility result demonstrated on material grown by MBE [10]. There, the doping had to be introduced underneath the channel (probably leading to dopant segregation into the channel) since the upper interface was of lower quality due to strain-induced roughening. Our results also evince the quality of the VS, in terms of threading dislocation density and surface roughness.



**Figure 8.** Schematic of the MODFET structures grown on a conventional thick graded VS (left) and on the novel thin VS (right), drawn to scale. The inset shows the stack of the active layers. A buffer extension of 150 nm was grown by MBE before the active layers.

Room temperature channel mobilities have been extracted from the magnetic field dependence of the conductivity and Hall coefficient (Figure 7). The right-hand panel of Figure 7 shows a mobility spectrum of a strained Ge p-MODQW structure on a relaxed linearly-graded SiGe buffer (sample 6016) at 300 K, found from the data in the left-hand panel. Two peaks are evident, corresponding to conduction in the strained Ge channel ( $2940 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$ ) and the boron-doped supply layer ( $180 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$ ). By integrating these peaks, the carrier sheet densities are found to be  $5.7 \times 10^{11} \text{ cm}^{-2}$  in the channel and  $1.0 \times 10^{13} \text{ cm}^{-2}$  in the supply layer [27, 28]. Similar values for the channel mobility have been found by mobility spectrum analysis in strained Ge structures grown with other techniques [37, 38].

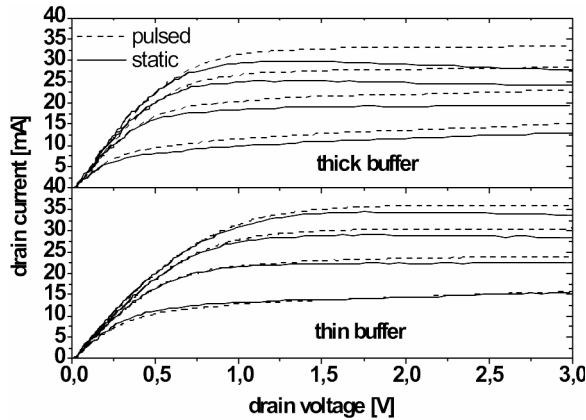
In addition, Si under tensile strain should feature enhanced hole mobility over unstrained Si due to a reduction of effective mass [34]. However, since tensile-strained Si on SiGe does not form a quantum well for holes then a surface channel must be induced using the field effect, as shown in the right-hand panel of Figure 2 [2].

### Electron-channel Devices

Modulation-doped n-channel FETs (n-MODFETs) and n-MODQWs have been fabricated using a combined LEPECVD+MBE process: a buffer is grown by LEPECVD and then the electrically active structure is grown by solid-source MBE [39-41]. This combines the advantages of LEPECVD (high growth rates for high-quality VS production) with the advantages of MBE (good control of n-type doping and concentration profiles).

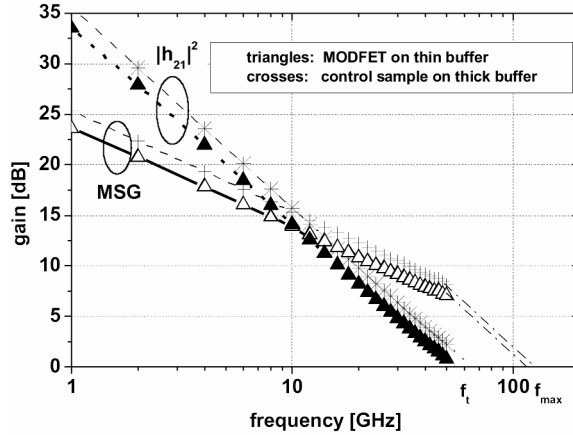


The active MODFET layer stack was grown by MBE at a constant temperature of 540°C and a rate of 0.25 nm s<sup>-1</sup> for SiGe or 0.15 nm s<sup>-1</sup> for Si. The double-sided modulation-doped structure is formed by a 9 nm strained Si channel, embedded in 4 nm doping setback SiGe layers and 5 nm Sb doped SiGe supply layers. Doping was achieved by secondary implantation (DSI) [42]. Device processing included isolation by dry mesa etching, deposition of SiO<sub>2</sub> as a field oxide, window opening by wet chemical etching, P implantation and thermal activation in the ohmic contact region, deposition and lift-off of the Ti/Pt/Au source and drain contacts and finally definition of the Pt/Au Schottky gate by means of electron-beam lithography. The smallest structures have a gate length  $l_G=70$  nm and a source-drain distance  $d_{SD}=1$  μm [30].



**Figure 9.** Comparison of the MODFET output characteristics on thin and thick relaxed LEPECVD-grown Si<sub>0.6</sub>Ge<sub>0.4</sub> buffers (lower and upper curves, respectively) under static and pulsed conditions. The gate voltage  $V_G$  was varied between -0.6 and +0.6 V in steps of 0.4 V.

A comparison of thick and thin VS structures is shown in Figure 8, and device characteristics are shown in Figures 9 and 10. The lower and upper set of curves in Figure 9 show the  $I$ - $V$  characteristics of 100 μm wide devices prepared on the thin and the thick LEPECVD-grown buffer, respectively. The measurements were performed both under static and pulsed conditions. The pulse width was 200 ns. Drain saturation currents  $I_{DSS}$  of more than 300 mA/mm and a maximum transconductance of  $g_m=230$  mS/mm have been achieved in both cases. The divergence between the DC and pulsed currents is much larger for the thick buffer. At full enhancement (drain voltage  $V_D=3$  V, gate voltage  $V_G=+0.6$  V) a current difference of 17% can be derived from the uppermost curves, which has to be compared to only 6% in the case of the thin buffer. This indicates a significant reduction of self-heating from the ten-fold decrease of buffer thickness. The difference in the self-heating effect by a factor of approximately three is in good agreement with the rough estimation that the thermal resistance of a device on a relaxed SiGe buffer is proportional to the square root of the buffer thickness [43]. Taking this into account a device temperature reduction of 70 K can be estimated by applying the thin VS.



**Figure 10.** De-embedded current gain  $|h_{21}|$  and maximum stable gain  $MSG$  spectra of 100  $\mu\text{m}$  wide devices. Transit frequencies of  $f_T=55\text{ GHz}/63\text{ GHz}$  and maximum frequencies of oscillation  $f_{max}(MSG)=113\text{ GHz}/128\text{ GHz}$  can be derived for devices on thin and thick VS, respectively.

The current gain  $h_{21}$  and the maximum stable gain (MSG) of 100  $\mu\text{m}$  wide devices are shown in Figure 10. By extrapolating the current gain, a transit frequency  $f_T=55\text{ GHz}$  can be derived for the transistors on the thin VS. The results are comparable to the cut-off frequency of the thick buffer control device having an  $f_T$  of 63 GHz. By using the acknowledged procedure of extrapolating MSG with a slope of 10dB/decade up to the point where the stability factor  $k$  reaches 1 and further extrapolation of the maximum available MAG with 20 dB/decade, maximum frequencies of oscillation  $f_{max}(MAG)=113\text{ GHz}$  and 128 GHz are achieved for the thin and thick buffer device. Assuming reflection-free input and output matching, cutoff frequencies of  $f_{max}(U)=138\text{ GHz}$  and 144 GHz can be derived from the 10 dB transits of Mason's gain  $U$  (for clarity not shown in Figure 10), respectively. High-frequency performance is not degraded significantly by a ten-fold reduction in buffer thickness; in fact, LEPECVD-grown thin VSs are competitive with thin VSs produced both low-temperature epitaxy and He implantation [13].

## Conclusions

LEPECVD is a new process for epitaxy of SiGe at rates of several nanometres per second. Growth rates are independent of alloy composition and substrate temperature, giving the maximum freedom for optimization of growth parameters. Being a gas source process, it is suitable for industrial production of electronic device-grade material.

High quality n-MODFETs have been produced in mixed LEPECVD+MBE technology [41], and a novel thin VS design (which is made possible by the high growth rates available in LEPECVD even at low substrate temperature) allows access to the advantages of strained Si without the disadvantages of thick graded SiGe layers [30].

High effective mobilities have been demonstrated at room temperature in p-HMOSFETs [33], and exceptional mobilities have been demonstrated in p-MODQW structures at low temperature [36].

## Acknowledgements

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