

Preface

Although the Integrated circuit (IC) was invented in 1958 by Jack Kilby of Texas Instruments (mesa process with germanium) and Bob Noyce of Fairchild (planar process with silicon), it was not until the mid-later 1960s that the bipolar IC and then, in the early 1970s, the MOSFET IC significantly entered the production scene. Pat Haggerty's vision at Texas Instruments of the pervasiveness of the microelectronics revolution, the concept of the learning curve and market elasticity in the early 1960s was of immeasurable significance to the fledging IC industry. Concurrently, projection of the memory bit per chip with time by Gordon Moore at Fairchild in 1965 – the number of transistors per IC doubles every year (updated by Moore at Intel in 1975 to about 18 months and, subsequently, re-assessed in 1995) – gave impetus to the industry that a viable market was indeed the case. These business oriented issues, coupled with Bob Dennard's one transistor / one capacitor dynamic ram memory cell (DRAM) at IBM in 1968 and the related scaling methodology established the basis for the growth of the MOSFET industry for the next thirty plus years.

The IC industry has sustained the above scaling methodology (critical feature reduction), in conjunction with the introduction of complementary metal oxide semiconductors (CMOS) and appropriate improvements in layout design through the end of the last century. We have now reached the point, however, where the conventional scaling methodology utilizing silicon dioxide (SiO_2) and subsequently silicon oxynitride (SiO_xN_y) has essentially reached the tolerable power limit for high-performance MOSFET ICs and stand-by (direct tunneling) leakage current for low-power applications such as cell phones and notebook computers. An alternative to the conventional silicon oxynitride gate dielectric (which typically is in the range of 0.8–1.5 nm physical thickness) is required to obviate the degradation in IC performance.

This monograph presents a perspective on the gate dielectric and the approaches in progress to rectify the above noted issues. That is, increasing the physical thickness of the gate dielectric to significantly reduce the power and direct-tunneling current issues while enabling the continued reduction in the electrically active gate dielectric thickness by utilizing high-k dielectric constant materials. The high-k materials facilitate both an increased physical thickness and a reduction in the electrical thickness to maintain the requisite scaling methodology. The latter is generally referred to as the equivalent

oxide thickness (EOT). This monograph, however, is envisioned to be more than just a current view of these alternative high-k gate dielectric approaches. Rather, both previous and present directions related to scaling the gate dielectric and their impact, along with the creative directions and future challenges defining the direction of high-k gate dielectric scaling methodology, will be reviewed.

The monograph is introduced by a comprehensive review of Moore's law by Dan Hutcheson and then is divided into four parts. The first part reviews the classical regime of SiO_2 , including a brief historical note by the late Else Kooi, kindly re-assessed by Albert Schmitz. Gene Irene then presents a comprehensive review of SiO_2 -based MOSFETs, followed by Robin Degraeve's assessment of SiO_2 reliability methodologies. Part 2 describes the transition to silicon oxynitrides as the gate dielectric. Shih-Hsien Lo and Yuan Taur review the gate dielectric scaling methodologies in the transition from 2.0 towards 1.0 nm as regards their implications for device performance. Thomas Skotnicki and Frederic Boeuf then review "optimal" device scaling methodologies for SiO_2 and silicon oxynitride by reminding us that we may not necessarily desire nor are required to scale every feature to its limit for a given technology generation as defined in the *International Technology Roadmap for Semiconductors* (ITRS). Finally, Hsing-Huang Tseng reviews the state-of-the-art for silicon oxynitride to both reduce gate leakage and boron penetration from a boron doped polysilicon gate electrode.

Part 3 addresses the transition to high-k gate dielectrics with an EOT less than 1 nm with eleven articles. Initially, Jon-Paul Maria discusses a variety of criteria for selecting alternative high-k gate dielectrics. Bob Wallace and Glen Wilk then discuss a host of materials issues for high-k gate dielectric selection and their integration with planar CMOS processes. Gregory Parsons reviews the role of interface composition and structure for the high-k gate dielectrics. In a complementary fashion, Gerry Lucovsky and Jerry Whitten discuss the electronic structure of a variety of high-k gate dielectrics and correlations amongst them. Andrei Istratov and Eicke Weber then review a host of physical-chemical properties of selected 4d, 5d and rare-earth metals in silicon.

Part 3 continues with a review of the deposition of high-k films by Jane Chang followed by Veena Misra's review of metal gate electrode materials compatible with the high-k gate dielectrics. Luigi Colombo, Antonio Roton-daro, Mark Visokay and James Chambers discuss CMOS IC fabrication issues for both the high-k gate dielectric and metal gate electrode materials. Alain Diebold and William Chism discuss the characterization and metrology of these high-k gate dielectric constant materials followed by George Brown's review of electrical measurements for the high-k gate films. Finally, Yang Yu Fan, Sivakumar Mudanai, Wanqiang Chen, Leonard Register and Sanjay Banerjee discuss the utilization of the high-k materials in IC design and related issues.

Part 4 addresses future directions for advanced technology generations. Fred Walker and Rodney McKee discuss high-k crystalline gate dielectrics from a research perspective. Ravi Droopad, Kurt Eisenbeiser and Alex Demkov then discuss the utilization of high-k crystalline gate dielectrics from an IC manufacturer's perspective. Finally, a roll-up of the high-k gate dielectrics with a host of related device alternatives is discussed for advanced MOSFET devices by Jeff Bokor, Tsu-Jae King, Jack Hergenrother, Jeff Bude, Dave Muller, Thomas Skotnicki, Stephan Monfray and Greg Timp.

The challenges of high-k gate dielectrics is one of the most critical issues in the evolving ITRS. The vision, experience and wisdom the authors have summarized will help succeed in ensuring this monograph is a timely, relevant, interesting and resourceful book focusing on both the fundamentals and evolving directions to ensure the successful integration of high-k gate dielectrics and metal gate electrodes in future ICs as envisioned in the ITRS.

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