

Chapter 2

IMPROVED MULTIRATE POLYPHASE-BASED INTERPOLATION STRUCTURES

1. INTRODUCTION

The design of improved SC structures for interpolating filtering embraces first the speed relaxation and number reduction of the opamps in the circuit for the optimum-class multirate realization, and secondly the elimination of the input lower-rate S/H shaping effect which then leads the SDA interpolation to operate in a similar manner as its digital counterpart. Previously available SC interpolator structures cannot fulfill all the above requirements [2.1, 2.2, 2.3, 2.4, 2.5, 2.6, 2.7, 2.8, 2.9, 2.10].

This chapter will first characterize the conventional sampled-data analog interpolation with its input lower-rate S/H shaping distortion and propose the ideal improved analog interpolation model and its traditional bi-phase SC structure. Then, by proving first the effectiveness of the employment of multirate polyphase structure for optimum-class improved analog interpolation that will completely get rid of the input lower-rate S/H shaping effect in the entire frequency axis, a family of multirate SC structures with increased speed, power and silicon area efficiency for IC realizations, namely, Active Delayed-Block (ADB) polyphase-based structures, will be proposed by combining the novel input sampling technique and the Direct-Form (DF) polyphase structures with original digital prototype interpolation filtering transfer function [2.11, 2.12, 2.13]. Two types of SC structure will be presented one employing a novel L-output-accumulator suitable for high-frequency operation, and the other using a one-output-accumulator yielding a reduced component count. Both canonic- and non-canonic-forms ADB polyphase structures with respect to the required actual delay terms for

ADB's will be proposed for both higher-order linear-phase FIR and high-selectivity/wideband IIR interpolation functions. Moreover, the specific low-sensitivity IIR multirate structures will also be investigated for higher-order filtering.

2. CONVENTIONAL AND IMPROVED ANALOG INTERPOLATION

Interpolation by a factor L corresponds to the process of sampling rate increase from f_s to Lf_s . Pure digital implementation of interpolation comprehends the combined operation of an up-sampler, for increasing the sampling rate from f_s to Lf_s , and inserting $(L-1)$ zero-valued samples between two consecutive input samples, and an interpolation filter for removing the unwanted frequency-translated image components associated with the signal sampled at the input lower rate. The spectrum of the resulting ideal output interpolated samples $x_{it}[nT_{it}]$ is given by

$$X_{it}(e^{j\omega}) = X_e(e^{j\omega}) \cdot H(e^{j\omega}) = X(e^{j\omega L}) \cdot H(e^{j\omega}), \quad \omega = \Omega T_{it} = \Omega T_s / L \quad (2.1)$$

where $X_e(e^{j\omega})$ and $X(e^{j\omega L})$, are, respectively, the spectrum of the up-sampled and the original samples, and $H(e^{j\omega})$ is the ideal frequency response of the interpolation filter (gain = L , cutoff frequency $\omega_c = \pi / L$). Therefore, an ideal S/H interpolated output signal $x_{it}(t)$ can be obtained by passing such interpolated samples through an ideal hold circuit, and its spectrum is represented by

$$X_{it}(j\Omega) = X_{it}(e^{j\Omega T_{it}}) \cdot \frac{T_{it} \sin(\Omega T_{it} / 2)}{\Omega T_{it} / 2} e^{-j\Omega T_{it} / 2} \quad (2.2)$$

In the (sampled-data) analog case, the exact interpolation (as in the above digital case) is not possible due to the input S/H signal, then it must be described by the conventional analog interpolation model in Figure 2-1(a). The analog interpolating filter, which can be analyzed as a discrete-time processor operating at Lf_s with an output hold at Lf_s , will sample and process the input signal at Lf_s (thus having L successive equal-value samples owing to the constant-held input within a full sampling period $1/f_s$) and its operation is depicted in Figure 2-1(b), both in time and frequency domains. The spectrum of the input S/H samples $x'_e[nT_{it}]$ can be expressed in terms of the spectrum of the up-sampled discrete samples $x_e[nT_{it}]$ by

$$X'_e(e^{j\omega}) = X_e(e^{j\omega}) \cdot H_{SD}^0(e^{j\omega}) \quad (2.3)$$

where

$$H_{SD}^0(e^{j\omega}) = \frac{\sin(\omega L/2)}{\sin(\omega/2)} \cdot e^{-j(L-1)\frac{\omega}{2}}, \quad \omega = \Omega T_{it} \quad (2.4)$$

in which $|H_{SD}^0(e^{j\omega})| = L$, for $\omega = 0$.

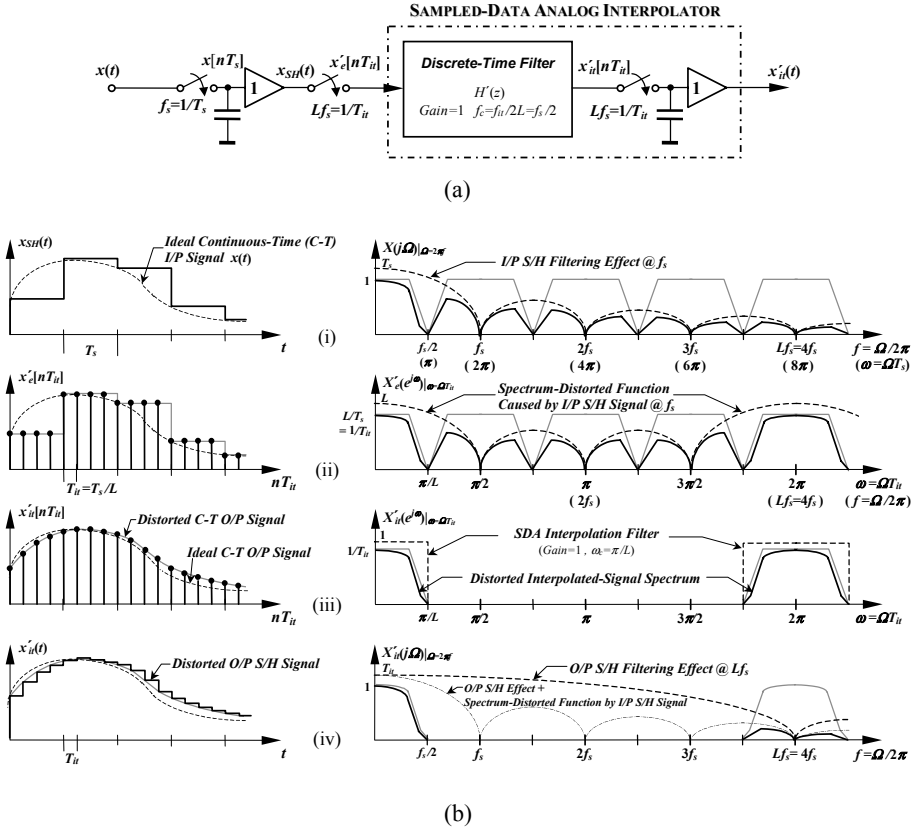


Figure 2-1. Conventional analog L-fold interpolation (a) Architecture model (b) Time- and frequency-domain illustration

From (2.4), the spectrum of the processed samples in an analog interpolation, as illustrated in (b-ii) of Figure 2-1, is a deformed version of $X_e(e^{j\omega})$ due to the multiplication by $H_{SD}^0(e^{j\omega})$ which is referred as Spectrum-Distorted function with a DC gain of L caused by the sampling of the constant-held input. Thus, a unity-gain interpolation filter ($H'(e^{j\omega}) = H(e^{j\omega})/L$) must be employed to process such samples, and the

spectrum of the resulting output interpolated samples $x'_{it}[nT_{it}]$ is expressed as

$$\begin{aligned} X'_{it}(e^{j\omega}) &= X'_e(e^{j\omega}) \cdot H'(e^{j\omega}) \\ &= X_e(e^{j\omega}) \cdot H_{SD}^0(e^{j\omega}) \cdot H'(e^{j\omega}), \quad \omega = \Omega T_{it} \end{aligned} \quad (2.5)$$

which indicates that the spectrum of the output samples possesses an extra deformation due to the Spectrum-Distorted Function $H_{SD}^0(e^{j\omega})$, as shown in (b-iii) of Figure 2-1. After taking into account the inherent output S/H filtering effect at higher sampling rate, the spectrum of the distorted S/H output signal $x'_{it}(t)$ shown in (b-iv) of Figure 2-1 can finally be represented by

$$X'_{it}(j\Omega) = X_{it}(e^{j\Omega T_{it}}) \cdot \frac{T_s \cdot \sin(\Omega T_s / 2)}{\Omega T_s / 2} e^{-j\frac{\Omega T_s}{2}} \quad (2.6a)$$

or

$$X'_{it}(j\Omega) = X_{it}(j\Omega) \cdot \left(\frac{1}{L} \cdot H_{SD}^0(e^{j\Omega T_{it}}) \right) \quad (2.6b)$$

in terms of the ideal interpolated discrete samples or the S/H signal, respectively. Obviously, for an integer sampling rate increase, an L-fold analog interpolation is just equivalent to an ideal L-fold digital interpolation plus the S/H ($\sin x/x$) effects, that are no longer, and as normal, at the higher output sampling rate (like in (2.3) for the ideal case) but at the lower input sampling rate. In other words, from (2.6b), the final output sample-and-held signal of analog interpolation suffers from an extra distortion due to this input-S/H-induced Spectrum-Distorted Function.

Such additional fixed-shaping spectrum distortion usually gives rise to a significant rolloff deformation in the passband, when the baseband signal is wide or close to the lower input sampling rate which is usually the case for high-speed applications (like video systems). Also, this affects the overall system response when frequency-translated bandpass processing is required (like subsampling in wireless communications). Hence, an improved analog interpolation is presented in Figure 2-2(a) destined to eliminate such frequency shaping distortion, thus leading to an increased simplification and freedom in the design of both the passband and the stopband. Although the input signal is still sampled-and-held at lower rate, the ideal overall interpolation performance will be exactly equivalent to a digital interpolation, apart from the S/H effect at the higher sampling rate that is always present in sampled-data analog systems.

A simple SC implementation of this improved analog interpolation is illustrated in Figure 2-2(b) which combines a bi-phase SC filter operating at Lf_s with a special sampling by a front two-switch input interface that operates as an up-sampler by forcing the circuit input to connect to ground at the appropriate time, thus generating zero-valued samples. However, this approach belongs clearly to the non-optimum-class of implementation since the filter core needs to operate at the highest sampling rate of the overall system, and also, an additional DC gain (with value L) is necessary in the filter thus rendering inefficient coefficient spread which leads to large power and area consumption.

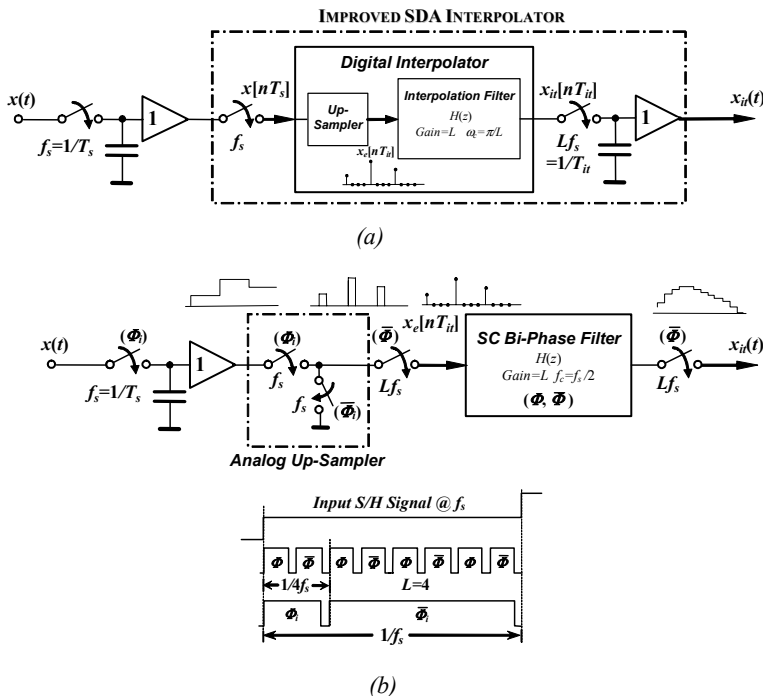


Figure 2-2. Improved Analog interpolation with reduced S/H effects (a) Architecture Model (b) Non-optimum SC implementation with a high-rate Bi-Phase filter

3. POLYPHASE STRUCTURES FOR OPTIMUM-CLASS IMPROVED ANALOG INTERPOLATION

An optimum-class realization of the improved analog interpolation, without lower input-rate S/H shaping distortion, can be achieved by employing polyphase decomposition which is an efficient and straightforward structure utilized in digital multirate filters [2.14, 2.15, 2.16]. Such realization, based on the original digital prototype interpolating transfer function without any modification, takes advantage of the inherent multirate property and allows the main filter core to operate, effectively, at the lowest sampling rate of the system, thus being appropriate for high-frequency filtering with added efficiency in terms of power and silicon area savings as well as circuit design headroom.

The interpolation can be realized with both Finite Impulse Response (FIR) and Infinite Impulse Response (IIR) filtering functions normally for lower-selectivity or linear-phase and higher-selectivity or wide-stopband applications, respectively. For FIR realization, the polyphase multirate structure can be derived from the original FIR filter by decomposing it into L (interpolation factor) polyphase subfilters $H_m(z)$ ($m=0,1,\dots,L-1$), according to

$$H(z) = \sum_{n=0}^{N-1} h_n \cdot z^{-n} = \sum_{m=0}^{L-1} H_m(z) \cdot z^{-m} = \sum_{m=0}^{L-1} \left(\sum_{i=0}^{I_m-1} h_{m+iL} z^{-iL} \right) \cdot z^{-m} \quad (2.7a)$$

where

$$I_m = \left\lceil \frac{N-m}{L} \right\rceil \quad (\lfloor x \rfloor \text{ denotes the minimum integer greater than or equal to } x) \quad (2.7b)$$

and the unit delay refers to the higher output sampling rate $1/Lf_s$. Each polyphase filter, whose coefficients correspond to the L -fold decimated versions of original filter impulse response, approximates an all-pass function and each value of m corresponds to a different phase shift network. Hence, they all efficiently operate at input lower sampling rate and contribute with one nonzero output for each, which corresponds to one of the L outputs of the interpolating filter generated in a sweep mode from the zeroth to the L^{th} polyphase filter by an output counter-clockwise commutator (at output higher rate) for each input sample [2.11, 2.12, 2.13].

Each polyphase filter can be simply implemented by Direct-Form (DF), thus being designated as *DF polyphase* structure. For simplicity, this is illustrated in Figure 2-3 with an example that demonstrates the effectiveness of the polyphase structure to achieve optimum-class improved interpolation filtering. Supposing that an input signal is required to be 2-fold interpolated with respect to a simple 3-tap FIR function, then the original digital transfer function of the interpolation filter is decomposed into a set of L polyphase filters $\{H_m(z), m=0, 1\}$, leading to the resulting polyphase structure of Figure 2-3, where all polyphase filters are realized with a DF structure.

The first polyphase filter produces an output sample given by

$$x_{it}[nT_{it}] = h_0 \cdot x[nT_{it}] + h_2 \cdot x[(n-2)T_{it}] \quad (2.8a)$$

which is equivalent to multiply the coefficient h_1 by a zero-valued sample. Similarly, since the second polyphase filter produces an output sample given by

$$x_{it}[(n+1)T_{it}] = h_1 \cdot x[(n+1)T_{it}] \quad (2.8b)$$

where $x[nT_{it}] = x[(n+1)T_{it}]$

it is also equivalent to multiplying by zero the coefficients h_0 and h_2 . Thus, such operation is equivalent to a digital interpolation where its zero-valued samples need to be created by a digital up-sampler.

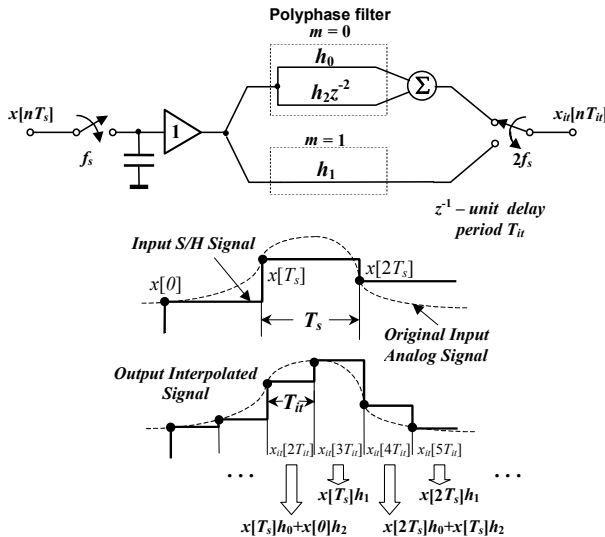


Figure 2-3. Improved analog interpolation with Optimum-class realization by Direct-Form polyphase structure ($L=2$)

In general, it is concluded that the DF polyphase interpolation, with original digital prototype transfer function, implements an improved analog interpolation without the input S/H filtering effect. Since every polyphase filter inherently operates at the lower input sampling rate, the input held signal is only sampled by the interpolator once per period. This also explains why the input S/H effect don't affect the overall system response of the polyphase-structure-based interpolation.

4. MULTIRATE ADB POLYPHASE STRUCTURES

4.1 Canonic and Non-Canonic ADB Realizations

DF polyphase structure is appropriate only when the FIR filter length N is not much greater than the interpolation factor L , e.g. $N \leq 2L$, since it leads to circuits having a rather large number of time-interleaved SC branches and switching phases, which increase not only its complexity beyond practical acceptable limits but the sensitivity to mismatch of capacitance ratios and switch timing. Hence, a more general architecture, designated by Active-Delayed Block (ADB) was introduced [2.17, 2.18] that is a polyphase-based structure to overcome such limitations for filter length $N > 2L$. Such ADB polyphase structure can be implemented in Canonic and Non-Canonic form with easy adaption to both FIR and IIR realizations.

4.1.1 FIR System Response

The FIR transfer function can be canonically decomposed in $B_c + 1$ blocks, each with only L coefficients, and it can be expressed as

$$H(z) = \sum_{n=0}^{N-1} h_n z^{-n} = \sum_{b=0}^{B_c} G_b(z) \cdot (z^{-L})^b = \sum_{b=0}^{B_c} \left(\sum_{n=0}^{L-1} h_{n+bL} z^{-n} \right) \cdot (z^{-L})^b \quad (2.9a)$$

where

$$B_c = \left\lfloor \frac{N-L}{L} \right\rfloor, \quad (2.9b)$$

The elements in each block b will have at least b delay terms z^{-L} (except $b=0$) that will be implemented by an SC ADB. Since each block $G_b(z)$ containing L coefficients (except the last block, $b=B_c$, which contains only $N-B_cL$ terms) can be decomposed again in a polyphase subfilter, that can be realized in DF structure with the sharing of a low speed serial ADB delay line composed by regular z^{-L} units, this structure is designated as *Canonic ADB Polyphase* structure [2.18].

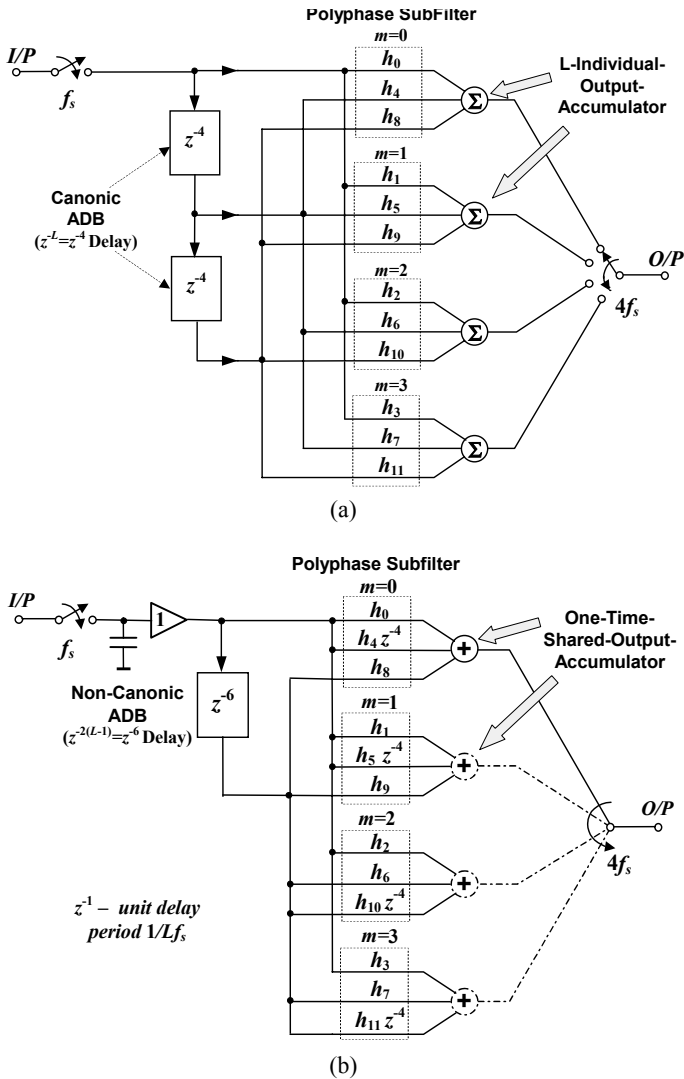


Figure 2-4. (a) Canonic-form (b) Non-canonic-form ADB polyphase structures for improved 4-fold 12-tap FIR interpolator

Minimizing the number of opamps in the ADB-based architecture can be achieved by reducing the number of both ADB's and accumulators, this can be obtained by decomposing the transfer function into blocks – $G_b(z)$ with more-than- L coefficients while making their shared delays larger than regular unit z^{-L} . Such realization is referred to as *Non-Canonic ADB Polyphase* structure, and can be obtained by decomposing the transfer function of an interpolation filter into $B_{nc}+1$ blocks, each with at most $2(L-1)$ coefficients, yielding

$$H(z) = \sum_{n=0}^{N-1} h_n z^{-n} = \sum_{b=0}^{B_{nc}} G_b(z) \cdot (z^{-2(L-1)})^b = \sum_{b=0}^{B_{nc}} \left(\sum_{n=0}^{2(L-1)-1} h_{n+b \cdot 2(L-1)} z^{-n} \right) \cdot (z^{-2(L-1)})^b \quad (2.10a)$$

where

$$B_{nc} = \left\lfloor \frac{N - 2(L-1)}{2(L-1)} \right\rfloor \quad (2.10b)$$

Figure 2-4(a) and (b) presents the corresponding non-recursive ADB polyphase structures for a 12-tap 4-fold FIR interpolating filter in canonic- and non-canonic-forms where the number of ADB's are respectively 2 and 1 according to (2.9b) and (2.10b). An L-individual-output-accumulator approach can be adopted for the canonic-form structure that is particularly suitable for high-frequency SC implementation, while only one time-shared accumulator is needed for non-canonic realization.

4.1.2 IIR System Response

For the optimum-class of IIR analog interpolation, the polyphase decomposition leads also to the most efficient and straightforward structure. The original prototype D^{th} -order denominator and $(N-1)^{\text{th}}$ -order numerator IIR transfer function needs to be modified according to the multirate transformation so as to restrict the composition of the denominator to only powers of z^{-L} [2.14, 2.19, 2.20, 2.21]. Consequently, the original and modified transfer functions can be expressed, respectively, as

$$H(z) = \frac{N(z)}{D(z)} = \frac{\sum_{i=0}^{N-1} a_i z^{-i}}{1 - \sum_{j=1}^D b_j z^{-j}} \quad (2.11)$$

and

$$\hat{H}(z) = \frac{\hat{N}(z)}{\hat{D}(z)} = \frac{\sum_{i=0}^{(N-1)+D(L-1)} A_i z^{-i}}{1 - \sum_{j=1}^D B_{jL} (z^{-L})^j} \quad (2.12)$$

The particular form of (2.11), which allows the recursive part to operate at the lower input sampling rate, can be constructed by combining a non-recursive ADB polyphase structure together with a recursive Direct-Form II (DFII) structure for realizing, respectively, the numerator and the denominator polynomials. Such architecture, where the common delay blocks z^{-L} are realized by a low speed ADB serial delay line and are efficiently shared by both recursive and non-recursive parts, can be referred to as *Recursive-ADB (R-ADB) Polyphase* structure [2.21]. This offers a more general, straightforward and flexible design with enhanced efficiency in terms of amplifier speed and number of phases when compared with previous structures [2.6, 2.7, 2.10].

Like in the FIR counterpart, this R-ADB polyphase structure can also be implemented in canonic and non-canonic forms categorized by the corresponding delay of the shared ADB's. The former has L unit delays whereas the latter requires delays of $2(L-1)$ (except the 1st block that has always a unity delay). Thus, for a general case ($D \neq N-1$), the IIR modified transfer function in canonic form, which requires $\max(B_{cn}, B_{cd})$ SC ADB's can be reformulated as

$$\hat{H}(z) = \frac{\sum_{j=0}^{B_{cn}} \left(\sum_{i=0}^{L-1} A_{i+jL} z^{-i} \right) \cdot (z^{-L})^j}{1 - \sum_{j=1}^{B_{cd}} B_{jL} (z^{-L})^j} \quad (2.13a)$$

where

$$B_{cn} = \left\lfloor \frac{N + D(L-1) - L}{L} \right\rfloor \& B_{cd} = D \quad (2.13b)$$

while the non-canonic transfer function that requires $\max(B_{ncn}, B_{ncd})$ ADB's can be expressed as

$$\hat{H}(z) = \frac{A_0 + z^{-1} \cdot \sum_{j=0}^{B_{ncn}} \left(\sum_{i=0}^{2(L-1)-1} A_{i+j2(L-1)+1} z^{-i} \right) \cdot (z^{-2(L-1)})^j}{1 - z^{-1} \cdot \sum_{j=1}^D \left(B_{jL} z^{-(jL-2(L-1)(p_j-1)-1)} \right) \cdot (z^{-2(L-1)})^{(p_j-1)}} \quad (2.14a)$$

where

$$B_{ncn} = \left\lfloor \frac{N + D(L-1) - 1}{2(L-1)} \right\rfloor \quad \& \quad B_{ncd} = \left\lfloor \frac{DL}{2(L-1)} \right\rfloor \quad (2.14b)$$

and

$$p_j = \left\lfloor \frac{jL}{2(L-1)} \right\rfloor \quad (2.14c)$$

It is obvious that a non-canonic structure requires fewer, though relatively high-speed, amplifiers due to the reduced number of ADB's and single accumulator. On the contrary, the canonic structure needs more, though slower, opamps, like in the FIR counterparts. More importantly, no matter non-recursive or recursive ADB structures are, both evolve from the DF polyphase prototype [2.11, 2.12, 2.13], thus will all succeed in the inherent immunity to the input lower-rate S/H shaping distortion.

4.2 SC Circuit Architectures

To generalize with simplicity, only SC circuitry for a recursive-ADB structure will be presented for the IIR interpolating filter, since the non-recursive ADB realization for the FIR function can be easily obtained only by removing the feedback recursive networks. Then, to illustrate the above, a lowpass interpolator for a video decoder will be used as an example, which converts a 3.6 MHz bandwidth composite analog video signal, from sampling at 10 MHz to 30 MHz. For standard CCIR 601 8-bit accuracy requirement, a 4th-order Elliptic filter with < 0.4 dB passband ripple and ≥ 40 dB attenuation is necessary. Its original (2.10) and multirate modified (2.11) transfer functions coefficients are listed in Table 2-1.

The corresponding canonic-form using R-ADB polyphase structures in a Complete-DFII (C-DFII) realization is shown in Figure 2-5, and after formulating its multirate transfer function through (2.13a) and (2.13b) the corresponding SC circuit is obtained and presented in Figure 2-6.

Table 2-1. Transfer function coefficients of 3-Fold SC LP IIR video interpolators:original (a_i and b_i) and multirate-transformed (A_i and B_i) for Elliptic and ER C-DFII structures

Original			Multirate Modified		
(2.3)	Elliptic ($D=4$)	ER ($N=9, D=2$)	(2.4)	Elliptic ($D=4$)	ER ($N=9, D=2$)
a_0	0.0958	0.1006	A_0	0.0958	0.1006
a_1	0.0808	0.2146	A_1	0.2927	0.3181
a_2	0.1554	0.3616	A_2	0.5807	0.6198
a_3	0.0808	0.4385	A_3	0.8945	0.9613
a_4	0.0958	0.4084	A_4	1.1316	1.1926
a_5		0.2868	A_5	1.1983	1.2257
a_6		0.1355	A_6	1.0592	1.0613
a_7		0.0415	A_7	0.8073	0.7813
a_8		-0.0249	A_8	0.5250	0.4620
			A_9	0.2741	0.2199
			A_{10}	0.1140	0.0836
			A_{11}	0.0351	0.0020
			A_{12}	0.0065	-0.0117
b_1	2.2112	1.0285	B_3	-0.9688	-1.0256
b_2	-2.3148	-0.6850	B_6	-0.3683	-0.3214
b_3	1.1918		B_9	-0.0082	
b_4	-0.2695		B_{12}	-0.0175	

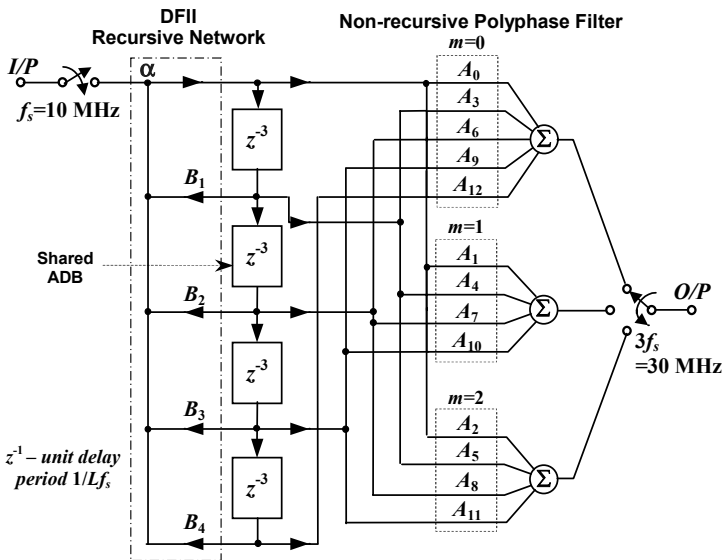


Figure 2-5. Canonic-form R-ADB/C-DFII polyphase structures for improved 3-fold SC IIR video interpolator

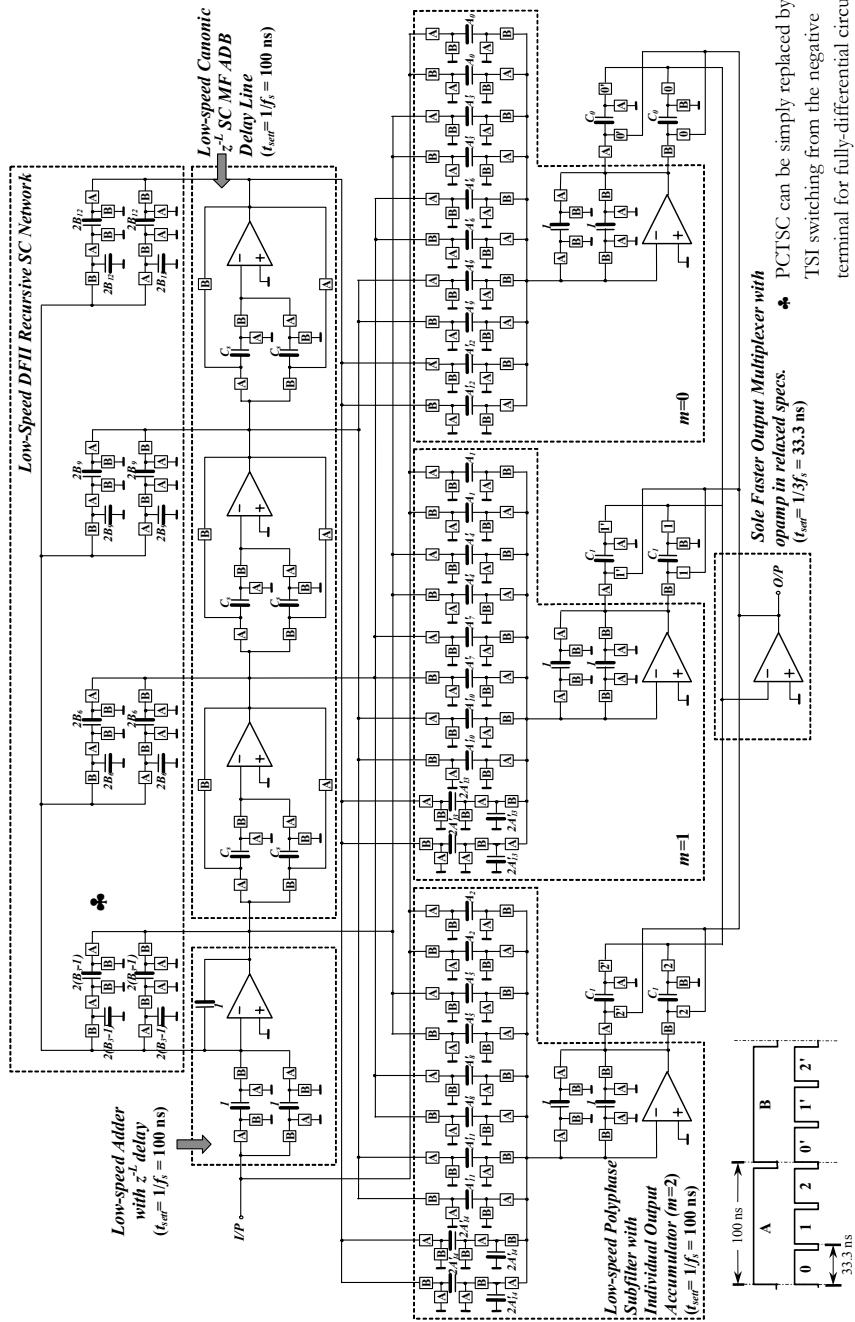


Figure 2-6. SC circuit schematic for canonic-form R-ADB/C-DFII polyphase structures

To further boost the speed capability of the filter, the double-sampling is efficiently employed due to the low-speed operation nature in canonic-form realization. The multirate denominator polynomials are obtained from the upper double-sampling DFII recursive feedback branches to the first specific adder stage that also implement simultaneously another functionality by embedding a z^{-3} delay. This adder/ADB together with the following SC ADB circuits form a low-speed serial delay line shared by both recursive and non-recursive networks. Especially, these L -unit ADB SC circuits exhibit a Mismatch-Free (MF) property for better reduction of the errors that will be accumulated along the delay line due to the finite gain and bandwidth, as well as the offset of the opamp when compared to the general charge-transferred delay circuit.

Considering one of the most efficient advantages of polyphase structures, namely the relaxed operation speed at the lower input sampling rate, the bottom half of the circuit contains $L=3$ low-speed DF polyphase filters by employing their corresponding individual slow accumulators, each being responsible for generating one of L output samples at lower input sampling rate. Thus, all the opamps in ADB's and accumulators have a very relaxed settling time requirement of full large input sampling period (100 ns), which is $L=3$ times longer than that of opamps, if a conventional bi-phase filter with double sampling was used. This also contributes to the reduction of the noise, charge injection and clock feedthrough errors in SC circuits.

The transfer function coefficients are implemented by either Toggle-Switched Inverter (TSI) and Parasitic-Compensated Toggle-Switched Capacitor (PCTSC) for positive and negative value respectively (PCTSC will be replaced by TSI switching from the negative terminal for fully-differential implementations which will be the dominant structure for state-of-the-art SC ICs). In addition, the recursive networks contribute not only to the common delay line but also to the non-recursive SC branches A_0 , A_1 and A_2 for each polyphase subfilter at the same time, since input and recursive signals must originally be added together at node " α ", as illustrated in Figure 2-5. In order to save this adder (one extra opamp) and to take advantage of both the existing output accumulator and of the opamp in the ADB, a coefficient-simplification procedure is proposed to each polyphase subfilter based on two sets of the same recursive networks – one that feeds back to the input of adder/ADB, and another that feeds forward to the output accumulator which can be efficiently combined together with existing non-recursive branches. In other words, no extra SC branches are needed, e.g., A_3 and A_6 in polyphase subfilter $m=0$ are simplified to $A'_3 = B_3 \times A_0 + A_3$ and $A'_6 = B_6 \times A_0 + A_6$ respectively, while A_4 in polyphase subfilter $m=1$ to $A'_4 = B_3 \times A_1 + A_4$.

$L=3$ parallel double-sampling Toggle-Switched Capacitor (TSC) branches followed by an output unity-gain buffer can be simply used as a multiplexer (MUX) for switching the interpolated output from those three polyphase subfilters. Besides, there is another simple MF SC multiplexer which can employ the well-known fully-differential and bottom-plate sampling techniques to eliminate the signal-dependent charge-injection and clock feedthrough errors that are unavoidably existed in the aforementioned unity-gain buffer approach. Although it operates at higher output sampling rate (33.3 ns settling time – full output period), its feasibility is derived from the fact that specifications of the multiplexer opamp are much less stringent than those in ADB's or accumulators if operating at the same speed. This happens because the opamp always operates with a large feedback factor (> 0.5 when the sampling capacitor is greater than the input parasitics capacitance of opamp), thus reducing its bandwidth or transconductance requirements. Normally, the relatively smaller total equivalent capacitive loading compared with those formed by a set of coefficient capacitors (for opamps in ADB's) with also a large summing feedback capacitor (for opamps in accumulators), together with usually smaller output voltage step during two consecutive phases (due to the sampling rate increase nature), normally relax the opamp slew-rate and bandwidth requirements which are all directly proportional to the opamp power consumption. If it is necessary to drive a large capacitive load (like a pad of IC for testing purpose), then buffers with low output-impedance are normally required for better performance, because for higher power efficiency, opamp used in SC circuits are normally designed with high output impedance (also called transconductance opamp or Operational Transconductance Amplifier-OTA). Thus, especially in baseband lowpass systems, the power of this multiplexer opamp can be even smaller than those with wide settling time in ADB's (presented next). Moreover, the errors caused by finite-gain and offset of this MF multiplexer will introduce smaller deviation and mostly just a gain shift and a DC offset in the overall system response. Then, its elimination of charge-transfer reduces not only the mismatch error for each path but also the special glitches in the output signal caused by the opamp high output-impedance that normally appears in the beginning of the charge-transfer in transconductance-opamp-based SC circuits. Consequently, the canonic ADB structure is very attractive for high frequency operation.

By formulating the multirate-transformed transfer function of this 3-fold Elliptic interpolating filter from (2.14a), (2.14b) and (2.14c), the circuit can be also designed with non-canonic R-ADB polyphase structures in a C-DFII architecture, where the simplified structure and its corresponding SC circuit diagram are presented in Figure 2-7 and Figure 2-8, respectively.

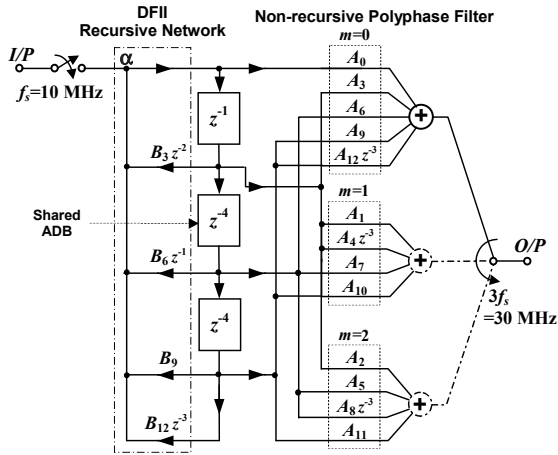


Figure 2-7. Non-canonic-form R-ADB/C-DFII polyphase structures for improved 3-fold SC IIR video interpolator

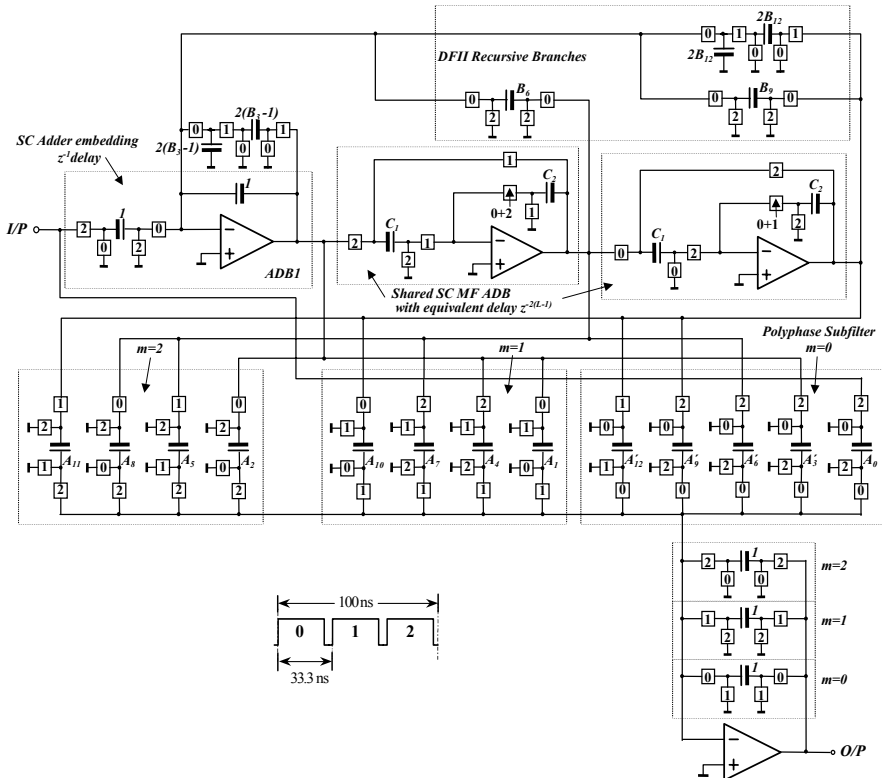


Figure 2-8. SC circuit schematic for non-canonic-form R-ADB/C-DFII polyphase structures

It is obvious that it needs less opamps with the use of $2(L-1)=4$ unit delay instead of $L-1=2$ for each ADB in canonic-form realization, and the extra 2-unit delay is elegantly implemented by holding charge in capacitors C_1 and C_2 in different turns. Especially, there is no charge transferring during the delay process for this novel SC ADB circuit, so it will eliminate the capacitor ratio mismatches and enhance the achievable speed. Here, only the unity-delay is embedded in the adder/ADB to simplify the coefficient-simplification procedure (only A_6 , A_9 & A_{12} for polyphase subfilter $m=0$) while without increasing the required number of ADB's. Moreover, only one time-shared SC output accumulator with 3 multiplexed summing branches for 3 polyphase subfilters is employed to produce L interpolated outputs. Although the higher-speed opamps are required here, they operate with the required settling time of full output sampling period (33.3 ns) which is still wider than what has been reported [2.5, 2.6, 2.7, 2.8, 2.9, 2.10]. The total number of opamps will be saved to 4 only and the sensitivity performance will also be improved when compared to those of the canonic realization, thus it is more suitable for lower speed applications.

The simulated overall and passband amplitude responses are presented in Figure 2-9. The passband satisfies the requirement (< 0.4 dB) although there is 0.2 dB rolloff caused by output sampling rate 30 MHz which is much better than nearly 2 dB rolloff suffered from the input S/H distortion in conventional non-optimum-class of SC interpolating filters.

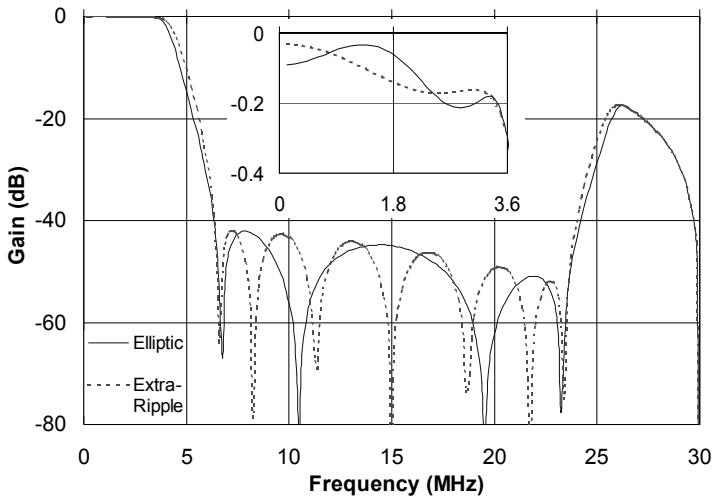


Figure 2-9. Simulated amplitude response for improved 3-fold SC IIR video interpolator with Elliptic and ER transfer function

5. LOW-SENSITIVITY MULTIRATE IIR STRUCTURES

5.1 Mixed Cascade/Parallel Form

Although high-order IIR interpolators can be implemented directly in a single stage by employing the above R-ADB/C-DFII polyphase structures, cascade or parallel form structures are usually preferable for their lower sensitivity to coefficient deviation. Therefore, for interpolation with relatively smaller or prime L factors but higher IIR filter order, Parallel Form (P-DFII) structures can be simply achieved by expressing the rational transfer function in a partial fraction expansion and implementing it by the 1st- and 2nd-order building blocks in parallel. Thus, the corresponding modified multirate transfer function can be expressed as

$$\hat{H}(z) = \sum_{i=1}^S \frac{\hat{N}_{p-i}(z)}{\hat{D}_i(z)} \quad (2.15)$$

where S is the number of the stages and each stage can be realized by the above DFII R-ADB polyphase structures.

Nevertheless, the cascade form has normally better sensitivity performance than parallel form due to the independence of the errors in each section caused by their poles and zeros deviation, while the sensitivity performance of parallel form highly depends on the output adder. However, the pure cascade form is actually a multistage implementation of interpolation, that is only suitable for large or nonprime alteration factor L due to its inherent nonidentity of input and output sampling rate. Therefore, here another alternative is proposed: Mixed Cascade/Parallel (MCP-DFII) structure, which is a combination of a cascade of low-order recursive DFII parts and a multi-feed-out parallel non-recursive polyphase subfilter structure (designated as internally-cascaded [2.22]) and is especially suitable for sampling rate conversion. Since the cascade of recursive parts leads to a considerably large reduction in the dependency between coefficient sensitivity and output adder, it improves significantly the overall circuit sensitivity performance. In this case, the modified transfer function can be mathematically decomposed into the following form

$$\hat{H}(z) = \sum_{i=1}^S \left(T_i(z) \cdot \frac{\hat{N}_{MCP_i}(z)}{\prod_{j=1}^i \hat{D}_j(z)} \right) \quad (2.16)$$

where the $T_i(z)$ is the accumulated delay factor introduced by the cascade of recursive parts and $T_1(z)=1$. An optimized choice of this delay factor will render a better performance, and the idea is actually to lower the quality factor of each cascaded stage.

This structure can be further explained by considering the application to the same 3-fold 4th-order video interpolator. The coefficients of the modified multirate transfer function for P-DFII and MCP-DFII ($T_i(z)=z^{-6}$) realizations are all tabulated in Table 2-2 and their corresponding R-ADB polyphase structures are shown in Figure 2-10(a) and (b) for P-DFII and MCP-DFII, respectively. As will be illustrated later, MCP-DFII structure offers a much better performance than C-DFII and P-DFII especially for high order functions. Hence, we only present in Figure 2-11 the SC implementation of MCP-DFII structure in non-canonic form for simplicity and comparison with the previous circuits, although canonic-form is also equivalently applicable, as well as the P-DFII can also be derived similarly. The output accumulators of the polyphase filters in these two 2nd-order sections are efficiently shared for reduced number of opamps. Furthermore, both P-DFII and MCP-DFII always offer an extra superiority in reducing the capacitor spread, e.g. Maximum coefficient spread for C-DFII, P-DFII and MCP-DFII are 209, 67 and 58, respectively, in this example. The simulated results are the same as C-DFII as shown in Figure 2-9.

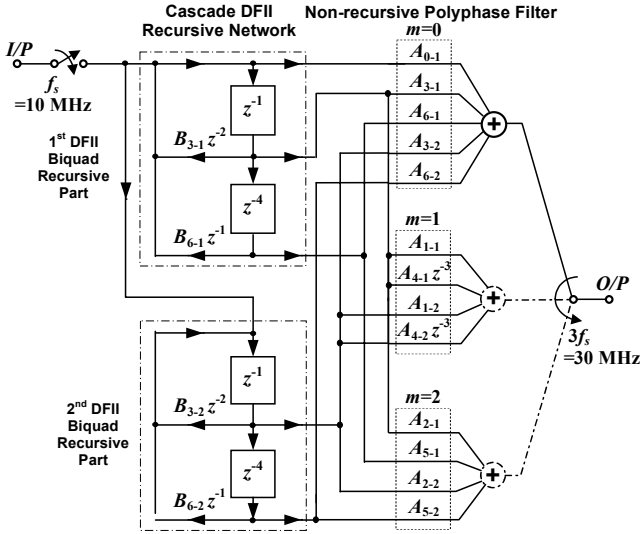


Figure 2-10(a). R-ADB/P-DFFI for Improved 3-fold SC IIR video interpolator

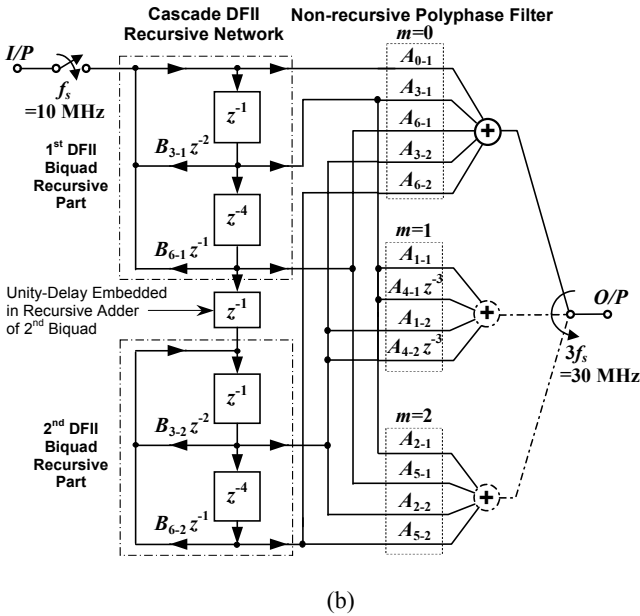


Figure 2-10(b). R-ADB/MCP-DFFI for Improved 3-fold SC IIR video interpolator

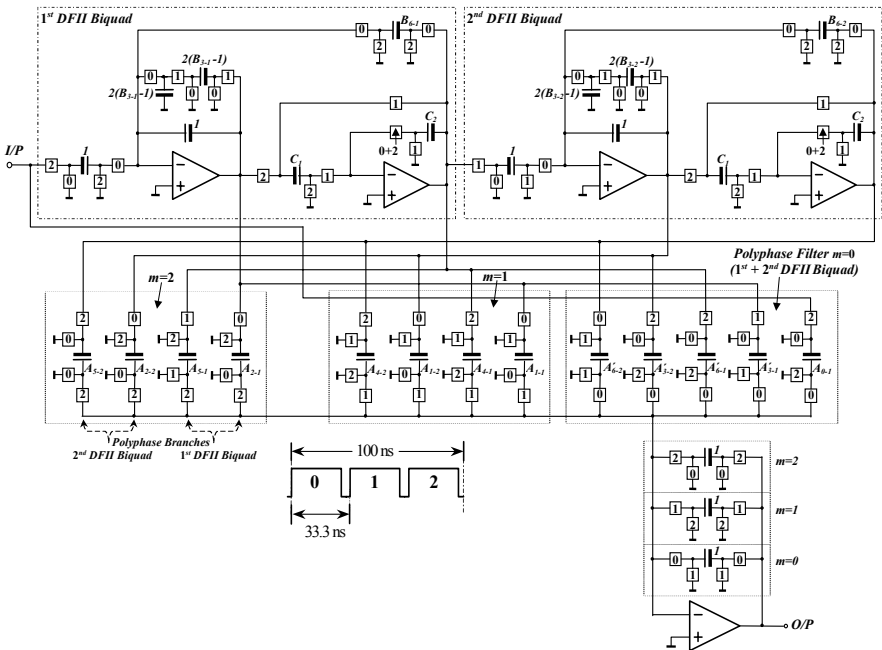


Figure 2-11. SC circuit schematic for non-canonic-form R-ADB/MCP-DFII polyphase structures

Table 2-2. Multirate-transformed coefficients of transfer function of 3-Fold SC LP IIR video Elliptic (D=4) interpolators in P-DFII and MCP-DFII structures

Elliptic	P-DFII		MCP-DFII	
	Biquad 1	Biquad 2	Biquad 1	Biquad 2
A_0	0.0958	0	0.0958	0
A_1	-0.8309	1.1236	0.2927	0.8948
A_2	-0.4863	1.0670	0.5807	0.6083
A_3	0.1621	0.7406	0.9027	0.3340
A_4	-0.4429	0.3175	1.1568	0.0656
A_5	-0.0593	0.0900	1.2484	-0.0172
A_6	0.3027	-0.0149	1.1330	-0.0410
B_3	-1.0550	0.0862	-1.0550	0.0862
B_6	-0.4174	-0.0419	-0.4174	-0.0419

5.2 Extra-Ripple IIR Form

Another alternative technique for IIR interpolation uses the Extra-Ripple (ER) type IIR transfer function obtained by the improved Martinez/Parks algorithm [2.23] for achieving better sensitivity in passband due to its advantage of smaller denominator order, by optimum positioning of the poles and zeros [2.23, 2.24]. For the same specifications of the above video interpolator, the original ER IIR transfer function is obtained with only lower 2nd-order denominator but at the price of a higher 8th-order numerator ($N=9$, $D=2$). However, its multirate-transformed transfer function, with coefficients shown in Table 2-1 together with the original, has a denominator order of 6, but, more importantly, exactly the same order of 12 in the numerator when compared with that of the 4th-order IIR Elliptic, as shown also in Table 2-1. This means that no penalty is present for increasing the number of zeros and that shows its additional superiority for the use in multirate circuits. It has an identical implementation in R-ADB/C-DFII structure with either canonic or non-canonic form, as in Figure 2-6 and Figure 2-8, but with 2 less recursive branches. If higher denominator order is required, both P-DFII and MCP-DFII realizations can also be preferably employed. The simulated results for their corresponding SC circuits in both canonic and non-canonic forms are the same and illustrated in the dashed curve of Figure 2-9.

6. SUMMARY

This chapter presents first the rigorous mathematical analysis on conventional sampled-data analog interpolation whose response is distorted by undesired input lower-rate S/H shaping effect. A new ideal improved analog interpolation model has then been presented to entirely eliminate such distortion over the whole frequency axis. Both traditional Bi-phase SC structures and multirate polyphase structures have been described in order to achieve such improved analog interpolation. Especially, the multirate polyphase structure has been proven to be an efficient and effective realization for optimum-class analog interpolation with respect to the competent power and silicon consumption. Different ADB polyphase-based structures with their corresponding SC architectures have then been investigated thoroughly for practical higher-order filtering functions: FIR non-recursive ADB and IIR recursive ADB in their canonic and non-canonic realizations with L low-speed accumulator and single time-shared accumulator schemes, respectively. Detailed practical IC design

considerations and different structures' pros and cons will be further studied and analyzed next.

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