

Chapter 2

HISTORICAL REVIEW AND STATE-OF-THE ART

Abstract: In this chapter, we provide a non exhaustive review of the research work conducted in the field of integrated circuit electromagnetic compatibility. A wealth of research results has appeared in the last couple of years, and this review aims at describing how new techniques, tools and methods have emerged. Roadmaps for integrated circuits and package, as well as EMC issues are also given in this chapter.

Key words: History; parasitic emission; susceptibility; modeling; standards; technology; packaging; issues

1. THE EARLY WORKS

In 1965, Gordon Moore co-founder of Intel Corporation published a long-term vision of the evolution of integrated circuits.

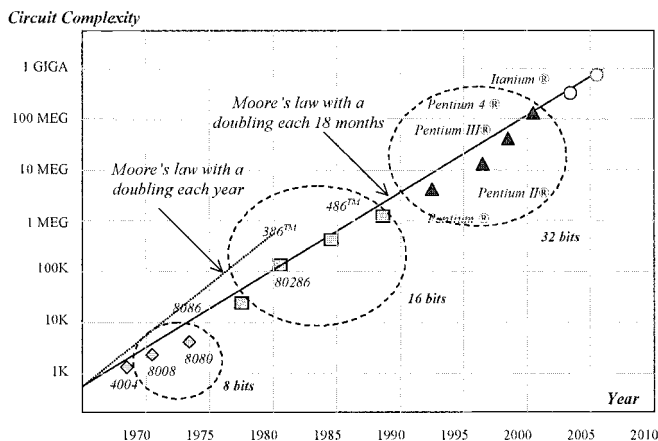


Figure 2-1. Moore's law compared to Intel processor complexity from 1970 to 2005.

SCEPTRE: A Program for Automatic Network Analysis*

Abstract: This paper describes the mathematical formulation of a computer program for automatic transient analysis of electronic networks. The formulation is based on the "state-variable" approach to network analysis and differs from other such programs primarily in the way that the network equations are manipulated to produce a solution. SCEPTRE includes a number of features aimed at providing greater flexibility and convenience for users of the program. Important among these features is that no prescribed equivalent circuit for active elements is required for program operation. Also, linearly dependent voltage and current sources in a network can be handled by the program, and provision has been made to allow a free-form format for input data. The paper includes a discussion of the program's ability to solve networks containing time-varying passive elements, and considers the factors that influence program running time.

* Work supported by the Air Force Weapons Laboratory under contract AF 29(601) 6852. Dissemination of the SCEPTRE program is controlled by the Air Force Weapons Laboratory, Attn: WLRRT (Capt. Gary Pritchard), Kirtland Air Force Base, New Mexico 87117.

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Figure 2-2. The software SPECTRE was originally designed for radiation simulation on electronic devices.

Recognizing a trend in integrated circuit complexity, he extrapolated the tendency and predicted an exponential growth in the available memory and calculation speed of microprocessors which, he said, would double every year (Moore, 1965). With a slight correction (i.e. doubling every 18 months, see Fig. 2-1), *Moore's Law* still holds today.

The American army was a pioneer in the field of integrated circuit EMC. As early as 1965 at the Special Weapons Center, based at Kirtland, New Mexico, they studied the effects of the electromagnetic fields triggered by nuclear explosions on electronic devices used in missile launch sites. As a result of this effort, the simulation software SPECTRE (Sedore, 1967a), was developed at IBM (Fig. 2-2) for simulating the effects of nuclear radiation on electronic components (Sedore, 1967b). With this software, it was possible to correlate simulations and experimental measurements obtained on an electromagnetic impulse test-bench.

At electronic equipment level, protection techniques were developed to face the couplings with radio and television emitters, radars and nuclear electromagnetic pulses. Several military norms were published in the United States on this subject, on one hand the BE Mil-STD (Military standard) 461, which concerned the interference levels that the equipments must hold (Mil-std, 1967), and on the other, the Mil-STD 462 that specified the measurement methods for electromagnetic interference characterization. One of the earliest academic publications on the simulation of integrated circuit concerned the 741 integrated operational amplifier, and was published by Wooley (1971). The author succeeded in simulating the different stages of this integrated circuit with the simulation software *CANCER*, from Berkeley University (An ancestor of the well-known analog circuit simulator SPICE).

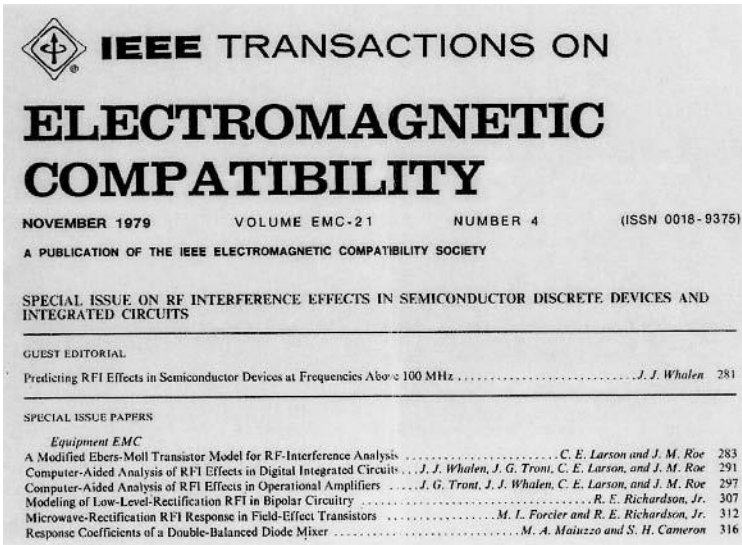


Figure 2-3. A special issue on radio-frequency interferences in integrated circuits.

As an Associate Professor at the State University of New York in Buffalo, NY USA, James J. Whalen, was another pioneer in the field of integrated circuit EMC. In 1975, he published studies on the radio-frequency pulse susceptibility of discrete transistors (Whalen, 1975). The *IEEE Transactions on Electromagnetic Compatibility* (Fig. 2-3) invited Prof. Whalen to release a special issue that put together a set of papers focused on the effect of radio frequency interferences on integrated circuits (Whalen, 1979). In his editorial, Whalen justified the interest of that special issue by the rising risk of interference between electromagnetic sources in the Very High Frequency band (VHF 30 MHz-300 MHz), Ultra High Frequency band (UHF 300 MHz-3 GHz) and even Extremely High Frequencies with radars (XHF 3 GHz-30 GHz).

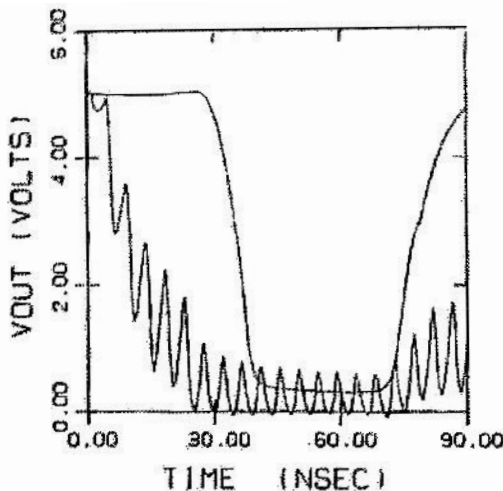
The special issue dealt specifically with the effects of the interference on semiconductor devices and the prediction of these behaviors by means of dedicated simulation tools. The need to modify available device models to account for the unusual conditions of radio-frequency interference was expressed by C. E. Larson (1979), who proposed a modification of the bipolar transistor model.

One year later, Chen and Whalen (1980) proposed a macro-model approach to speed up simulations, an idea that would be utilized by many other engineers and scientists in order to keep the simulation time reasonable while handling ever more complex integrated circuits.

The first ideas on carrying out conducted RF immunity measurements in a compact manner were defined by Bersier (1981) from Swiss Telecom in the beginning of the 80s. Then a method for testing the RF immunity of audio and video products was developed which would not require large semi anechoic rooms and high power RF sources. It was found that the relation between induced common-mode currents and the externally-generated EM-fields on the cables was about 1–5 mA/V/m. Furthermore, it was found that the common-mode impedance as seen by an apparatus in common-mode was around 150 Ω , which is close to the common-mode value as found by other authors.

The first susceptibility analysis of MOS components was published in 1980 and involved memory circuits. J.N. Roach (1981) characterized the sensitivity of 1Kbyte NMOS memories. Some years later, a study was published by (Tront, 1985) concerning the behavior of the 8085 processor in the presence of 100 and 220 MHz radio-frequency interference. Using the simulation software SPICE, he reproduced some of the phenomena observed during measurements (Fig. 2-4).

Watchdog circuits were added to microprocessors (Lu, 1982) for structural integrity checking. Watchdog circuits were found to be of great importance for processor recovery and safe reset after undergoing electromagnetic interference.



V_{OUT} versus time for $V_M = 20$ V and $f = 220$ MHz. A plot of the unperturbed V_{OUT} is superimposed on the curve.

Figure 2-4. Unperturbed and perturbed signals simulated by (Tront, 1985).

2. RESEARCH IN EMC FOR ICS BETWEEN 1990 AND 1995

Bakoglu (1990) compiled a remarkable synopsis of the parasitic effects in integrated circuits, packaging and printed circuit boards. He described different problems linked to transient current consumption at active edges of the clock and detailed the basic mechanisms for integrated circuit resonance. Package models were provided for Dual-In-Line (DIL), Quad-flat-pack (QFP) and Pin-Grid-Array (PGA) families.

Also in 1990, Kenneally presented measurement results for simple integrated circuits in CMOS and TTL technologies. He noticed that the sensitivity decreased as the radio-frequency interference increased, from 1 to 200 MHz.

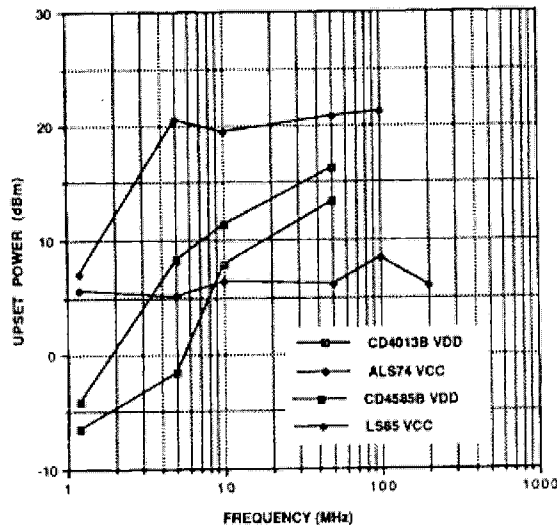


Figure 2-5. Susceptibility thresholds vary depending on the technology.

Significant differences were exhibited depending on the fabrication technology. In all cases, CMOS circuits tended to be less robust than TTL circuits (Fig. 2-5). As a Ph.D. student at the University of Toronto, Laurin (1991) published a study of the effects of radio frequency perturbations on the oscillator circuits used in a Motorola 6809 processor. When placing an electric current loop close to the oscillator, he observed clock jitter, function losses in the microprocessor and data losses on the serial data bus (Fig. 2-6).

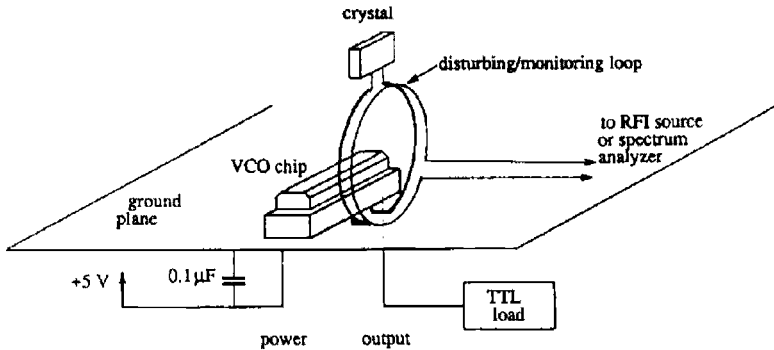


Figure 2-6. Perturbation of an oscillator using a magnetic probe (Laurin, 1991).

Also in relation with microprocessors, Tang (1993) from the University of Singapore showed that electromagnetic interference could cause non-fatal failures that resulted in counting inaccuracy in microprocessors. He performed conducted and radiated susceptibility measurements, and could demonstrate a specific byte-swap problem on the most significant byte of a counter, leading to severe counting errors. Solutions based on software modification and PCB layout improvement was proposed. The author pointed out that low-speed systems were vulnerable to EMI as much as high-speed systems.

Many EMC books published in the early 90s mainly focused on printed-circuit-board EMC. Most of these books only gave a little insight in specific problems of integrated circuits. In chapter 3 of his book *"Principles and applications of EMC"*, Weston (1991) compared the switching characteristics of various families of integrated circuits, as well as their impacts on radiated and conducted emission (Weston, 1991).

A study was published by Graffi (1991) about the behavior of 741 operational amplifiers when a 200 KHz - 50 MHz interference signal was superimposed on normal signals. He obtained good correlation between experimental measurements and simulations using simplified macro-model, which accelerated the computation by a factor of up to 50.

Time-Domain Reflectometry (TDR) was used by (Hauwermeiren, 1992) for the characterization of package behavior at very high frequencies. A simple model based on discrete R, L, C components was proposed for Leadless Chip Carriers (LCC) and Pin Grid Arrays (PGA). His approach was very close to the one later proposed by the IBIS group for the modeling of packaging.

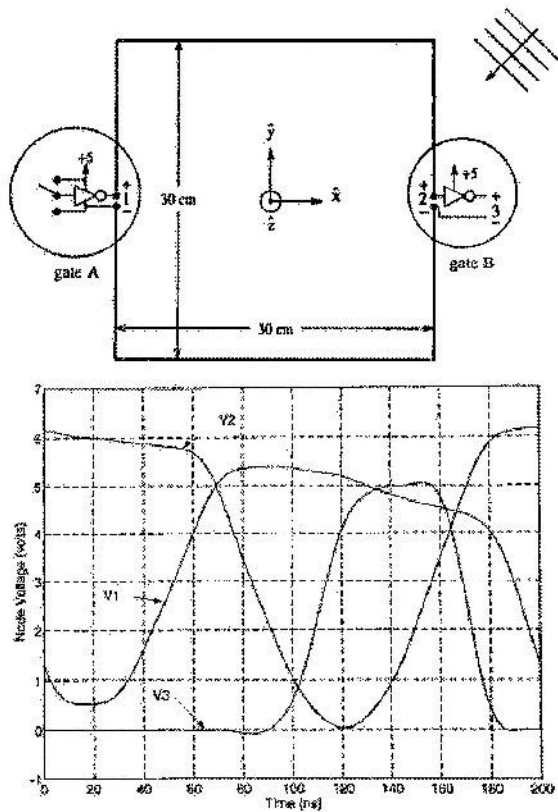


Figure 2-7. Parasitic commutation of an inverter circuit output (V3) connected to a long wire (Near end V1, far end V2) acting as a receiving antenna for a field of 2 V/m.

Synchronous switching noise is one of the most significant chip-level concerns for EMC and signal integrity engineers. One of the earliest publications on this topic was a paper by (Downing, 1993) on the characterization of decoupling capacitance effects including on-chip decoupling and decoupling close to the integrated circuit.

3. SUSCEPTIBILITY OF INTEGRATED CIRCUITS (STARTING 1995)

The effects of an electromagnetic wave coupling to PCB traces and the consequences of this coupling on simple circuits were analyzed by Laurin (1995). With field strengths as high as 200 V/m, no disturbance was observed on the component.

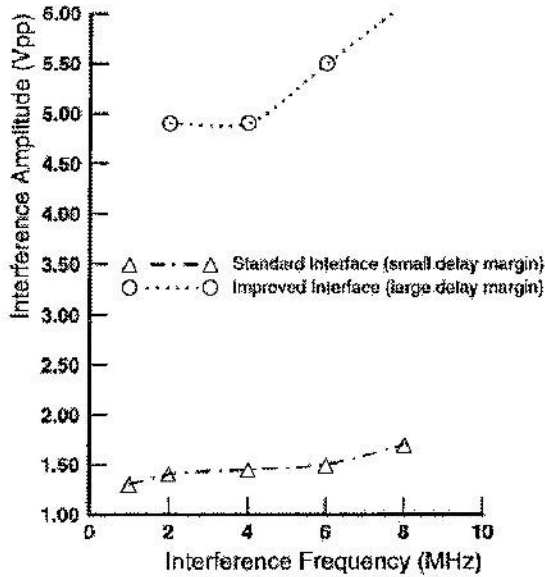


Figure 2-8. Two circuits with same functionality but very different immunity levels.

Adding a long metal wire that was half-a-wavelength long to the interference frequency allowed fields as low as 2 V/m to cause severe malfunctions due to erroneous switching (Fig. 2-7). The authors differentiated between a *static regime* and *transient regime*. In the static regime, only perturbations with high energy affected logic levels. In the transient regime, even weak perturbations could affect switching delays and circuit thresholds.

Chappel (1997) discussed the possibility of *hardening* integrated circuits to electromagnetic interference by specific design techniques that raised the immunity level of ICs from a low 1.5 V to more than 5 V, in the frequency range 1 to 10 MHz (Fig. 2-8). Several other circuits have also been proposed that exhibit a high immunity to RFI including Schmidt triggers, low-voltage differential swing circuits and delay-insensitive structures.

Hattori (1998) demonstrated the advantages of frequency-domain simulations as opposed to time-domain analysis. This approach proved to be very efficient to obtain the behavioral response of analogical circuits quickly, and more particularly the offset variations versus frequency.

While the demand for mobile communications was exploding, the behavior of integrated circuits in the presence of GHz-range interference was not extensively studied.

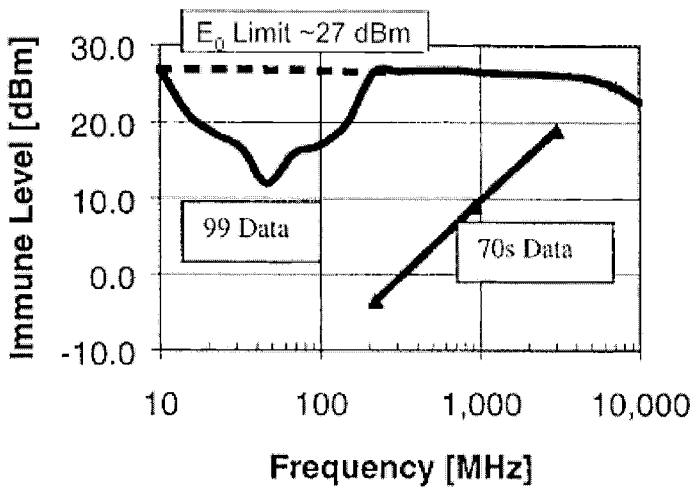


Figure 2-9. : Immunity of the NAND 74LS00.

In 2000, an updated version of the *Integrated Circuit Electromagnetic Immunity Handbook* published by NASA gave valuable information on the immunity levels of simple integrated circuits up to 10 GHz (Sketoe, 2000). Chapter 4 presented measurement results concerning simple components, with a very interesting comparison with similar measurements performed in the early 80s. The frequency range was 10 MHz to 10 GHz. From the results shown in Fig. 2-9, the immunity level of recent components has proven to be higher than 70s versions, that could be explained by input/output protection improvements.

Through experience gained on a variety of microprocessors and micro controllers, some engineers started developing strategies for hardening microprocessor-based systems. Coulson (1997) identified the vulnerable points, proposed specific circuits such as supply supervisors or watch-dogs, but also some software-based techniques such as memory integrity checking, token passing, and redundancy coding. Campbell (1998) claimed that by simple *defensive software* programming, a micro controller immunity performance could be increased up to one order of magnitude at a low implementation cost.

Less optimistic, Ong (2001) studied the effect of software-based techniques on the reliability of embedded applications in the presence of EMI. The “defensive software” approach based on function tokens was found to be inefficient and not generally applicable. In contrast, the implementation of NOP fills in unused memory proved to have a positive impact on system reliability.

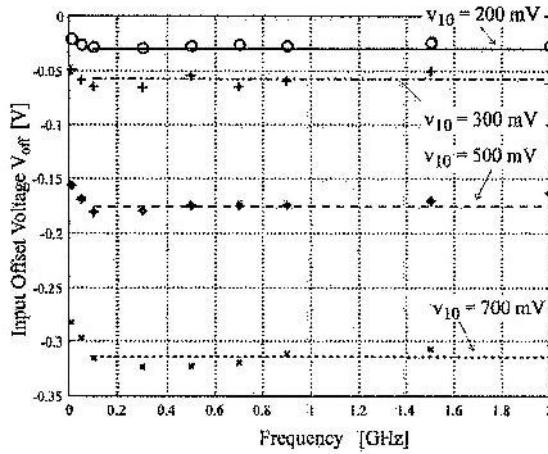


Figure 2-10. Response of an operational amplifier to 100 MHz-2 GHz RFI using microwave probing directly on the chip.

More recently, Fiori (2002) published a study of radio-interference effects on analog amplifiers, up to 2 GHz. The measurement setup employed microwave probes directly positioned on the chip so as to maintain a 50- Ω impedance from the measurement equipment to the integrated circuit (Fig. 2-10). He observed increased DC shifts of the amplifier offset with the RFI amplitude which surprisingly remained almost constant from 100 MHz to 2 GHz.

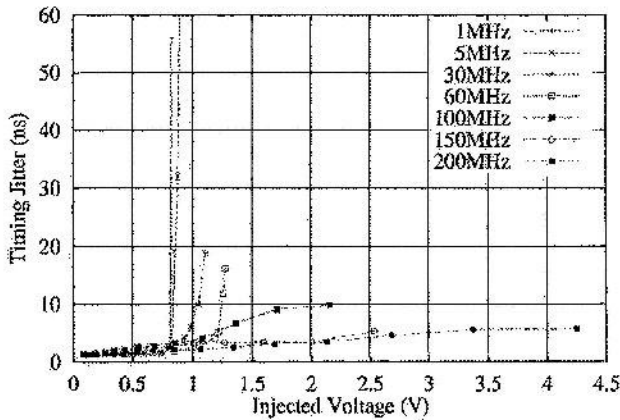


Figure 2-11. Modification of switching delays as a function of amplitude and interference frequency.

Robinson (2003) modeled the variation of signal propagation delays in integrated circuits due to electromagnetic aggressions. Although the experiments were only conducted up to 200 MHz (Fig. 2-11), the component sensitivity to interference tended to decrease with frequency, at frequencies well above the designed operating frequency of the device under test.

4. PARASITIC EMISSION OF INTEGRATED CIRCUITS

Goodman (1995) published results of a comparison between measurements and simulations of signal propagation in Pin-Grid Arrays (PGAs). He showed varying deleterious effects of signal transmission depending on the package pins, explored ground signal delays, and used simple R,L,C elements as proposed in (Hauwermeiren, 1992), but for significantly higher frequencies.

While using discrete R,L,C components to model package leads, bonding and integrated input/output structures, he used transmission lines for the printed circuit board tracks to validate the model up to 4 GHz.

Constant increases in integrated circuit complexity require packages with higher pin density and broader bandwidth. (McCredie, 1996) successfully modeled the switching noise of an ASIC mounted on a compact BGA with around 1000 I/O pins using distributed current sources, on-chip and on-package decoupling capacitance models as well as serial connection inductances (Fig. 2-12).

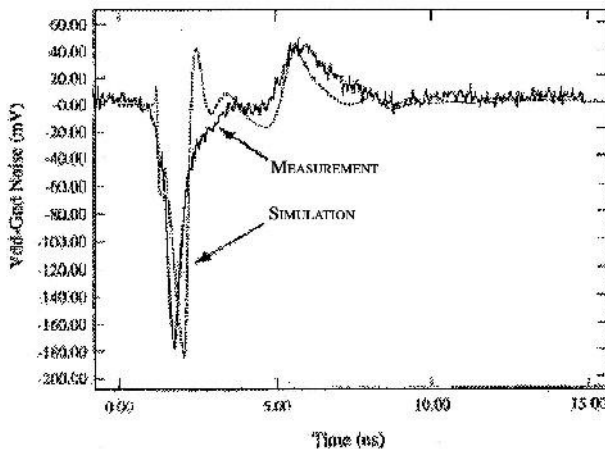


Figure 2-12. Switching noise measurement and modeling on high complexity pin grid array.

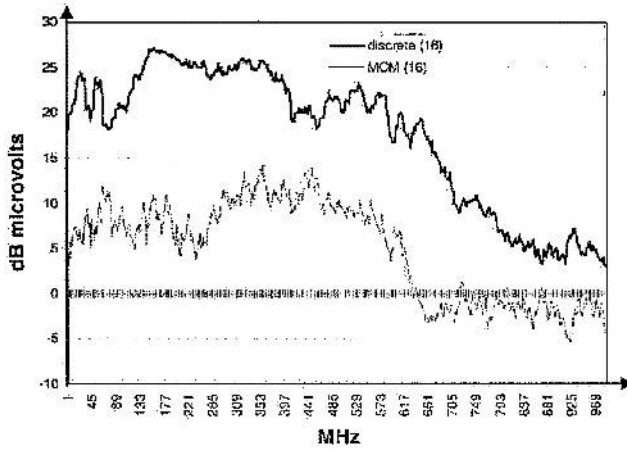


Figure 2-13. Package influence on the radiated emission in TEM cell (dB μ V vs. frequency, in MHz).

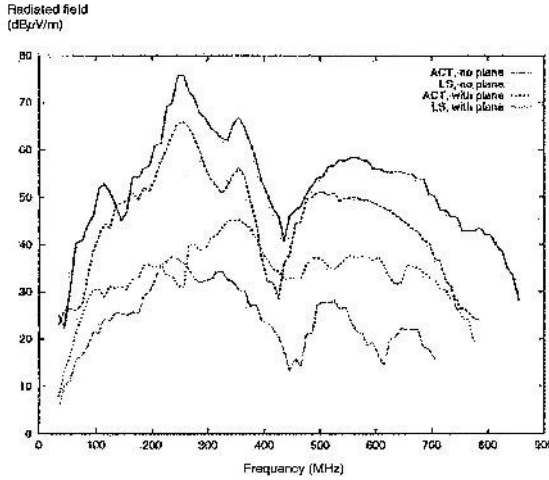


Figure 2-14. Far-field emission (50 MHz-900 MHz) measured at a 3-m distance, produced by simple ICs for varying technologies.

The same year, T. Williams published a practical book on design with EMC constraints with one chapter dedicated to integrated circuits (Williams, 1996). In the United States, the Society for Automotive Engineering (SAE) proposed a measurement method for radiated emissions of integrated circuits using a TEM cell.

Very interesting comparative studies were published by Slattery (1997) regarding 8 and 16 bit microcontrollers, that characterized the impact of technological variations, package and temperature on the spectrum (Fig. 2-13).

Robinson (1998) compared the radiated emissions produced by different families of logic circuits. An antenna was mounted 3 m away from the test board on an open-field test site. Results were provided for simple circuits such as inverters and NAND gates from various logic families: ACT (Advanced CMOS-TTL), FCT (Fast speed CMOS), HC (High speed CMOS), and HCT (High speed CMOS-TTL). Significant behavioral differences were observed, as illustrated in Fig. 2-14.

The author claimed that the peak amplitude E in the measured spectrum could be approximated by the formula

$$E = kAf_{\max}^{0.7} \quad (2-1)$$

where:

k =constant related to the integrated circuit design and technology

A =supply amplitude (V)

f_{\max} =operating frequency (Hz).

Jonghoon (1998) presented the TEM cell measurements of complex processors with and without local decoupling capacitors. This measurement technique is described in details in Chapter 4. The observed benefit of on-chip decoupling capacitors was significant (Fig. 2-15).

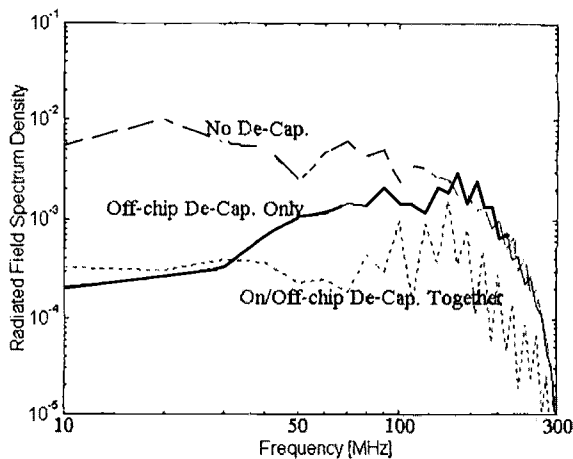


Figure 2-15. Impact of on-chip and off-chip decoupling capacitance on radiated emissions.

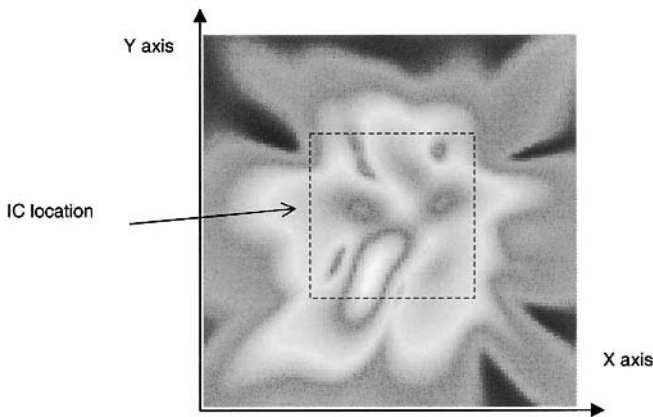


Figure 2-16. Near-field scanning.

Several works were published soon after (Steinecke, 2000; Van Wershoven, 2000) that confirmed that implementing large embedded capacitors, with values from 1 to 50 nF depending on the technologies and the size of the die, was a very efficient way of reducing emissions. Slattery also used the TEM cell (1999) to compare the emission characteristics of several microprocessors.

Van Wershoven (2000) also showed that active slew-rate control could further reduce radiated emissions. Another approach was suggested by Kim Soo-Hyung, who analyzed the impact of absorbent materials (Soo-Hyung 2000) such as ferrites mixed with epoxy, and observed a 3 to 20 dB reduction of the harmonics, especially beyond 300 MHz.

The near field scanner was adapted to the problem of the integrated circuits in 1995 by K. Slattery who was a consultant for Chrysler Corporation at the time. Slattery (1999) also designed and built one of the first near-field measurement scanners with a resolution high enough to map the fields above integrated circuit packages (Fig. 2-16). Many research labs involved in the study of chip-level EMC are now using near-field scanners based on the Slattery design.

Integrated circuit suppliers in Japan are world leaders in the production of low emission processors, in particular for automotive applications. Therefore, it is not surprising to find Japanese authors in scientific publications on the subject. For example, Hayashi (2000) described his approach to low-noise ASIC design, while Takahata (1999) proposed a circuit design model based on power-supply impedance, that provided the foundation for standard model proposals such as (IMIC, 2001).

4.1 Alternatives to Achieve Low Emission

Hardin and colleagues at Lexmark Corporation were probably the first to propose the idea of reducing peak emissions in the harmonics of the clock frequency by fluctuating the clock period in a controlled manner (Hardin, 1994). This idea is illustrated in Fig. 2-17.

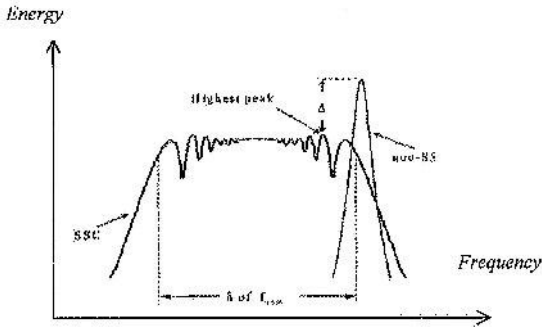
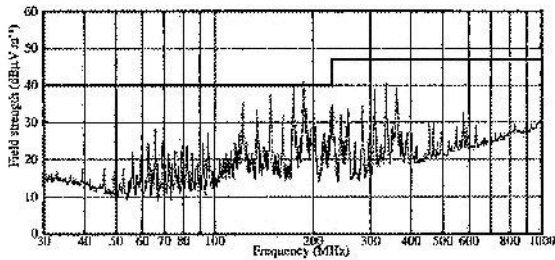


Figure 2-17. The spread-spectrum technique helps to reduce radiated emission.



(a)

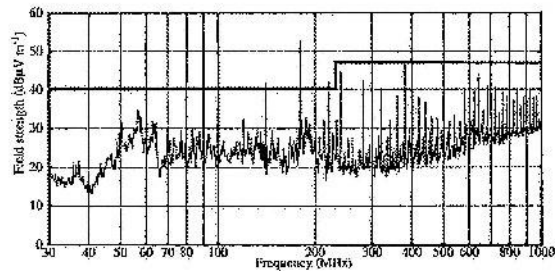


Figure 2-18. Parasitic emission of synchronous processor (a) compared to synchronous ARM60 processor (b).

The energy of a single harmonic concentrated in a very narrow bandwidth is redistributed over a larger frequency band. This noise reduction technique has also been applied to switching power supplies (Feng, 1994). Initially, it was viewed by some experts as a “way to cheat” the radiated emissions test procedures. However, (Slattery, 2001) published experimental results showing that this technique does actually reduce the risks of interference in electronic systems.

An interesting alternative for emission reduction may be found in asynchronous circuit design. Furber published results (1999) showing significant reduction of the peak harmonic (near 180 MHz) as well as high frequency harmonics in the asynchronous version of the ARM60 processor, as seen in Fig. 2-18. An important reference on asynchronous design techniques is the book of Sparso (2001).

5. STANDARDIZATION IN INTEGRATED CIRCUIT EMC

A set of important Electromagnetic Compatibility regulations were implemented in the European community in 1996, which probably revived the interest of the researchers and engineers for this subject, mainly in Europe. The European regulations set maximum limits for parasitic emission levels, as well as minimum immunity levels for most electronic devices.

At the component level, the most important standards were developed under the supervision of the international electro technical commission (IEC) which oversees important standardization activity through more than 100 technical committees. One of these committees, called *Technical Committee 47A*, had focused on integrated circuits as early as 1990. The role of this committee was to prepare international standards focusing specifically on logic circuits, memory, converters and hybrid modules. Another sub-committee called *Technical Committee 93*, was established a little later and focused on integrated circuit design automation.

5.1 Measurement Methods

Various measurement approaches for emission and immunity to electromagnetic waves were developed during the 90s in several countries, mainly in France, Germany, Italy, Holland, the USA and Japan. The establishment of these measurement methods was led by the automotive industry, which was facing frequent electromagnetic interference problems due to the increasing number of on-board electronic devices.

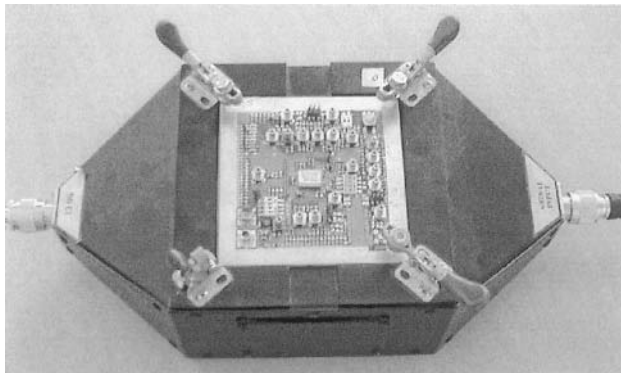


Figure 2-19. The TEM cell standardized in the USA (SAE, 1995).

One of the most common problems was interference in the FM band due to the switching noise of embedded micro-controllers.

The *Society of Automotive Engineers* (SAE) proposed a radiated measurement method using the TEM cell (Fig. 2-19) for the measurement of radiated emissions. A group from Holland proposed a conducted method based on the Workbench Faraday Cage (WBFC), and the German standardization group VDE proposed a conducted measurement method using a 1-ohm resistance in series with the component connection to ground. Researchers in Japan proposed a magnetic loop probing test and the SAE also proposed a near-field scanning technique.

In October 1997, the *Sub-Committee 47A* of the IEC decided to create a working group (WG9) to analyze the suggested measurement methods for integrated circuits. The group held several meetings from 1998 to 2000, notably in Seoul and Paris. After considerable discussion, it was decided to create a “tool box” of five methods for evaluating integrated circuit EMC: a TEM cell measurement, a surface scan technique, a $1\Omega/150\Omega$ method, measurement in a WBFC and the magnetic probe method. These measurement procedures are described in the document IEC 61967 “Integrated circuits – Measurement of electromagnetic emissions 150 KHz to 1 GHz” (IEC, 2001):

- Part 1: General conditions and definitions.
- Part 2: Measurement of radiated emissions – TEM-cell method.
- Part 3: Measurement of radiated emissions – Surface scan method.
- Part 4: Measurement of conducted emissions – $1\Omega/150\Omega$ direct coupling method.
- Part 5: Measurement of conducted emissions – Workbench Faraday cage method.
- Part 6: Measurement of conducted emissions – Magnetic probe method.

A comparative study of these measurement techniques was published by Lubineau (1999), as well as Fiori (2003) who conducted experimental measurements using these methods on identical devices. Both researchers provided valuable suggestions regarding the measurement setup and limitations. In the *Review of Radio Sciences* edited by Stone (2003), one chapter is dedicated to a synopsis of recent publications in EMC for ICs, with highlights on measurement techniques, modeling and reduction of parasitic emissions, as well as a review of research activities concerning the susceptibility of digital and analog components.

Standard measurement procedures for immunity have also been developed and are described in the five parts of the IEC document 62132 “Integrated circuits - Measurement of electromagnetic immunity » (IEC, 2002). The document is organized as follows:

- Part 1: General conditions and definitions.
- Part 2: Measurement of radiated immunity – TEM cell method.
- Part 3: Measurement of conducted immunity – Bulk current injection method (BCI).
- Part 4: Measurement of conducted immunity – Direct power injection method (DPI).
- Part 5: Measurement of conducted immunity – Workbench Faraday Cage method.

5.2 An EMC Model for Components

The first important contribution to the EMC modeling of components came from the IBIS (*I/O Buffer Information Specification*) group that proposed a standard description of the electric performance of the input/output structures of integrated circuits (Fig. 2-20).

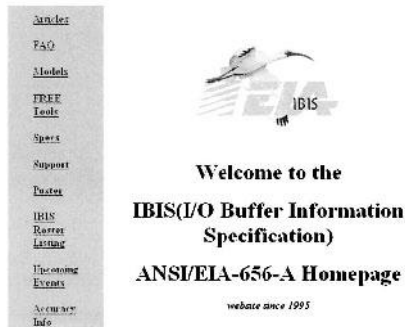



Figure 2-20. The IBIS home page.

The IBIS format was created by Intel Corporation in the early 90s, and was improved in successive versions. In 1993, a group called the IBIS Open Forum was created on the basis of voluntary contribution and association. In 1995, they became affiliated with the *Electronic Industries Alliance* (EIA).

The forum meets on a monthly basis using teleconferences, and works on updates of standards and on technical improvements by means of BIRDs (*Buffer Issue Resolution Documents*). Bob Ross, the coordinator of this forum for several years, has helped to coordinate rapid improvement and word-wide recognition of this format as a standard. The IBIS specification was ratified in 1995 in version 1.1 under the acronym ANSI/EIA-656.

The IBIS standard has been constantly updated since that time (IBIS, 2001), and version 4.1 was ratified in 2004. Details on the IBIS format are provided in chapter 5 of this book. From an electromagnetic compatibility point of view, IBIS provided information about the inputs and outputs of integrated circuits that was not previously available in data sheets. However, it did not provide any information about the core noise or high-frequency currents on the power supply pins.

In 1997, it was decided to create at IEC an EMC task force for which the assigned objective was to promote progress in the study of integrated circuits modeling and simulation. The *Working Group 6* (WG6) had to propose an EMC model for integrated circuit devices and to submit it to national committees for remarks and suggestions.



93/146/CDV

DRAFT TECHNICAL REPORT

Project number 62014-3/TR/Ed.1	
IEC/TC or SC TC 93	Secretariat U.S.A.
Distributed on 2001-11-30	Voting terminates on 2002-05-03
Also of interest to the following committees:	Supersedes document:
Functions concerned <input type="checkbox"/> Safety <input checked="" type="checkbox"/> EMC <input type="checkbox"/> Environment <input type="checkbox"/> Quality assurance	

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Titre: CEI 62014-3: CEM des composants -
 Partie 3: Modèle électrique des circuits intégrés (ICEM)

Titre: IEC 62014-3: EMC for Component – Part 3:
 Integrated circuits Electrical Model (ICEM)

Figure 2-21. The ICEM emission model proposal to IEC.

Table 2-1. The members of the IEC technical committee focused on EMC of integrated circuits in 2005.

Name	Affiliation	Representing
Gunter Auderer	Freescall, Munich	Germany
Ross Carlton	Freescall, Austin	USA
Mart Coenen	Philips Semiconductors	Netherlands
M. Joester	Siemens Automotive Regensburg	Germany
F. Klotz	Infineon,	Germany
J. Kolodziejski	University Warschau,	Poland
H. W. Luetjens	Philips Semiconductors	Germany
C. Marot	Siemens Vdo Toulouse	France
S. Mitani	Hitachi	Japan
A. Nakamura	Hitachi	Japan
C. Terrier	EM Microelectronic Marin SA	Swiss
O. Wada	Okayama university	Japan
T. Watanabe	NEC	Japan

In France, a research project was initiated by a group of academic and industrial partners in Toulouse from 1997 to 2000. The goals of this project were to establish the foundation for a standard model for predicting the emissions from components, and later to reuse this model for the prediction of immunity in the frequency band 1 MHz – 1 GHz. Starting with the characterization of simple components (Lubineau, 1999), a generic model applicable to complex integrated circuits such as ASIC and micro-controllers was proposed under the name ICEM (*Integrated Circuit Emission Model*) (Ben Dhia, 2002). The French UTE group worked on a standard proposal based on ICEM (Fig. 2-21) and applied the approach to commercial components (Lochot, 2003). At the end of 2002, the ICEM proposal appeared on the IEC web site, under the name *IEC 62014-3: Models of Integrated Circuits for EMI Behavioral Simulation*.

Another model proposal called IMIC (IMIC, 2001) was put forward by industrial and academic partners in Japan. At the end of 2003, the proposal *Interface Model for Integrated Circuits* (IMIC) appeared as IEC 62404 (IEC 2003).

5.3 Towards a Merge

At IEC level, the TC47A was designated to analyze the EMC standard model proposals ICEM, IMIC, as well as a new Japanese proposal called LECC with the objective of proposing a unified model that would use the best of each proposal.

The list of participants of this working group in 2005 is given in Table 2-1. The group also continued its work on measurement methods and expanded its activities to include the modeling of immunity. In 2005, more than 13 documents related to integrated circuit EMC were under consideration, which is a good indicator of the challenges and issues of this new field.

6. SPECIAL EVENTS AND PUBLICATIONS

The first workshop dedicated to integrated circuit EMC was held in January 1999 in Toulouse, and the second workshop in June 2000, also in Toulouse. The official language of both events was French. The 3rd workshop (*EMC Compo 02*) was held in English and attracted approximately 70 experts mainly from France, Germany, Italy and Belgium. In 2004, more than 100 experts from academic institutes and industries attended the 4th workshop (*EMC Compo 04*) held in Angers, France. The 2005 edition was organized in November at Munich, Germany (*EMC Compo 05*), and the 2007 edition should take place in the Netherlands.

A special issue of the Microelectronics Journal (Mejo, 2004) was devoted to the EMC of components, on the basis of a selection of papers from the workshop. The special issue included an overview of the standardization efforts, contributions related to emission prediction, test circuit emission characterization, asynchronous design, and analog circuit susceptibility analysis.

7. IC ROADMAPS

Tremendous advances in lithography over the past few years have made GHz clock rate microprocessors available for general use today. The key improvements have concerned the reduction of the device channel and the multiplication of interconnect layers, as shown in Fig. 2-22 where two portions of layout are reported in 0.8 μ m CMOS process available in 1990 (left) and 90nm (right) CMOS process, available in 2005.

Inside general-purpose electronic systems such as personal computers or cellular phones, we may find numerous integrated circuits (IC) set together with discrete components on a printed circuit board (PCB) as shown in Fig. 2-23. The integrated circuits have various sizes and complexity. The main core consists of a microprocessor, considered as the heart of the system, that includes several million transistors on a single chip.

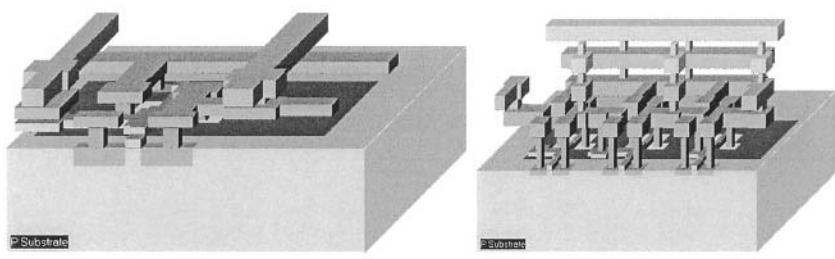


Figure 2-22. Evolution of the integrated circuit technology from 0.8μm 2-metal layer CMOS process down to 90nm 8-metal layer CMOS process.

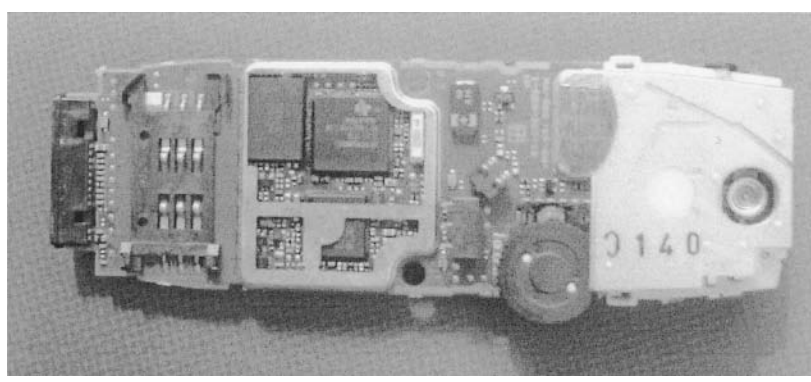


Figure 2-23. Photograph of the internal parts of a cellular phone.

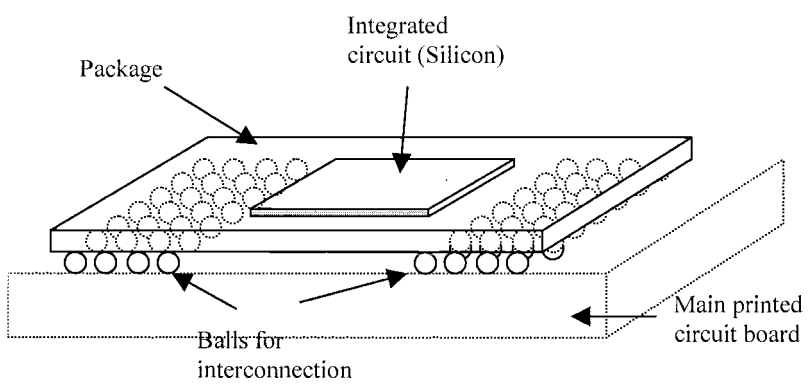


Figure 2-24. Typical structure of an integrated circuit.

The push for smaller size, reduced power supply consumption and enhancement of services has resulted in continuous technological advances, with possibilities for ever-higher integration.

The integrated circuit consists of a silicon die, which is usually around 1 cm x 1 cm in the case of microprocessors and memories. The integrated circuit is mounted on a package (Fig. 2-24) which is placed on a printed circuit board. The active part of the integrated circuit is only a very thin portion of the silicon die.

On the edge of the chip, small solder bumps are used as electrical connections between the integrated circuit and the package. The package itself is a sandwich of metal and insulator materials that convey the electrical signals to large solder bumps which interface with the printed circuit board.

Fig. 2-25 describes the evolution of the complexity of Intel ® microprocessors in terms of devices number on the chip. The Pentium IV ™ processor produced in 2003 included about 50,000,000 MOS devices integrated on a single piece of silicon no larger than 2 x 2 cm.

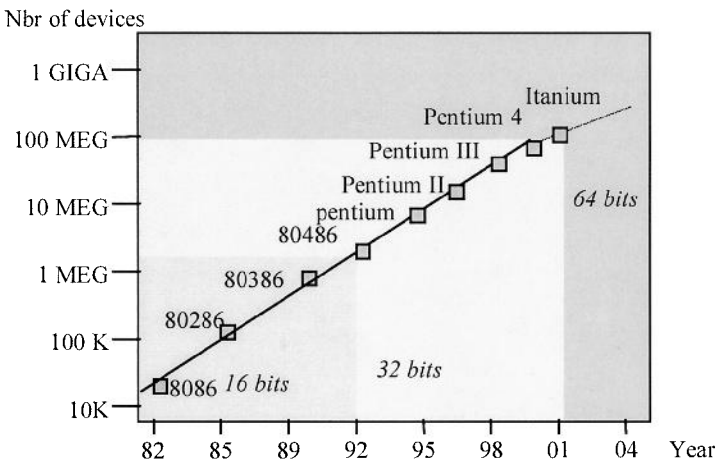


Figure 2-25. Evolution of microprocessors.

Fig. 2-26 illustrates the clock frequency increase for high-performance microprocessors and industrial micro-controllers with the technology scale down. The microprocessor roadmap is based on Intel processors used for personal computers, while the micro-controllers roadmap is based on Freescale micro-controllers used for high performance automotive industrial applications.

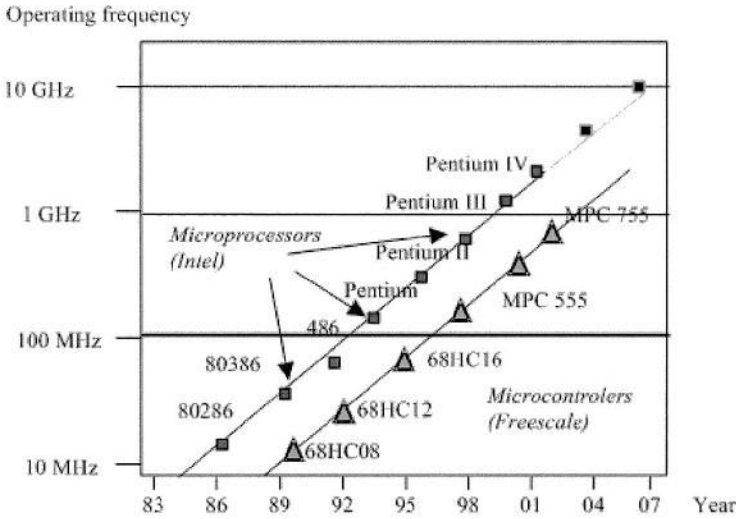


Figure 2-26. Increased operating frequency of microprocessors and micro-controllers.

The PC industry requires microprocessors running at the highest frequencies, which entails very high power consumption (30 Watts for the Pentium IV generation). The automotive industry requires embedded controllers with more and more sophisticated on-chip functionalities, larger embedded memories and interfacing protocols. The operating frequency follows a similar trend to that of PC processors, but with a significant shift.

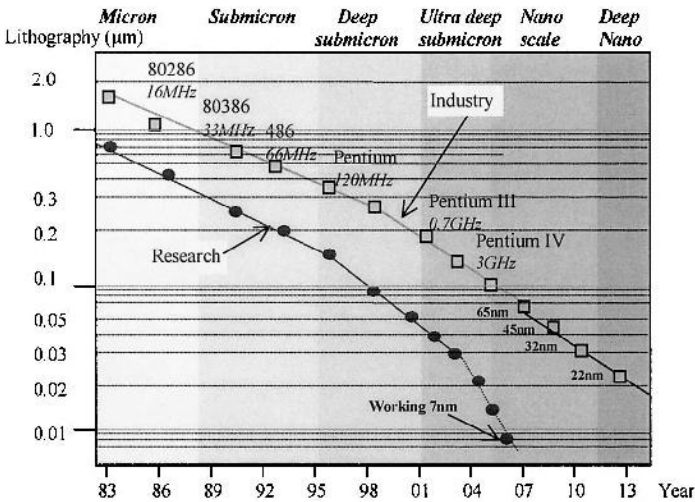


Figure 2-27. Evolution of lithography.

Let us consider four main generations of integrated circuit technologies: micron, submicron, deep submicron and ultra deep submicron technologies as illustrated in Fig. 2-27. The sub-micron era started in 1990 with the 0.8 μm technology. The deep submicron technology started in 1995 with the introduction of lithography better than 0.3 μm . Ultra deep submicron technology concerned lithography below 0.1 μm .

Nanoscale technologies started in 2004 with the 90 nm CMOS technology, followed by the 65 nm. Deep nanoscale technologies should include 32 nm and 22 nm processes, to appear in 2010-2013.

In Fig. 2-27, it is shown that research has always kept around 5 years ahead of mass production. It can also be seen that the trend towards smaller dimensions has accelerated since 1996. The lithography is expected to decrease down to 65 nm by 2007. The lithography expressed in μm corresponds to the smallest patterns that can be implemented on the surface of the integrated circuit. The main consequence of improved lithography is the ability to implement an identical function in an ever-smaller silicon area. Consequently, more functions can be integrated in the same space.

Moreover, the number of metal layers used for interconnects has increased steadily in the course of the past ten years. More layers for routing means a more efficient use of the silicon surface, as is the case for printed circuit boards. Active areas, i.e MOS devices, can be placed closer to each other if many routing layers are provided (Fig. 2-28).

The increased density provides two significant improvements: the reduction of the silicon area goes together with a decrease of the parasitic capacitance of junctions and interconnects, thus increasing the switching speed of cells. Secondly, the shorter dimensions of the device itself speed up the switching, which leads to further operating clock improvements.

When switching, each gate generates a small current pulse which flows mainly on the supply lines. The addition of these elementary current pulses provokes enormous current flows within the chip, close to 100 A in the latest generation of high performance microprocessors.

The increase in operating frequencies, circuit complexity and number of I/Os tends to increase interference, as well as conducted and radiated parasitic emission.

Meanwhile, the silicon wafer, on which the chips are manufactured, has constantly increased in size, thanks to the technological advances. A larger diameter means more chips fabricated at the same time, but it also requires ultra-high cost equipments able to manipulate and process these wafers with an atomic-scale precision. This trend is illustrated in Fig. 2-29. The wafer diameter for 0.12 μm technology is 8 inches or 20 cm (One inch is equal to 2.54 cm). The thickness of the wafer varies from 300 to 600 μm .

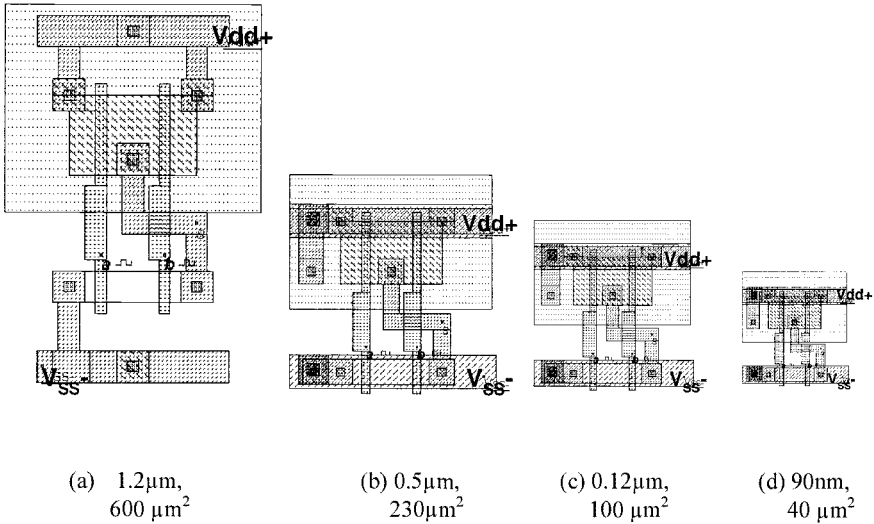


Figure 2-28. The evolution of the silicon area used to implement a basic logic gate.

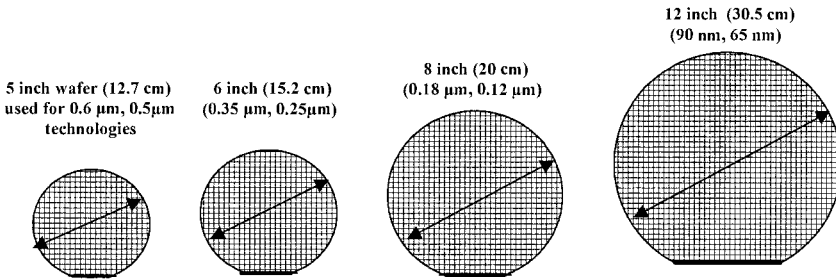









Figure 2-29. The silicon wafer used for patterning the integrated circuits.

8. PACKAGE ROADMAP

So far, the packaging of integrated circuit has been improved so as to increase the number of input/outputs (Table 2-2).

The packaging technology has rapidly improved in terms of I/O density, from the early Dual-in-line structures to the ultimate “Chip-scale” packaging (Fig. 2-30). The most common packaging technology for microprocessors and micro-controllers is the Ball-gate-array (BGA) and Fine pitch Ball Gate Array (FBGA) technology.

Table 2-2. Packaging aspect and I/O number.

Packaging	Definition	Maximum number of I/Os
	Dual In Line (DIL)	40
	Shrink Dual In Line (SDIL)	100
	Small Outline Package (SOP)	100
	Quad Flat Pack (QFP)	250
	Ball Gate Array (BGA)	1000
	Fine Pitch Ball Gate Array (FBGA)	3000
	Chip Scale Package (CSP)	>5000

The integrated circuit is usually connected to the package by bonding wires or solder balls. In the first case, the bonding wires are made of gold. The wires build the link between the pads and the package leads. An example of package connection using bonding wires is shown in Fig. 2-30, for a Quad Flat Pack (QFP).

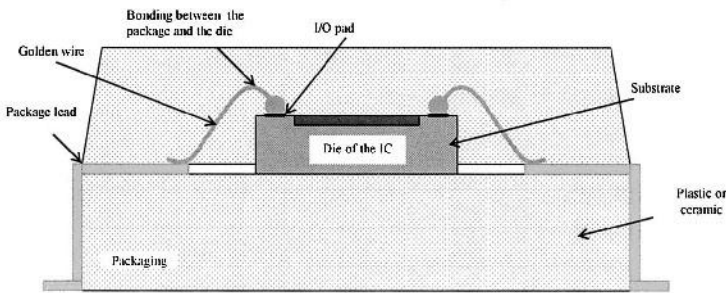


Figure 2-30. The structure of a Quad flat pack (QFP).

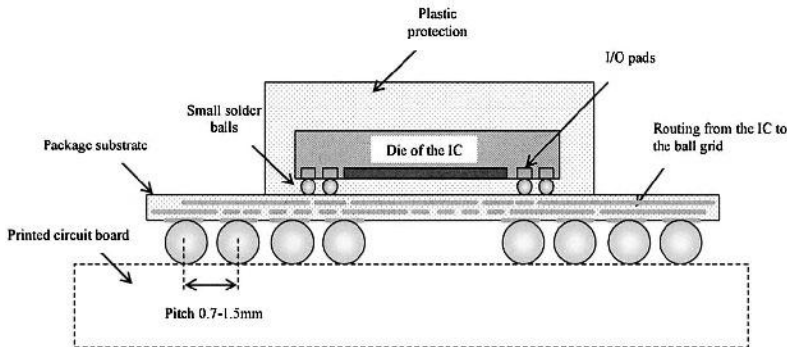


Figure 2-31. The die is attached to the package using micro balls, then the package is linked to the PCB via solder balls to the printed circuit board (BGA).

As the complexity of integrated circuits has kept increasing, a new type of link has been invented, thus creating all the connections between the die and the package in one single step. This technology, called ball grid array, was introduced some years ago and is now commonly used for integrated circuits with more than 200 pins. The cross-section of a ball-grid array and one integrated circuit example are proposed in Fig. 2-31. The die of the integrated circuit is flipped and connected to a specific package thanks to small solder balls.

The package is used as a routing matrix from the IC pads (Pitch close to $100\ \mu\text{m}$) to the ball gate array (Pitch between $500\ \mu\text{m}$ and $2\ \text{mm}$). The package is a complex network of very thin copper conductors embedded in an insulator. The BGA substrate may include from 2 to 6 metal layers to achieve the routing of general purpose signals and the distribution of power supply. In terms of parasitic emission, the trend towards a decrease of lead length reduces the antenna effects of the package and thus contributes to the decrease of parasitic emission. Furthermore, the reduced size of the leads also decreases the coupling of incident waves to the device, and consequently improves the integrated circuit immunity to radio frequency interference. This global trend has been confirmed by (Sketoe, 2000) with the analysis of IC susceptibility for various packaging technologies.

The chip scale packaging (CSP) shown in Fig. 2-32, consists in connecting directly the chip to the printed circuit board without any intermediate package substrate. The die is flipped and electrically connected to the board via solder balls. The routing constraints in the printed circuit board are very strict as the ball pitch may be as low as $200\ \mu\text{m}$. As there is no more antenna effect, both the emission and susceptibility of such packages should be very low, compared to previous package technologies. However, the die itself may act as a patch antenna for frequencies well above the GHz.

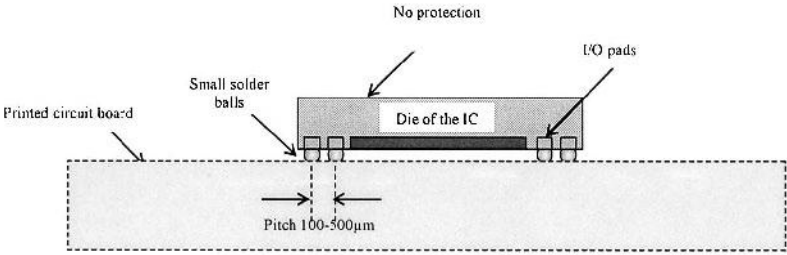


Figure 2-32. The principles of chip scale package

To reduce the surface of the electronic systems, the trend is to stack integrated circuits within a single package, also called System-in-Package. The benefit of this technique is mainly a much more compact system, yet it entails a much more complex assembly as well as reliability and thermal dissipation issues.

One example of stacked integrated circuits is shown in Fig. 2-33. Stacked integrated circuits are particularly attractive when processors, memories, power management, actuators, sensors and radio frequency elements are to be managed simultaneously.

Due to cost and reliability issues, the stacking of heterogeneous integrated circuits may be preferred to a single all-integrated die solution. In terms of EMC, the system-in-package raises the issue of near-field emission and susceptibility between a potential aggressor and its victim situated less than one millimeter away from each other. Coupling may be very strong and lead to a variety of parasitic effects such as capacitive and inductive coupling.

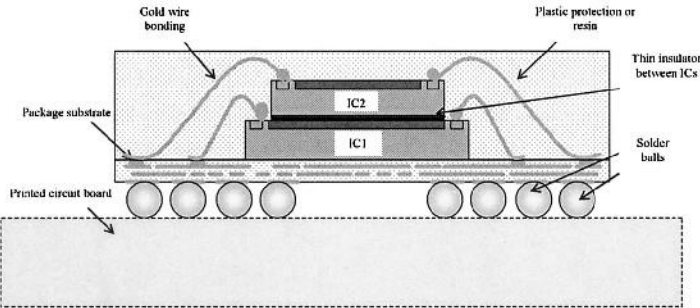


Figure 2-33. The stacking of two different dies in the same package.

9. EMC ISSUES

The need to characterize the electromagnetic compatibility (EMC) performance of integrated circuits (ICs) has been driven by the diverging requirements of semiconductor manufacturers and users on one hand and technology trends on the other.

Modern radio frequency equipments operate at frequency ranges officially called very-high frequencies (VHF), ranging from 30 MHz to 300 MHz, ultra-high frequencies (UHF) ranging from 300 MHz to 3 GHz, and super high frequencies (SHF) ranging from 3 GHz to 30 GHz. Mobiles phones and wireless networking have been the driving applications of radio-frequency integrated circuits, as described in Fig. 2-34.

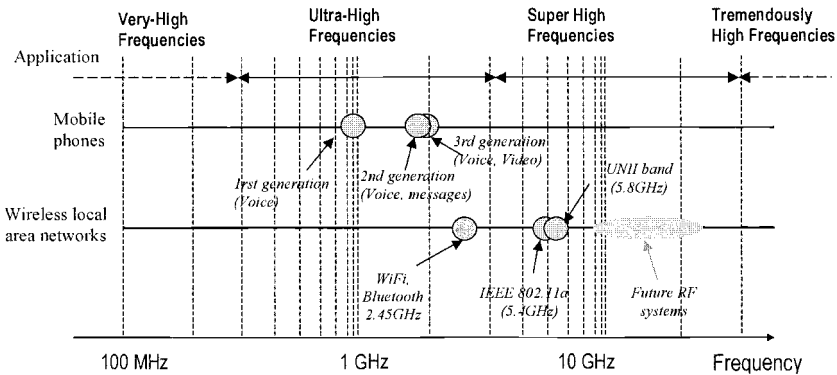


Figure 2-34. The mobile phones and WLAN systems in the frequency spectrum.

The emission spectrum which is strongly correlated with the operating clock frequency, tends to be shifted toward higher frequencies. The IC operating clock frequency, about 10 MHz for early 16-bit processors, is now approaching 1 GHz and is forecast to reach frequencies far beyond the GHz. The parasitic emission spectrum may interfere with several critical frequency bands such as FM radio, mobile phones or local wireless protocols like Bluetooth (Fig. 2-35). Considering the evaluation of parasitic emission level once the integrated circuit has been fabricated, conventional IC design methodologies are obsolete: they often require a redesign with the help of EMC experts (Fig. 2-36).

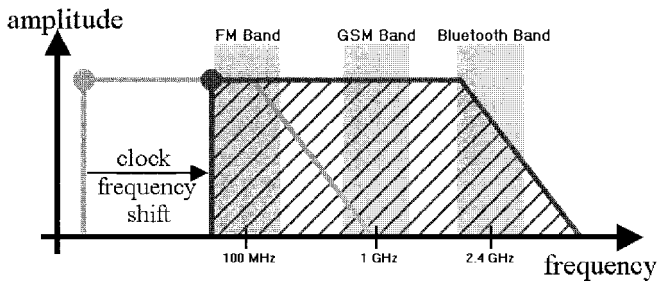


Figure 2-35. Consequences of operating clock increase: parasitic emissions can reach critical frequency bands.

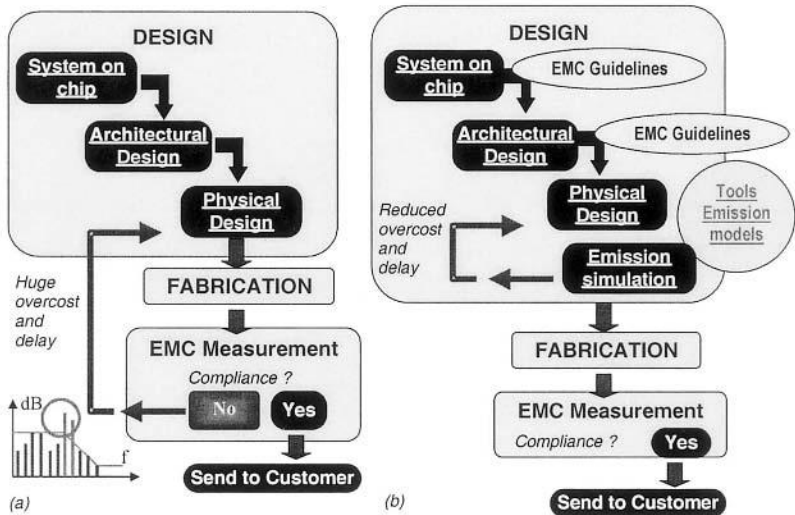


Figure 2-36. Conventional IC design methodologies (a) and low emission design methodologies (b).

But including reduction techniques in the early design phases and simulating the parasitic emission before fabrication, as suggested by low emission design methodologies, require efficient IC models and adequate tools. As a low parasitic emission can represent a significant commercial argument for choosing an integrated circuit, several approaches for reducing parasitic emission at chip level have recently been proposed. Various design strategies have proven efficient to reduce the parasitic emission by several dB for micro-controllers.

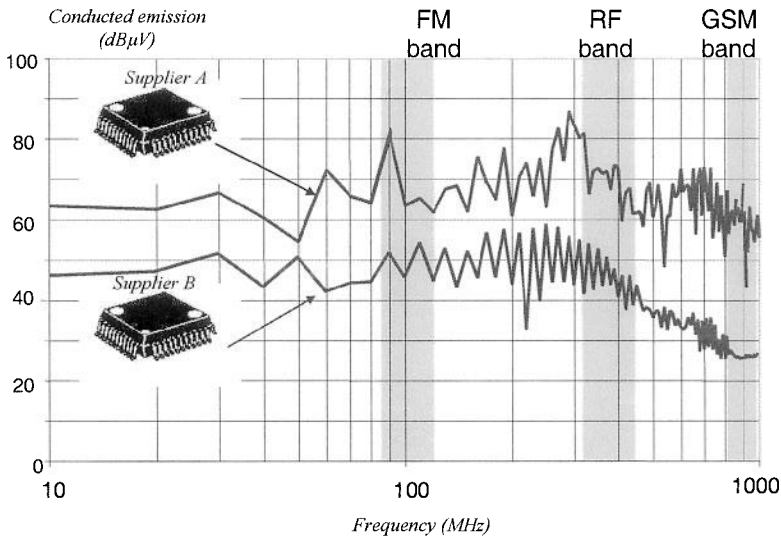


Figure 2-37. Two ICs from different suppliers may exhibit significant differences in terms of parasitic emission.

Fig. 2-37 shows a comparison between two pin-compatible ICs from two different suppliers, mounted on the same test board and measured on the same test bench. Significant differences can be noticed.

Effective techniques involve on-chip decoupling capacitance, current-limiting choke resistance, and supply network optimization. Such design techniques are described in chapter 7. Distributing decoupling capacitors close to main current sources (CPU, clock drivers, PLLs), in combination with current-limiting resistors in series on the supply lines have turned out to reduce the peak harmonics by 10-20 dB.

Other techniques for reducing the parasitic emission concern the use of low-swing clock signals, or asynchronous design approaches.

10. CONCLUSION

Due to increased expectations for low emission and highly immune ICs, EMC measurement methods have been standardized, EMC design guidelines for ICs have been proposed, and later EMC performance prediction tools have been developed since research in that field started in 1970. We expect this field to remain quite active in the future, due to continuous demand towards more complex circuits, higher clock speeds, and lower supply voltages.

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Techniques for low emission and susceptibility

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