

CHAPTER 2

The Altera UP 3 Board

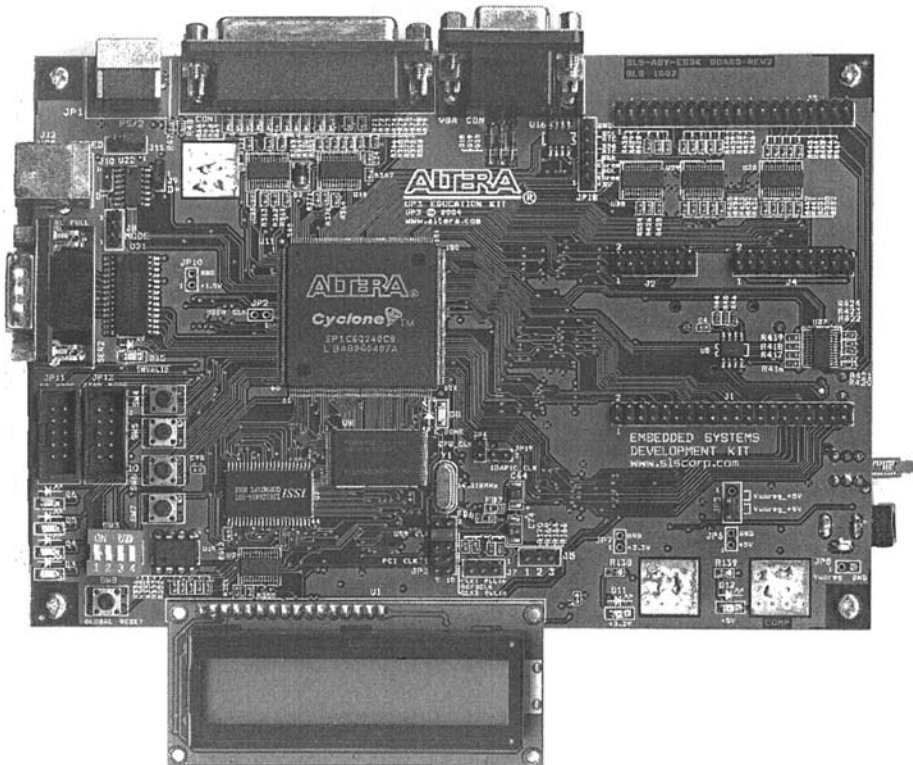


Photo: The Altera UP 3 board contains a Cyclone FPGA, external SRAM, SDRAM & Flash memory, and a wide assortment of I/O devices and connectors.

2 The Altera UP 3 Board

The Altera University Program 3 (UP 3), FPGA design laboratory board is shown in Figures 2.1 and 2.2. This board contains a Cyclone FPGA, several external memory devices and a wide range of I/O features. Two versions of the UP3 board are currently available with either a Cyclone EP1C6Q240 or the larger EP1C12Q240 FPGA. The FPGA and memory devices can be programmed using a JTAG ByteBlasterII cable attached to a PC printer port. An external 6V DC power supply or an AC to DC wall adapter is used to provide power. An on-board clock oscillator and clock chip provides several clock signals that are selectable with the board's jumpers.

Note the orientation of the LCD Display module in Figure 2.1 and how it extends beyond to edge of the board. Do not plug the module in backwards as it may damage the LCD by reversing its power connections.

A ByteBlasterII programming adapter cable is supplied with the UP 3 board and it connects the UP 3 board to the PC's parallel port (LPT) for device programming. The printer port mode of the PC should be set in the PC's BIOS to ECP or EPP.

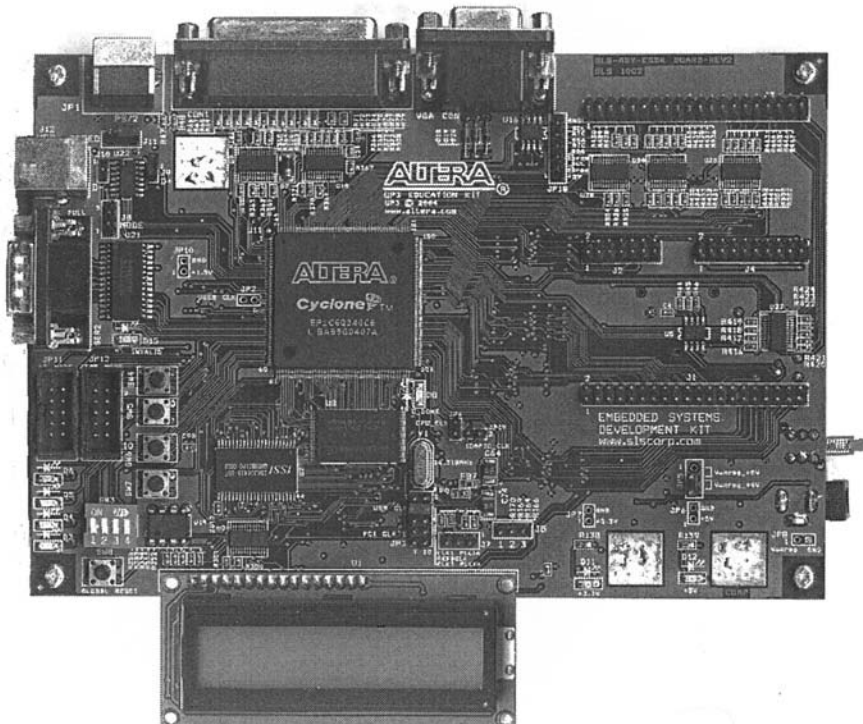


Figure 2.1 The Altera UP 3 board.

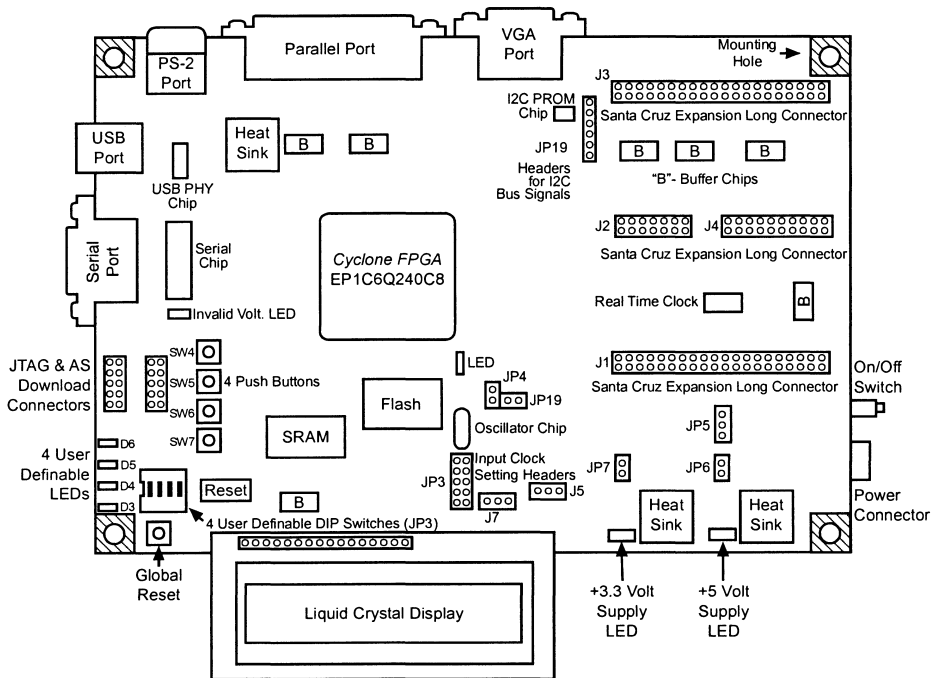


Figure 2.2 The Altera UP 3 board's features.

2.1 The UP 3 Cyclone FPGA Features

The Cyclone FPGA is the large square chip located in the center of the UP 3 board as seen in Figure 2.1. Two versions of the UP 3 are currently available. The 312 model has the larger EP1C12 and the 306 model uses the EP1C6 as seen in Table 2.1. There are some minor pin changes between the EP1C6 and EP1C12 board's LCD and memory devices. You must also compile your design for the correct Cyclone device assignment or it will not download the device.

Table 2.1 UP 3 Board's Cyclone FPGA Features

Cyclone FPGA Feature	EP1C6Q240	EP1C12Q240
Logic Elements (LEs)	5,980	12,060
4K bit RAM blocks (M4Ks)	20	52
Total Internal RAM bits	92,160	239,616
Phase Locked Loops (PLLs)	2	2
User I/O pins	185	173

2.2 The UP 3 Board's Memory Features

In addition to the Cyclone FPGA's internal memory, the UP 3 board provides several external ROM and RAM memory devices as seen in Table 2.2. Capacities of external memory are much larger than the internal memory, but they will have a longer access time. FPGA processor cores such as the Nios use external memory for program and data memory and the FPGA's internal memory for register files and cache. Flash and EEPROM are used to provide non-volatile memory storage. The EPCS1 serial Flash chip is used to automatically load the FPGA's serial configuration data at power up in systems where you do not want to download the board with the ByteBlaster II each time power is applied. Links to datasheets for all of the UP 3 board's chips can be found at the book's website.

Table 2.2 UP 3 Board's Memory Features

Memory Device	Size	Part Number
SRAM	64K by 16 bits	ISSI IS61C6416
SDRAM	1M by 16 bits	ISSI IS42S16400B
Flash Memory	1M by 16 bits	Toshiba TC58FVB106AFT-70
I ² C EEPROM	16K by 1bit	ISSI IS24C16
Serial Flash Memory	1M by 1bit	Altera EPCS1

2.3 The UP 3 Board's I/O Features

The UP 3 board provides a wide variety of I/O features as summarized in Table 2.3. For most devices, the UP 3 board's hardware provides only an electrical interface to the FPGA's I/O pins. Logic that provides a device interface circuit or controller will need to be constructed using the FPGA's internal logic. Many design examples of interfacing these various I/O devices can be found in the following chapters of this book.

The Cyclone FPGA is a surface-mount chip that it is soldered directly to the board. It is difficult if not impossible to replace the Cyclone chip without expensive surface mount soldering equipment, so extreme care should be exercised when interfacing the Cyclone I/O pins to any external devices.

Also, remember to assign pins as shown in the tutorials to avoid randomly turning on several of the memory devices at the same time. A tri-state bus conflict occurs when several tri-state outputs are turned on and they attempt to drive a single signal line to different logic levels. It is possible that such a tri-state bus conflict on the memory data bus could damage the devices by overheating them after several minutes of operation.

Table 2.3 Overview of the UP 3 Board's I/O Features

I/O Device	Description	Hardware Interface Needed
USB 1.1	Full Speed and Low Speed	Processor & USB SIE engine core
Serial Port	RS 232 Full Modem	UART to send and receive data
Parallel Port	IEEE 1284	State machine or Proc. for handshake
PS/2 Port	PC Keyboard or Mouse	Serial Data - PS/2 state machine
VGA Port for Video Display on Monitor	RGB three 1-bit signals provide 8 colors	State machine for sync signals & user logic to generate RGB color signals
IDE Port	Connector	Processor & IDE Device Driver
Reset Switch	Use for Global Reset	Must use a reset in design
Pushbutton Switches	4 Non-debounced (0=HIT)	Most applications will need a switch debounce Circuit
Expansion Card	Santa Cruz Long 72 I/O	Depends on expansion card used
LEDs	4 User Definable (1=ON)	None
LCD Display	16 Character by 2 line ASCII Characters	State machine or Processor to send ASCII characters and LCD commands
Real Time Clock	I ² C clock chip	Serial Data - I ² C state machine
DIP Switch	4 Switches (1=ON)	None or Synchronizer Circuit

WHEN CONNECTING EXTERNAL HARDWARE, ADDITIONAL PINS ARE AVAILABLE FOR USE ON THE SANTA CRUZ EXPANSION CONNECTORS ON THE BOARD. REFER TO THE UP 3 EDUCATION KIT REFERENCE MANUAL FOR DETAILS. THIS MANUAL COMES WITH THE UP 3 BOARD AND IS AVAILABLE FREE AT [HTTP://WWW.ALTERA.COM](http://www.altera.com) OR AT [HTTP://WWW.SLSCORP.COM](http://www.slscorp.com).

Table 2.4 contains the pin assignments and names used for the UP 3 board's most commonly used I/O devices. Pin differences for the larger 1C12 UP 3 board are listed in parenthesis. The larger 1C12 has twelve additional power and ground pins, so fewer pins are left for general purpose I/O.

NOTE: If you ever switch between 1C6 and 1C12 boards, you will need to change the device, fix the pin assignments, and then recompile for the new FPGA device. A complete table including all I/O devices can be found in Appendix C. The voltage levels on FPGA pins can vary, so be sure to check for the proper voltage levels when selecting an I/O pin to interface new external hardware to the board. 5V logic levels are available on J3.

Do not connect high current devices such as motors or relay coils directly to FPGA I/O pins. These pins cannot provide the high current levels needed, and it may damage the FPGA's output circuit.

Table 2.4 UP 3 Board's most commonly used FPGA I/O pin names and assignments

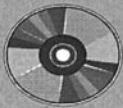
Pin Name	Pin#	Pin I/O Type	Function of Pin
PS2_CLK	12	Bidirectional	PS2 Connector
PS2_DATA	13	Bidirectional	PS2 Connector
RESET	23	Input	Power on or SW8 pushbutton reset (Reset = 0)
USB_CLK	29	Input	USB 48MHz Clock - jumper
USER_CLOCK	38	Input	External Clock from J2 Pin 2
PBSWITCH_4	48	Input	Pushbutton SW4 (non-debounced, 0 = button hit)
PBSWITCH_5	49	Input	Pushbutton SW5 (non-debounced, 0 = button hit)
LCD_E	50	Output	LCD Enable line
LED_D6	53	Output	LED D3 (0 = LED ON, 1= LED OFF)
LED_D5	54	Output	LED D4 (0 = LED ON, 1= LED OFF)
LED_D4	55	Output	LED D5 (0 = LED ON, 1= LED OFF)
LED_D3	56	Output	LED D6 (0 = LED ON, 1= LED OFF)
PBSWITCH_6	57	Input	Pushbutton SW6 (non-debounced, 0 = hit)
DIPSWITCH_1	58	Input	DIP Switch SW3 #1 (ON = 1, OFF = 0)
DIPSWITCH_2	59	Input	DIP Switch SW3 #2 (ON = 1, OFF = 0)
DIPSWITCH_3	60	Input	DIP Switch SW3 #3 (ON = 1, OFF = 0)"
DIPSWITCH_4	61	Input	DIP Switch SW3 #4 (ON = 1, OFF = 0)
PBSWITCH_7	62	Input	Pushbutton SW7 (non-debounced, 0 = hit)
LCD_RW	73	Output	LCD R/W control line
MEM_DQ[0]	94	Bidirectional	Memory/LCD Data Bus
MEM_DQ[1]	96(133)	Bidirectional	Memory/LCD Data Bus
MEM_DQ[2]	98	Bidirectional	Memory/LCD Data Bus
MEM_DQ[3]	100	Bidirectional	Memory/LCD Data Bus
MEM_DQ[4]	102(128)	Bidirectional	Memory/LCD Data Bus
MEM_DQ[5]	104	Bidirectional	Memory/LCD Data Bus
MEM_DQ[6]	106	Bidirectional	Memory/LCD Data Bus
LCD_RS	108	Output	LCD Register Select Line
MEM_DQ[7]	113	Bidirectional	Memory/LCD Data Bus
VGA_GREEN	122	Output	VGA Connector Green Video Signal
CPU_CLOCK	153	Input	CPU Clock 100 or 66MHz - jumper
VGA_BLUE	170	Output	VGA Connector Blue Video Signal
VGA_VSYNC	226	Output	VGA Connector Vert Sync Signal
VGA_HSYNC	227	Output	VGA Connector Horiz Sync Signal
VGA_RED	228	Output	VGA Connector Red Video Signal

2.4 Obtaining a UP 3 Board and Cables

UP 3 boards are available for purchase from Altera's University Program at special educational pricing for schools and students (www.altera.com). UP 3 education kits come with an AC to 6V DC power supply, a special serial cable, and a ByteBlasterII cable.

A Longer Cable for the ByteBlaster

For use with the UP 3 or UP 2 board, a longer 25pin to 25pin PC M/F parallel printer cable is useful since the 1 foot Byteblaster II cable provided with the boards is often too short to reach the PC's printer port. All 25 wires must be connected in the printer extension cable. Any computer store should have these cables. A three-foot well-shielded cable works best. Avoid using extra long cables or very low-cost cables without good shielding as they can cause problems.



ADDITIONAL UP 2 RELATED MATERIALS CAN BE FOUND IN THE CD-ROM
CHAPTER DIRECTORIES IN THE \UP2 SUBDIRECTORY.



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