

## Chapter 2

# NOISE ANALYSIS AND DESIGN IN DEEP SUBMICRON

Traditionally, area-minimization and speed-maximization were the only factors relative to a design's effectiveness that were measured. Low power, high-throughput, and computationally intensive circuits are also critical application domains<sup>1</sup>. In addition to these three design parameters; area, speed, and power, there are two design metrics, which have been of great importance to current designs. These metrics are noise and reliability<sup>3,4</sup>. The five metrics are shown in Fig. 2-1 with an arrow associated to show whether this metric should be increased or decreased.

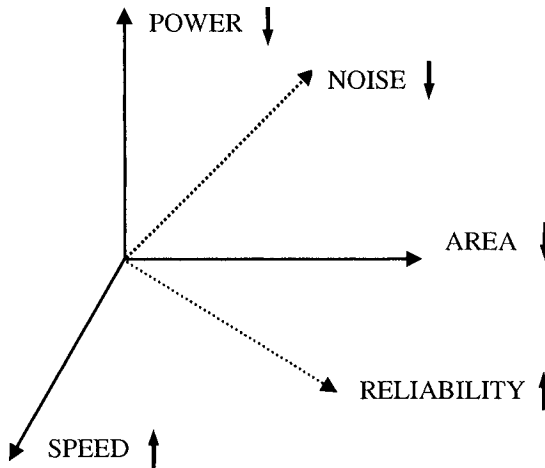


Figure 2-1. Design metrics.

The current trend of technology scaling is predicted to continue. Feature sizes will continue to shrink to very deep submicrometer (VDSM) dimensions while clock frequencies will continue to increase. Shrinking feature size implies not only shorter gate lengths but also decreasing interconnect pitch and device threshold voltages. Now, a single IC can contain an entire system (a system-on-a-chip, SOC), and the interconnections can have many interleaved signal layers and multiple planes of interconnect. Reduction in the top and bottom areas of a minimum-width wire means that total wire capacitance is decreasing. Resistance, however, is increasing faster, despite efforts not to scale metal thickness. Practical efforts to control RC delays through the use of low-resistivity metal (copper), low-dielectric-constant insulators, and wide, thick wiring will require future interconnection analysis to consider inductance and inductive coupling. It is projected that use of a lower resistivity metal (copper) and that replacement of silicon dioxide ( $k \sim 4$ ) with various insulating materials of a progressively lower dielectric constant ( $k \sim 2-3$ ) will be adopted in the chip fabrication process. The use of copper will reduce degradation of signal propagation delay time due to voltage drop on power lines. The use of low  $k$  dielectrics will decrease the degradation of signal propagation delay time by reducing capacitive coupling. While technology scaling results in lower threshold voltages, the threshold voltage magnitude determines noise immunity in these circuits.

## 2.1 NOISE

The term noise in digital VLSI systems has come to mean any unwanted deviation in the voltages and/or currents at various nodes within a circuit. When noise acts against a stable logic level on a circuit node, it can transiently destroy logical information carried by the node. If this ultimately causes an incorrect machine state stored in a latch, functional failure will result. Even when noise does not cause functional failure, it has an impact on timing, affecting both delay and slew. Also, noise can cause the dissipation of extra power due to incorrect switching.

Digital circuits create deterministic noise several orders of magnitude greater than noise from stochastic physical sources. Problems due to these noise sources were first observed in mixed signal applications, which plunged highly noise-sensitive analog circuits into a noisy digital environment. Although digital circuits create much more noise than analog circuits, digital systems are prevalent because they are inherently immune to noise. Valid voltage ranges for defining the digital 0 and 1 are shown in Fig. 2-2.

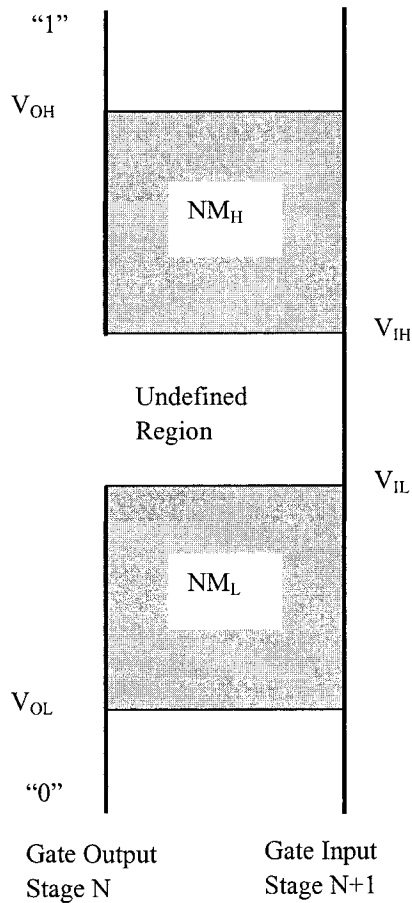


Figure 2-2. A range of analog voltages defines the digital 0 and 1.

The inherent noise immunity of digital circuits is due to the presence of high-gain restoring logic gates such as the inverter shown in Fig. 2-3, which has a very nonlinear voltage transfer characteristic. However, as power supply levels have decreased, this advantage has diminished. Thus, the problem of noise has increased in importance such that on-chip noise is the main research area for continuing the growth in integrated circuit density and performance.

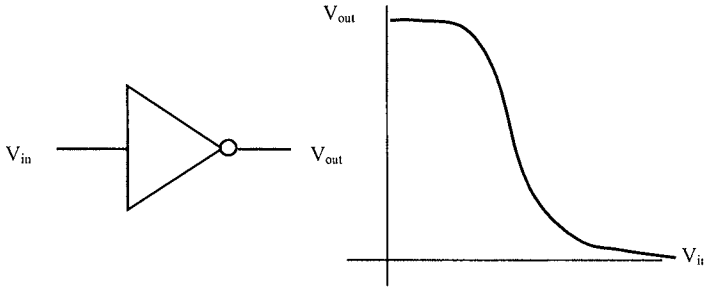


Figure 2-3. Inverter nonlinear voltage transfer characteristics.

With technology scaling, noise is a problem affecting all types of designs from custom microprocessors to standard-cell ASICs. A noise analysis solution must be capable of analyzing tens of millions of transistors, considering both circuit and interconnect noise, and evaluating the distinct noise tolerances of each node in the circuit. Successful design methodologies incorporate a three-level noise strategy. The first line of defense is a set of noise avoidance rules to guide circuit and interconnect design. These rules should prevent most noise problems without introducing too much area or timing constraints. Next, a detailed static noise analysis of the design should find all possible noise failures. Finally, careful circuit simulation should determine whether the design could tolerate some failures flagged by static noise analysis.

## 2.2 RELIABILITY

One of the most important attributes of any system is its reliability. It is imperative to consider reliability into complex chips even more carefully as the chip functionality increases almost without limit. This important issue is addressed with emphasis on how to consider reliability from early design phases<sup>4</sup>, rather than treating reliability assurance as a backend manufacturing process. As CAD tools have played key roles in developing integrated circuits and systems, new reliability analysis tools need to be developed and used in SOC design. For more than a decade, new CAD capabilities have been developed with reliability focus, specifically to address reliability concerns due to hot carrier induced degradation of circuits, electromigration, ESD, crosstalks, leakage currents and high power dissipation.

It was also reported in ITRS 1999 Edition 5 that computer-aided design (CAD) tools would need to incorporate contextual reliability considerations in the design of new products and technologies. It is essential that advances in failure mechanism understanding and modeling, which result from the use

of improved test methodologies, be used to provide input data for these new CAD tools. With these data and smart reliability CAD tools, the impact on product reliability of design selections can be evaluated. New CAD tools need to be developed that can calculate degradation in electrical performance of the circuit over time. The inputs used would be the predicted resistance increases in interconnect wires and vias in the circuit based on the following:

- wire length;
- current densities;
- calculated local operating temperature, which includes the effects of Joule heating in the circuit element and elsewhere.

These specific tools will need to become an integral part of the circuit designer's tool set. They will help to predict product reliability before processing begins and to develop solutions that anticipate technology and thereby, accelerate their introduction.

## 2.3 NOISE SOURCES

Serious on-chip electrical problems are being encountered in DSM. These problems include signal distortion along coupled interconnect lines, voltage variations in the power supply distribution, substrate coupling, charge sharing, charge leakage, process variation, thermal noise, and alpha particles, each of which is a major source of on-chip noise in VLSI circuits.

### 2.3.1 Interconnect crosscapacitance noise

Interconnect Crosscapacitance noise refers to the charge injected in quiet wires (victims) by neighboring switching wires (aggressors) through the capacitance between them (Crosscapacitance). The resulting noise has the form of a pulse in which the leading edge is determined by the switching slew of the aggressor and the trailing edge is determined by the restoring time constant of the victim. This is perceived to be the most significant source of noise in current processes, Fig. 2-4. If the net is a dynamic node, the restoring time is infinite and the node will never recover. It can lead to setup violations in downstream latches or flip-flops. Also when the aggressors are switching in the same direction of the victim, the transport delay and slew decreases, leading to hold time violations.

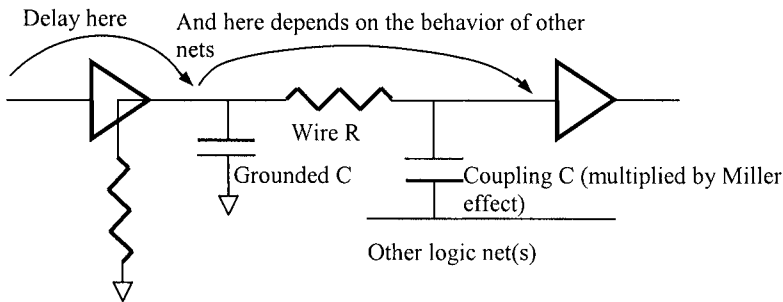


Figure 2-4. Various noise sources for digital circuits.

### 2.3.2 Charge sharing noise

Charge sharing noise is caused by charge redistribution between a dynamic evaluation node and intermediate nodes in pull up or pull down logic stack, Fig. 2-5. This primarily impacts domino nodes, weakly driven pass gate latches, and dynamic latches. The primary technology variable here is the ratio of junction capacitance to gate and interconnect capacitance. For most circuits, this noise is not dramatically changed with technology scaling.

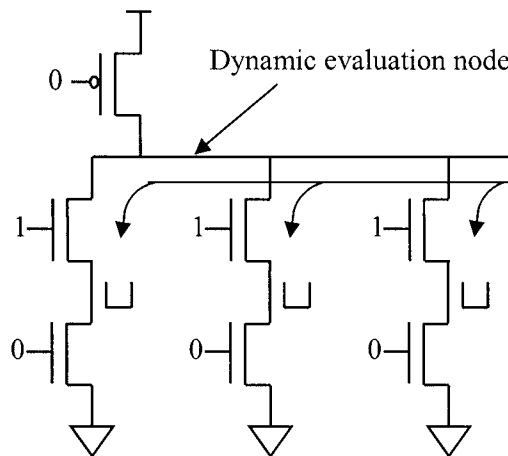


Figure 2-5. Charge sharing noise

### 2.3.3 Charge leakage noise

Charge leakage noise is mainly composed of subthreshold conduction in nominally off transistors. The leakage current can either charge/discharge a dynamic node or cause the stable state of a weakly held node to be significantly different from rails. This is mainly a concern for wide domino NOR, PLA, and memory arrays. This current rises exponentially with reduction in the threshold voltage and is becoming very significant in DSM. It is helped greatly by feedback devices.

### 2.3.4 Power supply noise

Power supply noise is the difference between the local voltage references of the driver and the receiver. The increased amount of current on power supply lines causes a raise in IR drop on voltage references. This makes the gate more highly sensitive to noise spikes. This low frequency component (IR drop) is managed well by flip-chip C4 packaging, which provides a very low resistance current path. Besides, the higher speed transients allowed by scaled transistor sizes is associated with higher  $L di/dt$  due to the large package and on chip inductances. Furthermore, the decoupling capacitance of the circuit is decreased due to the reduced sizes of the gates. Power supply noise is a dominant factor in the design of wide domino circuits and in circuits using contention where the AC logic level is shifted with respect to power supply rails. To counter these problems in high speed designs, several physical design techniques have been proposed: sizing up the P/G lines to accommodate the large current peaks and to minimize the IR and  $L di/dt$  voltage variations in these lines<sup>6</sup>; increasing the number of P/G pins; and deploying decoupling capacitors in the P/G lines<sup>2,7</sup>; performing clock skew scheduling to minimize the number of simultaneous switching<sup>8</sup>; and using copper in place of aluminum to overcome the increased resistance of scaled interconnect.

### 2.3.5 Mutual inductance noise

Mutual inductance noise occurs when signal switching causes transient current to flow through the loop formed by the signal wire and current return path<sup>9</sup>, thereby creating a changing magnetic field, Fig. 2-6. This induces a voltage on a quiet line, which is in or near this loop. These noise sources can be cumulative if there are several signals switching simultaneously in a bus. Mutual inductance is a long-range phenomenon and, hence, is worse in the presence of wide busses. High-speed switching and synchronous bus structures are making this noise very significant in current technologies.

Inductive noise can combine with capacitive noise to cause even worse noise than shown in Fig. 2.6. Because the analysis of inductive effects is highly dependent on layout and is quite complex, the approach is usually to solve the problem out through rules rather than analyze arbitrary configurations.

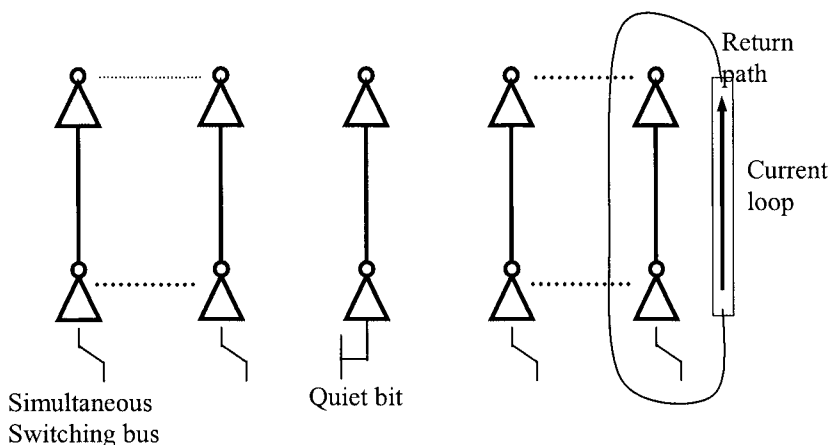


Figure 2-6. Mutual inductance noise from simultaneous switching on a wide bus.

### 2.3.6 Thermal noise

Thermal effects are an inseparable aspect of electrical power distribution and signal transmission through the interconnects due to self-heating (or Joule heating) caused by the flow of current. Thermal effects impact interconnect design and reliability in the following ways: First, they limit the maximum allowable RMS current density (since the RMS value of the current density is responsible for heat generation) in the interconnects, in order to limit the temperature increase. Second, interconnect lifetime (reliability), which is limited by electromigration (EM) (transport of mass in metals under an applied current density), has an exponential dependence on the inverse metal temperature. Hence, temperature rise of metal interconnects, due to self-heating phenomena, can also limit the maximum allowed average current density, since EM capability is dependent on the average current density<sup>10</sup>. Third, thermally induced open-circuit metal failure under short-time high peak currents (including ESD) is also a reliability concern<sup>11</sup> and can introduce latent EM damage that has important reliability implications<sup>12</sup>. It has been argued that thermal effects will increasingly dominate interconnect design rules that specify maximum current densities for circuit designers<sup>13</sup>. Recently, Hunter<sup>14</sup> has followed up on this issue by



solving the EM lifetime equation for Al-Cu, and the 1D heat equation in a self-consistent manner. In this approach, both EM and self-heating can be comprehended simultaneously.

### 2.3.7 Process variation

The typical characteristics of the process like the gate oxide can vary among wafers or even on a single die. The devices and their properties are defined only within a certain margin and hence will affect the performance of the circuit.

## 2.4 NOISE REDUCTION TECHNIQUES

Noise reduction techniques can be classified into four categories: signal-encoding schemes, which have been proposed to minimize transition activities on buses; circuit techniques to make circuits more immune to noise; interconnect structures techniques, which are changing the interconnect topology, wire sizing, spacing, and buffer locations; and high-level synthesis techniques. In addition to these categories, using new materials in interconnect including fiber optics or electromagnetic transmission, 3D interconnects which uses multiple levels of active devices, and new packaging methodologies<sup>1</sup> are some other techniques.

The most common techniques for reducing noise in digital circuits include disallowing of

- Pass gates at the ends of long wires
- Long wire runs feeding domino gate inputs
- Single n-FET or p-FET pass gates because of the  $V_t$  voltage drop they cause
- High-beta static circuits feeding low beta static circuits or vice-versa.

### 2.4.1 Signal encoding techniques

Increased coupling effect between interconnects in ultra deep sub-micron technology not only aggravates the power-delay metrics but also deteriorates the signal integrity due to capacitive and inductive crosstalk noises. Conventional approaches to interconnect synthesis aim at optimal interconnect structures in terms of interconnect topology, wire width and spacing, and buffer location and sizes<sup>15</sup>.

Signal encoding schemes have been proposed to minimize transition activities on buses while ignoring cross-coupled capacitances. When statistical properties are unknown a priori, the bus-invert method<sup>16</sup> and the

on-line adaptive scheme<sup>17</sup> can be applied to encode randomly distributed signals. On the other hand, highly correlated access patterns exhibit a spatio-temporal locality, which can be exploited for energy reduction<sup>18</sup> in Gray code<sup>19,20</sup>, the T0 method<sup>21</sup>, the working-zone encoding<sup>22</sup>, the combined bus-invert/TO<sup>23</sup>, and the coupling-driven method<sup>24</sup>. Lower bounds for minimum achievable transition activity have been derived for noiseless buses<sup>25</sup> and for noisy buses<sup>26</sup>. A segmentation method was introduced to reduce power consumption<sup>27</sup>. In specification, transformation approaches were used to reduce the number of memory accesses at the behavioral level<sup>28</sup>. The effectiveness of various encoding schemes was compared at the system level<sup>29</sup>.

#### 2.4.1.1 Bus-invert encoding

The bus-invert coding has been introduced to reduce the bus activity: Hamming distance between the consecutive binary numbers. If the Hamming distance of the two consecutive binary numbers is more than half of the word length, the latter binary number is sent in inverted polarity by asserting an additional signal line that indicates bus inversion<sup>16</sup>. It can be used to reduce the weight (the number of ones or zeros) of the binary numbers if the bus-inversion decision is made when the weight is more than half of the bus width. The bus-invert method is as follows:

1. Compute the Hamming distance (the number of bits in which they differ) between the present bus value (also counting the present invert line, Fig. 2-7) and the next data value.
2. If the Hamming distance is larger than  $n/2$ , set invert = 1 (and thus make the next bus value equal to the inverted next data value).
3. Otherwise, let invert = 0 (and let the next bus value equal to the next data value).
4. At the receiver side, the contents of the bus must be conditionally inverted according to the invert line, unless the stored data are not encoded as it is (e.g., in a RAM). In any case, the value of invert must be transmitted over the bus (the method increases the number of bus lines from  $n$  to  $n + 1$ ).

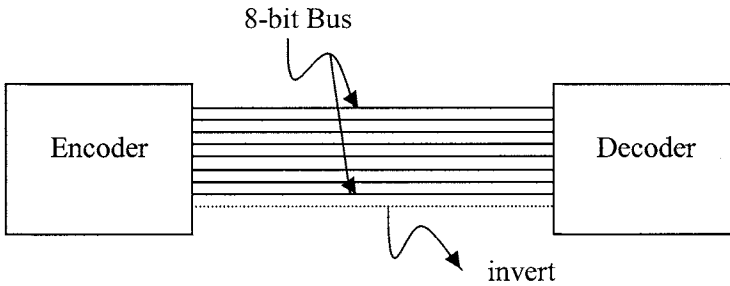


Figure 2-7. Invert signal in bus-invert method.

#### 2.4.1.2 The Gray code encoding

Gray code has only one-bit different in consecutive numbering for addressing. Due to the locality of program execution, Gray code addressing can significantly reduce the number of bit switches. Experimental results show that for typical programs running on a RISC microprocessor, using Gray code addressing reduces the switching activity at the address lines by 30~50% compared to using normal binary code addressing.

#### 2.4.1.3 The TO encoding

The bus transitions are reduced by freezing the address lines when consecutive patterns are found to be sequential. An extra bus line is employed to inform the receiver side whether or not the current pattern is sequential.

#### 2.4.1.4 The working-zone encoding (WZE)

The basis of the WZE technique is as follows:

1. It takes into account the locality of the memory references: applications favor a few working zones of their address space at each instant. In such cases, a reference can be described by an identifier of the working zone and by an offset. This encoding is sent through the bus.
2. The offset can be specified with respect to the base address of the zone or to the previous reference to that zone. Since we want small offsets encoded in a one-hot code, the latter approach is the most convenient. As a simple example, consider an application that works with three vectors (A, B, and C) as shown in Fig. 2-8. Memory references are often interleaved among the three vectors and frequently close to the previous reference to the vector. Thus, if both the sender and the receiver had three

registers (henceforth named holding a pointer to each active working zone, the sender would only need to send:

1. the offset of the current memory reference with respect to the association to the current working zone;
2. an identifier of the current.

To reduce the number of transitions, the offset is encoded in a one-hot code. Since the one-hot code produces two transitions if the previous reference was also in the one-hot code, and an average of  $n/2$  transitions when the previous reference is arbitrary, using a transition-signaling code reduces the number of transitions.

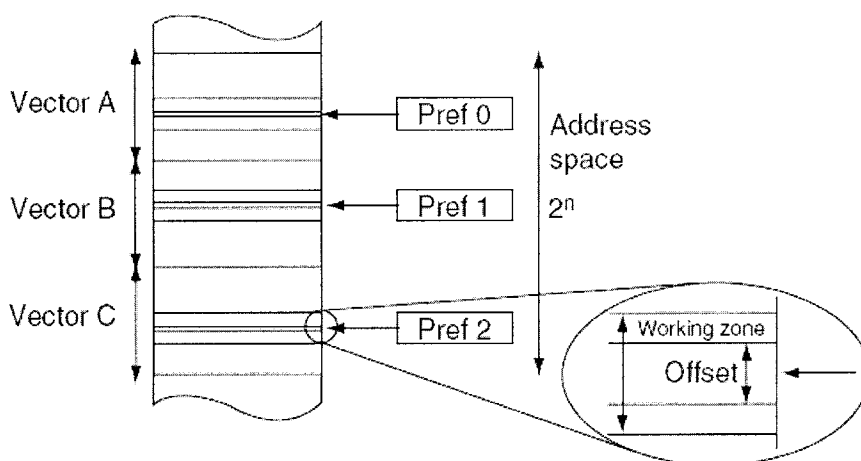


Figure 2-8. Address space for three vectors.

#### 2.4.1.5 Coupling-driven signal encoding

The key idea is that transforming the signal sequences traveling on-chip buses that are closely placed could alleviate coupling effects<sup>24</sup>. Small blocks of encoding and decoding logic are employed at the transmitter and receiver of on-chip buses as shown in Fig. 2-9.

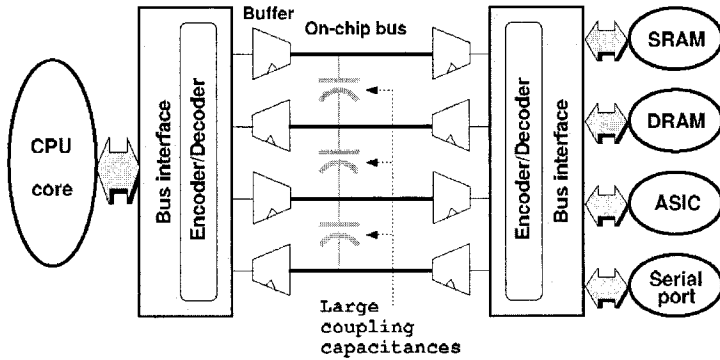


Figure 2-9. Tightly cross-coupled on-chip buses in a system-level chip design.

There are four types of possible transitions when dynamic charge distribution is considered over coupling capacitances as in Fig. 2-10. There are two parallel wires placed with minimum spacing. A type I transition occurs when one of the signals switches while the other stays unchanged such that the coupling capacitance is then charged up to  $k_1 C_x V$ , where the coefficient  $k_1$  is introduced as a reference for other types of transition. In a type II transition, one bus switches from low to high while the other switches from high to low. The effective capacitance will be larger than  $k_1$  by a factor of  $k_2$  the value of which is usually two. In a type III transition, both signals switch simultaneously and  $C_x$  will not be charged. However, because of possible misalignment of the two transitions, the amount of power consumption varies according to the dynamic characteristics by a factor of  $k_3$ . In a type IV transition, there is no dynamic charge distribution over coupling capacitance. Thus,  $k_4$  is set to zero.

There are some assumptions. First, synchronous latches are located at the transmitter side, thus all the transitions shall take place at the same time on the bus. The simultaneous transitions exclude type III transitions by setting  $k_3 = 0$ . It means that the achieved results are on the lower end of power saving. Second, statistics on the information source are not given in advance. Hence this scheme is suitable for data bus encoding, where it is difficult to extract accurate probabilistic information off-line. Enumeration method is employed to represent the coupling effect. If a bus line  $B_i$  is located between two other lines, a signal transition on  $B_i$  can trigger charge shifts on both coupling capacitances connected to  $B_{i-1}$  and  $B_{i+1}$ , respectively. In other words, at most two couplings can be initiated by a signal transition. Thus,  $2(N-1)$  bits are sufficient to represent the whole set of couplings in an  $N$ -bit bus per bus cycle. According to the types of correlated transition between neighboring buses, the coupling encoder generates a codeword as follows: 00 for a type III or IV transition, 01 for a type I transition, and 11 for a type

II transition. The reason 11 is assigned to a type II transition is that switching in different directions required changing the polarity of the charge stored in the coupling capacitance, hence, consuming about twice the amount of charge required for a type I transition. The codeword 11, instead of 10, helps to make a decision on data inversion using a majority voter, because the majority voter outputs high when at least eight input lines are high out of fifteen inputs. The majority voter can be implemented by using either full-adder circuitry or resistors and a voltage comparator. The control signal *inv* can be transmitted to the receiver using extra bus lines or extra transfer cycles. One problem of additional bus lines for control is the area overhead that may not be allowed due to physical constraints. In some cases, widening the space between signal bus lines can reduce the coupling effects more effectively than introducing extra control lines, because the coupling capacitance is inversely proportional to net space. Temporal redundancy is an alternative using extra clock cycles to transfer control signals.

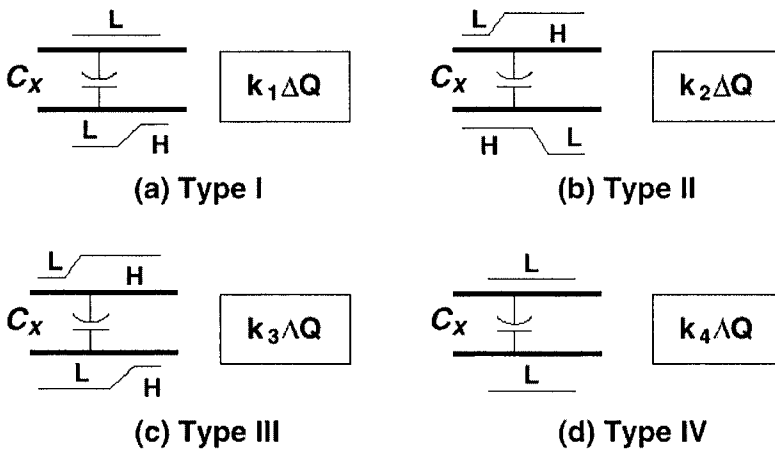


Figure 2-10. Transition types: (a) Single line switching; (b) both lines switching in opposite direction; (c) both lines switching in the same direction; (d) no switching.

## 2.4.2 Circuit techniques

One way to effectively increase noise immunity is to increase the switching threshold voltage  $V_{th}$  of the gate.  $V_{th}$  is defined as the input voltage at which the output changes state. Increasing the  $V_{th}$ , on the other hand, has an adverse effect on the performance such as speed and power consumption that are the prime features of dynamic circuits.

### 2.4.2.1 Gated-Vdd

Gated-Vdd is used to decrease the leakage power<sup>30</sup>. The key idea for gated-Vdd is to introduce an extra transistor in the supply voltage (Vdd) or the ground (Gnd) path. The extra transistor is turned on in the used section and off in the unused gated section. It maintains the performance and advantages of low power supply and threshold voltages while reducing leakage and leakage energy dissipation. The fundamental reason for the reduction in leakage is the stacking effect of self reverse-biasing series-connected transistors. However, it impacts the switching speed due to a non-zero voltage drop across the gated-Vdd transistor between the supply rails and the “virtual Gnd” for NMOS gated Vdd, Fig. 2-11, or the “virtual Vdd” for PMOS gated-Vdd.

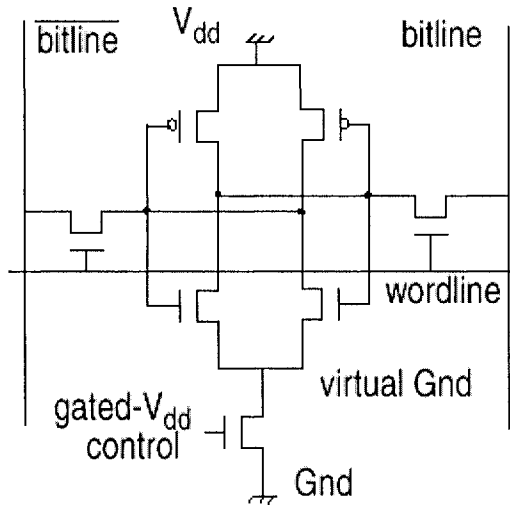


Figure 2-11. NMOS gated-vdd.

### 2.4.2.2 Dual threshold voltage

Dual threshold technique<sup>31</sup> is used to reduce leakage power by assigning high threshold voltage to some transistors in non-critical paths, and using low threshold transistors in critical paths. In order to achieve the best leakage power saving under target performance constraints, an algorithm is presented

for selecting and assigning an optimal high threshold voltage. Results show that dual threshold technique is good for power reduction.

#### 2.4.2.3 Dynamic threshold voltage

DTMOS (Dynamic Threshold MOS)<sup>32</sup> is a scheme that allows for a self-adjusting threshold voltage. By tying the gate to the body, the threshold voltage decreases as the gate voltage increases, and vice versa. In this manner, a higher zero-bias threshold can be used to reduce the leakage current. In a speed-adaptive threshold-voltage CMOS (SA-Vt CMOS) circuit<sup>33</sup>, the substrate bias is controlled so that delay in the circuit stays constant. Distributions of device speeds are squeezed under fast-operation conditions. With a ring oscillator using 0.25- $\mu$ m CMOS devices as a test circuit, it was found that the worst-case operating frequency was improved from 20 MHz to 55 MHz, and the fluctuation of the operating frequency was suppressed from 44 % to 15 %, while the supply-voltage variation was under 0.1 V with a 1.8 V supply voltage.

#### 2.4.2.4 C4 Flip-Chip

C4 Flip-Chip is used to manage the IR drop. IBM researchers developed C4 technology in the 1960s, Fig. 2-12. The bonding process is characterized by the soldering of silicon devices directly to a substrate (organic, for example). The chip faces the substrate, as opposed to wire bonding, hence the name flip-chip bonding. The salient features of this packaging methodology are as follows: 1) Solder bumps are distributed on metal terminals on the chip itself. These solder bumps are typically composed of 97% lead and 3% tin. The substrate has identically placed metal pads on its surface. 2) The chip is turned over and the metal pads are aligned to solder bumps; metal reflow is used to form connectivity between the substrate and chip.

The advantages of C4 technology are numerous and important, as follows:

- increased I/O density – C4 bumps may be placed over the entire area of the chip (called area array) rather than simply the periphery;
- self-aligning process step – due to surface tension;
- reduced die size for previously pad limited designs;
- reduced simultaneous switching noise due to smaller inductance of bumps compared to wire leads;
- better thermal properties as the backside of the wafer is now available for heat sinking;



- much better power distribution capabilities as circuits in the middle of the die can now access Vdd/Gnd directly;
- low cost and high throughput (all connections for one chip are made simultaneously in C4 as opposed to one-by-one in wirebonding);
- shorter wire lengths and fewer global wires ease wiring requirements.

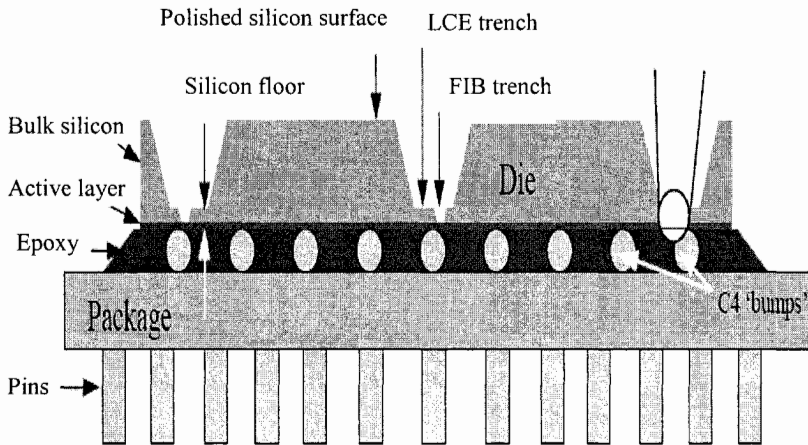


Figure 2-12. C4 Flip-Chip.

The main drawbacks to C4 at this time are that the use of lead in the solder bumps leads to the emission of alpha particles which can lead to circuit failure in sensitive circuits such as DRAMs. However, restricting the placement of solder bumps over these sensitive areas can minimize this effect. Research is ongoing to find alternate materials for solder bumps, as well. Also, the use of C4 packaging allows designers to do many different things in the floorplanning and routing stages of a design. Commercial tools for place-and-route, etc. are predicated on the use of peripheral wirebonding for I/O pads. New tools need to be in place for designers to take full advantage of flip-chip's advantages.

#### 2.4.2.5 Pseudo CMOS

Pseudo CMOS, Fig. 2-13 provides the logic capability of domino and the noise robustness of CMOS.

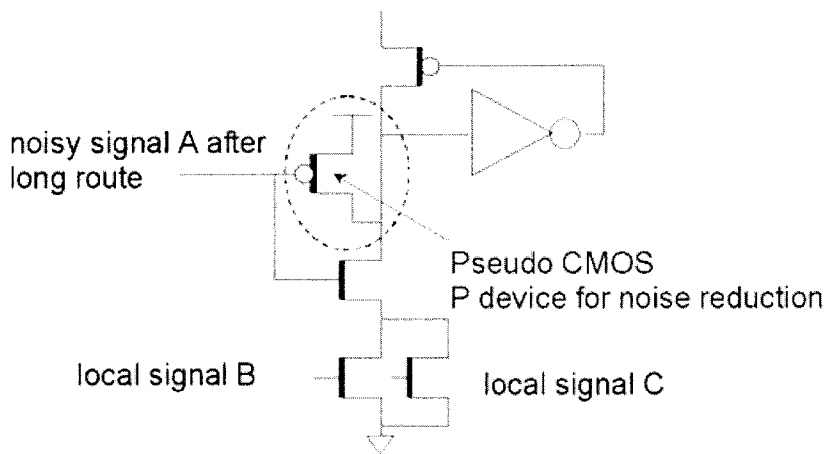


Figure 2-13. Pseudo CMOS.

#### 2.4.2.6 PMOS pull up technique

The PMOS pull up technique, Fig. 2-14, utilizes a pull-up device to increase the source potential of the NMOS network thereby increasing the transistor threshold voltage  $V_t$  and  $V_{st}$  during the evaluate phase<sup>34</sup>. This technique suffers from large static power dissipation.

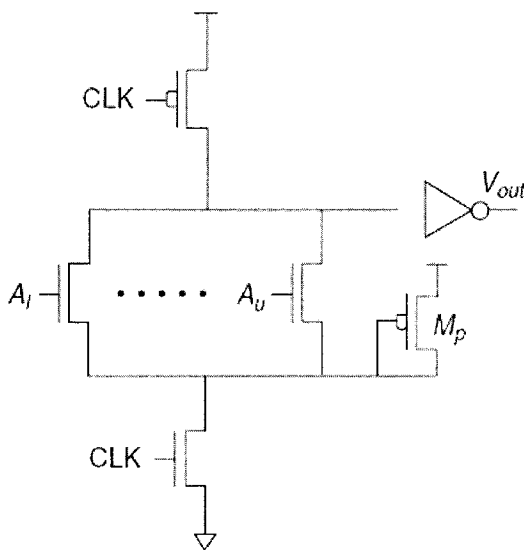


Figure 2-14. The PMOS pull up technique

### 2.4.2.7 CMOS inverter technique

The CMOS inverter technique utilizes a PMOS transistor for each input<sup>35</sup>, (Fig. 2-15), thereby adjusting  $V_{st}$  to equal that of a static circuit. This technique cannot be used for dynamic NOR-type circuits, as certain logic combinations will short  $V_{dd}$  to GND.

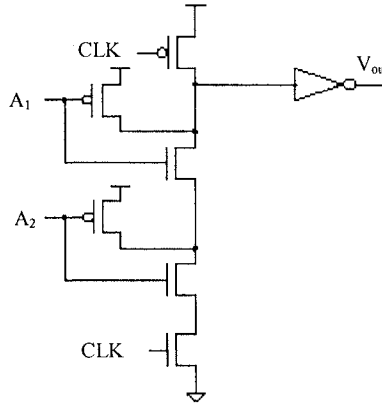


Figure 2-15. The CMOS inverter technique.

### 2.4.2.8 The Mirror technique

The mirror technique, Fig. 2-16, utilizes two identical NMOS evaluation networks and one additional NMOS transistor  $M_I$  to pull up the source node of the upper NMOS network to  $V_{dd} - V_t$  during the precharge phase<sup>36</sup> thereby increasing  $V_{st}$ . The mirror technique guarantees zero DC power dissipation, but a speed penalty is incurred if the transistors are not resized.

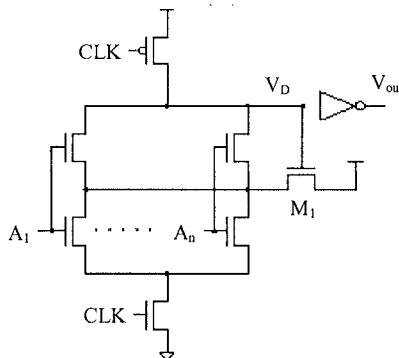


Figure 2-16. The mirror technique<sup>36</sup>

### 2.4.2.9 The twin-transistor

The twin-transistor technique, Fig. 2-17, utilizes an extra transistor for every transistor in the pull-down network in order to pull up the source potential<sup>37,38</sup>. The twin transistor technique consumes no DC power.

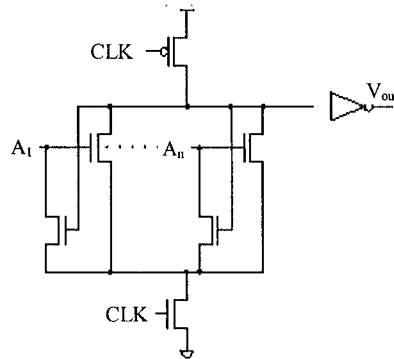


Figure 2-17. The twin transistor technique.

### 2.4.3 Architectural techniques

A high level description of a modified scheme for powering up/down resources is presented<sup>39</sup>. The scheme presented reduces the instantaneous current drawn from the supply when the resource is turned on and off and can be applied at different levels of the design abstraction. It is based on dividing the available resources in the system into smaller parts and then switching each part individually on and off at separate times instead of doing it instantaneously. This time separation between the on and off switching of the parts results in reduced sudden current pulses delivered from the supply and, hence, reduces the glitches appearing on the power and ground lines. A block diagram of the modified clock gating technique where the resource is divided into four parts is shown in Fig. 2-18. The clock signal is fed to each part through a separate AND gate that is controlled by an enable signal that is delayed with respect to the enable signal used for the previous resource. Another technique that is used to reduce the effect of the instantaneous current pulses is the decoupling capacitance technique. Decoupling capacitors have been effectively used to reduce  $dI/dt$  noise on printed circuit boards. This technique has become available on-chip to reduce the effect of inductive noise on the supply rails<sup>40</sup>.

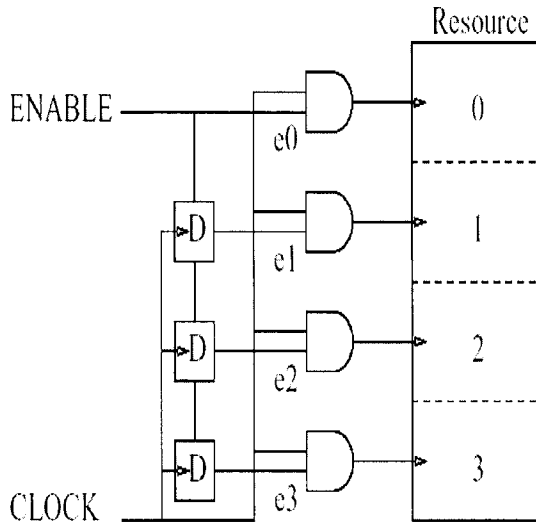


Figure 2-18. Using an enable signal to reduce inductive noise.

## 2.5 NOISE ANALYSIS ALGORITHMS

A specific level of noise is unavoidable in digital circuits. The question is to decide when it causes function failure. Unity gain is a criterion to decide when a circuit is considered unstable

### 2.5.1 Small signal unity gain failure criteria

Traditional analysis of noise margins relied on the small signal unity gain failure criteria<sup>9</sup>. For a small change in input noise to a circuit biased at an operating point, the resultant change in output noise is measured, Fig. 2-19. If  $|d(\text{Output})/d(\text{Input})| > 1$  then the circuit is considered unstable. Unity gain is a good design metric but is neither necessary nor sufficient for noise immunity.

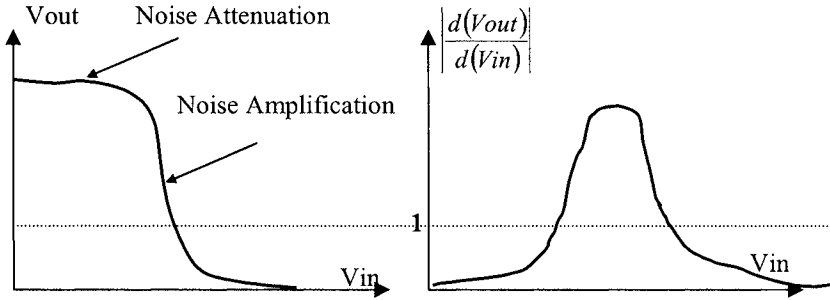


Figure 2-19. DC transfer function of an inverter illustrating small signal unity gain.

Most aggressively designed paths have some noise-sensitive stages interspersed with quiet stages. We need to allow some noise amplification in the sensitive stage knowing that the quiet stages will finally attenuate it.

### 2.5.2 Case study: Intel failure criteria

In this section, we list the steps and guidelines followed by Intel in determining a circuit failure.

- Break the circuit into circuit stages.
- Track the noise propagation across these stages by AC circuit simulation.
- Measure if any circuit stage failed due to
  - Injected noise combined with
  - Noise propagated from previous stages
- Noise can propagate across any number of stages eliminating the need for any unity gain budgeting.
- Combination of noise sources and simultaneous noise on multiple inputs should be considered.
- The peak noise in the event of two simultaneous couplers on a line is larger than the sum of these two events.
- The simultaneous occurrence of different parallel inputs has to be considered.
- New Transistor level (symbolic circuit) simulation should be found, since SPICE is very slow.
- Solving the differential equation symbolically in a piecewise linear manner can decrease the CPU time needed with good accuracy.

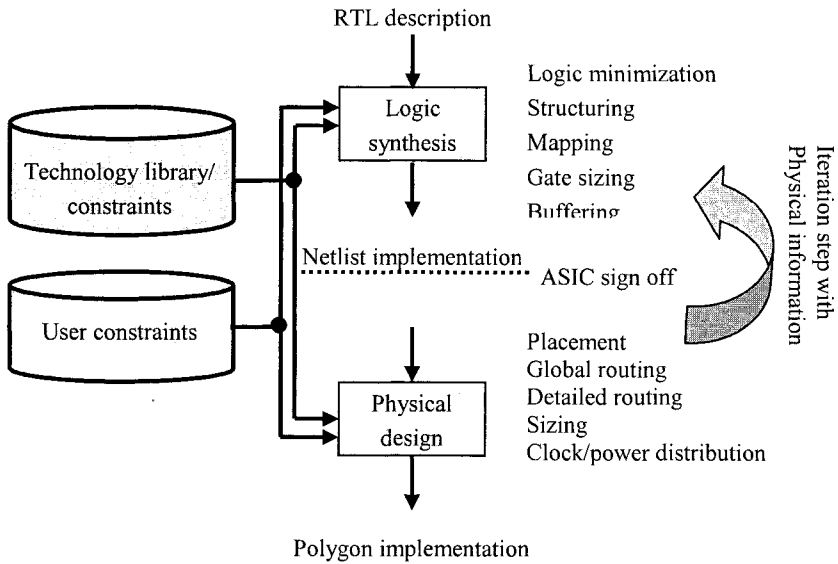


Figure 2-20. Traditional ASIC design flow.

The traditional design flow in Fig. 2-20 contains a separation between the logic synthesis step and the physical design step. For designs with aggressive performance goals, it was found that several iterations between synthesis and physical design are required to converge to a desired implementation<sup>39</sup>.

As a result, design teams have begun to bring more of the backend design flow in-house, and the handoff to the semiconductor-vendor occurs only at the end. This approach is shown in Fig. 2-21 and is known as the customer-owned tooling (COT) approach.

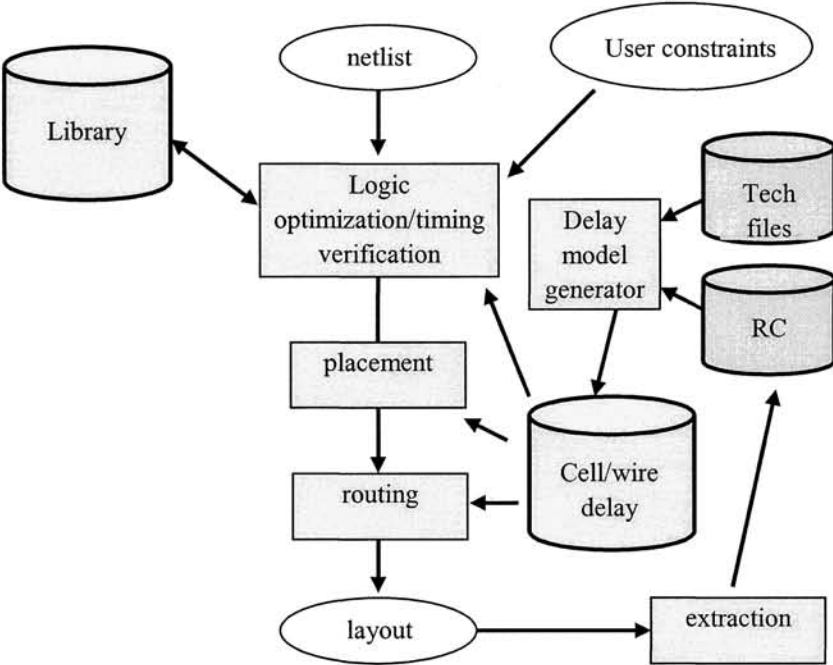


Figure 2-21. Today's high performance logical/physical flow.





<http://www.springer.com/978-0-387-25870-6>

Interconnect Noise Optimization in Nanometer  
Technologies

Elgamel, M.; Bayoumi, M.

2006, XIX, 137 p., Hardcover

ISBN: 978-0-387-25870-6