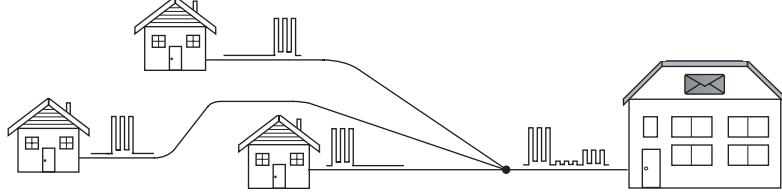


## Introduction

For long-haul and ultra-high-speed data communication, fiber-optical networks with optical amplifiers have become the main technology and do not require receivers with highest sensitivity [1,2]. The growing demand on broadband Internet access, however, has motivated development of low-cost, high-sensitivity optical receivers with a wide dynamic range for the optical input power. The gap of transmission bandwidth at the “last mile” can be closed by fibers-to-the-home (FTTH) at medium data rates. Figure 1.1 shows the principle of a passive optical network. The three homes in the example are connected to the post office on the right-hand side via a passive optical star coupler. The homes are sending in time-division multiplex access (TDMA) in a well-defined order. Due to the different distances between the homes and the receiver in the post office the attenuation is different and therefore the received signals are in a wide optical power range. A burst-mode receiver is necessary to handle the incoming signals.

Bipolar, CMOS, BiCMOS, and SiGe receivers are compared in this book. Therefore also the technologies are compared concerning noise, and receivers in these technologies are presented and compared. Bipolar transistors are faster than CMOS transistors with the same structure size and have the advantage of higher transconductance. The matching of bipolar transistors is also better than that of MOSFETs.

CMOS technologies have the advantage that they are faster on the market than bipolar or BiCMOS technologies. Especially BiCMOS technologies with the same minimum structure as CMOS technologies are normally available a few years later and are more expensive than CMOS processes of the same structure size. However, analog circuits in a 120 nm CMOS process can be realized with a similar or equal performance as in a sub-micron bipolar or BiCMOS process (e.g., 0.6 or 0.35  $\mu\text{m}$ ). If systems-on-chip including large digital parts with a large number of transistors are needed, deep-sub-micron CMOS, however, is an advantage compared to sub-micron BiCMOS technologies, because the chip area for the digital part is much less in deep-sub-micron



**Fig. 1.1.** Example configuration for a passive optical network

CMOS. It has to be mentioned, however, that for low volumes of ICs or ASICs deep-sub-micron CMOS circuits are much more expensive than sub-micron BiCMOS chips due to the large difference of mask costs.

Due to increasing doping levels of wells, channels, and substrate in down-scaling technologies, the width of the space-charge region is reduced. Also the electric field strength increases and therefore low supply voltages are necessary to stay below the breakdown field strength. These low supply voltages are the reason why classical methods of circuit design, e.g., the classical cascode circuit are no longer useable.

The low-noise optical receivers presented in this book are designed in standard digital 180 nm CMOS as well as 120 nm CMOS technology to show the low-noise capability of deep-sub-micron CMOS for high photodiode capacitance. The reason for choosing deep-sub-micron CMOS technology was the possibility to easily integrate a signal-processing digital part. The signal does not leave the chip after the optical receiver and therefore output drivers and output impedance matching can be saved in systems-on-a-chip (SoCs). Packaging costs and influences of parasitic elements, e.g., from electrostatic discharge (ESD)-structures, bond-pads and bond wires are avoided in SoCs.

To detect the infrared light of  $\lambda = 1.3 \mu\text{m}$ , an external quaternary photodiode is necessary. This external photodiode causes a high input-node capacitance. The transimpedance amplifiers (TIA) in deep-sub-micron CMOS presented in this work, nevertheless, show a high sensitivity and a wide input-current range. To avoid overdrive, the transimpedance has to be variable. Therefore, usually switching of the compensation capacitance is necessary to guarantee stability. The parasitic capacitances of the MOSFET switches, however, reduce the data rate and sensitivity in these designs. Another solution for this problem is suggested here. Reducing the open-loop gain of the amplifier in order to achieve stability instead of switching the feedback capacitance enables a high dynamic optical input power range and high data rates.

The focus of this work is on the development of the preamplifier of the optical deep-sub-micron CMOS receiver. This is normally a TIA and due to the fact that there is no digital part integrated in the test-chips introduced here the biasing voltages are generated externally. Furthermore, a  $50 \Omega$  driver is implemented to drive the measurement system. In the final design the optical receiver front-end is followed by a main amplifier and the digital part and therefore the circuit for characterization is not necessary in the final system.

Fundamentals of network access and the difference between continuous-mode and burst-mode communication are discussed in Chap. 2. Furthermore the components of the optical receiver front-end are summarized. Photodetectors are described in Sect. 3. An overview of the basic knowledge about transimpedance and main and limiting amplifiers is given in Sect. 4.

In Chap. 5 a short overview of the used deep-sub-micron CMOS processes is presented. The disadvantages and the challenge of using a standard digital technology for an analog design is pointed out.

Chapter 6 processes the circuit theory of the transimpedance amplifier (TIA) with a section about stability. Chapter 7 introduces bit-error rate and sensitivity and in the following the noise theory of transistors on the one hand and TIAs on the other. First the circuit of an ideal TIA is analyzed and after this a real TIA is examined more closely. The noise theory first describes the main parameters having influence on the sensitivity, the bit-error ratio, the power penalty and the noise of the input circuit. The noise model of field-effect transistors is summarized and the noise of the input circuit is calculated for a TIA with an ideal, but noisy amplifier and for TIAs with two different CMOS input stages realized during this work.

Before our own designs are presented, an overview of the state of the art in bipolar, CMOS, BiCMOS, and SiGe optical receivers is given in Chap. 8. It includes highly sensitive optical continuous-mode receivers as well as real burst-mode receivers.

The developed designs are presented in the last chapter. First, the design environment and the measurement setup are discussed and the schematics as well as layout plots and measured results are presented. At the end of the chapter a conclusion and a comparison of our own designs with the state of the art is given.

The sensitivities achieved in 120 nm CMOS with various designs are  $-31.4$  dBm at  $622 \text{ Mb s}^{-1}$ ,  $-28.6$  dBm at  $1.25 \text{ Gb s}^{-1}$ , and  $-20.4$  dBm at  $2.5 \text{ Gb s}^{-1}$ , respectively. The minimum achieved switching time between minimum and maximum optical input power for burst-mode application is  $1.7 \text{ ns}$ . The maximum optical input power range is  $27 \text{ dB}$  at  $1.25 \text{ Gb s}^{-1}$  which is more than the dynamic range presented in the literature [3–6] with  $21 \text{ dB}$ . These  $21 \text{ dB}$  optical input power ranges mean that for a typical attenuation of a silica glass single-mode fiber of  $0.4 \text{ dB km}^{-1}$  at the used wavelength of  $1.3 \mu\text{m}$  [7] the developed receivers are able to handle homes with distances varying by about  $50 \text{ km}$ , assuming no additional losses and dispersion.

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