

Preface

The integrated circuit with each new generation has been characterized by increasing functionality. In the 1980's Very Large Scale Integrated Circuits (VLSIC) began to emerge with transistor counts approaching one million plus per chip! The IC package quickly became more than a "chip carrier". Now the packaging had to address the electrical, mechanical and thermal requirements of the IC, and had to do so cost-effectively. A package costing more than the chip was not an option. In addition, the demands of the marketplace for product that was "smaller, better and cheaper" came into play.

As a result the late '80s saw paradigm shifts in IC packages and packaging options. Area array packages, in particular, the Ball Grid Array (BGA) began to emerge that more effectively addressed increasing chip I/O count. Ceramic packaging for high performance circuits (microprocessors digital signal processors) gave way to organic based packages, the plastic BGA (PBGA), offering a more favorable solution to package cost. And the hybrid circuit suddenly became a multichip module!

Over the past 15 years the author has developed and presented professional development courses at various technical symposia as well as on-site at semiconductor, component and equipment manufacturers and materials suppliers facilities. The courses have covered topics that make up the electronic manufacturing arena focusing on packaging and assembly of the integrated circuit.

This book evolved from these courses and discusses the many changes that have taken place not only with the physical package itself but also the currently available packaging options and assembly technologies. It is intended to serve as an *introduction* to IC packaging and assembly providing sufficient coverage to afford a working knowledge of the basic concepts and technologies. The book is intended for personnel new to the industry and, those indirectly involved in electronics manufacturing such as upper management, quality assurance, procurement, marketing and sales, and equipment manufacturers and material suppliers. For those directly involved the book can serve as a useful *overview* of new and emerging technologies.

The First Chapter is discussion of electronic manufacturing that basically describes the packaging and assembly of the integrated circuit. It identifies the various levels of microelectronic assembly, i.e., Level 1.0 interconnects – chip to package and Level 2.0 – chip or package to a substrate board and the packaging options, – single chip, multichip and chip on board.

The Second Chapter briefly reviews the integrated circuit manufacturing process and the *applicability* of much of the procedures and practices to IC packaging and assembly. It highlights the significance of a cleanroom operating environment and the photolithographic process in particular, as a model for implementing a proven high yield cost effective manufacturing technology.

Subsequent Chapters 3 and 4, discuss the trends in the IC package, the Chip Scale Package, and Wafer Level Packaging. Chapter 5 covers Multichip Packaging and the various sub-classifications – the hybrid circuit, the multichip module, System

in Package, System on Packaging and the rapidly developing 3-D Packaging that includes stacking of both multiple die and packages.

Working with bare die as opposed to package devices is discussed in Chapter 6 and covers the subject of Known Good Die or KGD. It presents the concerns associated with bare die and multichip applications and the problem related to the lack of sufficient electrical testing of unpackaged die to insure the device meeting full electrical specifications. Various approaches to resolving this problem and providing for Known Good Die are discussed.

The assembly of a bare die onto an organic board, Chip on Board (COB) is covered in Chapter 7. Implementation and incorporation into Surface Mount Assembly lines and concerns are included. A “packageless packaging” approach makes it a viable packaging option offering both increased component density and an enhanced reliability at the Level 2.0 printed circuit board (PCB) assembly.

The Level 1.0 interconnect technologies are covered in subsequent chapters, C&W Assembly in Chapter 8, TAB in Chapter 9, and Flip Chip Bumping and Assembly, Chapter 10 and 11 respectively.

The last four chapters, 12 through 15, cover the manufacturing technologies, namely Thin Film, Thick Film, Cofired Ceramic and the Organic Laminate Technology, for packages – SCP and MCP, and High Density Interconnect (HDI) substrates. The Thin Film process technology is highlighted as the leading technology in meeting the challenges that arise with the packaging and assembly of current and future integrated circuits. It basically emulates the IC manufacturing and therefore has the inherent capability for achieving very fine line conductor circuitry and the high wiring density required for high density interconnects supporting Levels 1.0 and 2.0. The application of the Thin Film Technology to Thick Film, Cofired and Laminate, to further enhance the overall advantages of each is also discussed. Chapter 15 presents a discussion of a combined Thin Film and Laminate process (Build Up Technology, BUT) as a key enabler for Level 2.0 interconnect substrates that adequately accommodates all current and future IC packaging and assembly technologies.



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