
Preface

With dramatic increases in on-chip packing densities, routing congestion has become a major problem in integrated circuit design, impacting convergence, performance, and yield, and complicating the synthesis of critical interconnects. The problem is especially acute as interconnects are becoming the performance bottleneck in modern integrated circuits. Even with more than 30% of white space, some of the design blocks in modern microprocessor and ASIC designs cannot be routed successfully. Moreover, this problem is likely to worsen considerably in the coming years due to design size and technology scaling.

There is an inherent tradeoff between choosing a minimum delay path for interconnect nets, and the need to detour the routes to avoid “traffic jams”; congestion management involves intelligent allocation of the available interconnect resources, up-front planning of the wire routes for even distributions, and transformations that make the physical synthesis flow congestion-aware. The book explores this tradeoff that lies at the heart of all congestion management, in seeking to address the key question: how does one optimize the traditional design goals such as the delay or the area of a circuit, while still ensuring that the circuit remains routable? It begins by motivating the congestion problem, explaining why this problem is important and how it will trend. It then progresses with comprehensive discussions of the techniques available for estimating and optimizing congestion at various stages in the design flow.

This text is aimed at the graduate level student or engineer interested in understanding the root causes of routing congestion, the techniques available for alleviating its impact, and a critical analysis of the effectiveness of these techniques. The scope of the work includes metrics and optimization techniques for congestion at various stages of the VLSI design flow, including the architectural level, the logic synthesis and technology mapping level, the placement phase, and the routing step. This broad coverage is accompanied by a critical discussion of the pros and cons of the different ways in which one

can minimize the ill-effects of congestion. At the same time, the book attempts to highlight further research directions in this area that appear promising.

Although this book is not meant to be an introductory text to VLSI CAD, we have tried to make it self-contained by providing brief primers that go over the classical techniques in routing, placement, technology mapping and logic synthesis, before diving into discussions on how these techniques may be modified to mitigate congestion. Our coverage focuses on congestion issues dealing primarily with standard cell based designs. In particular, the models and optimization methods that pertain specifically to field-programmable gate arrays (FPGAs) have not been explicitly addressed in this book.

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Prashant Saxena
Rupesh S. Shelar
Sachin S. Sapatnekar

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Saxena, P.; Shelar, R.S.; Sapatnekar, S.

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