
Preface

Research in placement algorithms for VLSI circuits has enjoyed a renaissance in recent years. Today, there are a number of high quality academic placers that have been developed in universities. The amount of research on this topic clearly reflects the importance of the placement as the single most critical component for achieving timing/design closure in a modern physical synthesis tool. Placement algorithm itself has been researched for more than three decades. Yet, the problem is still very challenging for multiple reasons. First, the exponential increase of the circuit density according to Moore's Law has led to designs with tens of millions of placeable objects today. Although such complex designs are composed hierarchically based on the logic or function hierarchy, multiple studies (e.g. [3]) show that placement based on the logic hierarchy may lead to considerably inferior results. The preferred methodology is to place the entire design flat (with millions or tens of millions of placeable objects) to derive a good physical hierarchy and then use it to guide the subsequent physical synthesis process. Therefore, the modern placers have to handle extremely large problem sizes. Second, today's System-on-Chip (SoC) designs introduce complex constraints, such as routability and timing constraints, as well as the support of mixed size macros, area I/Os, multi-Vt and multi-Vdd islands for power optimization. Moreover, recent work on placement optimality studies ([1,2]) suggest that there exists significant room for improvement even for wire length optimization alone (details will be discussed in Chap. 2). All these reasons stimulated renewed interests in research in circuit placement problems, both in academia and industry, in the past a few years.

To help further stimulate advances in placement research, ISPD (International Symposium on Physical Design [7]) hosted two placement contests using new, large-scale benchmark suites based on real industrial designs ([5,6], see Chap.1 for more detailed discussion). The common goals of the two ISPD placement contests were:

- To provide new modern placement benchmarks to stimulate new development in placement research

- To provide a common basis for quantitative measurements of contemporary placement algorithms, and help the academic community to publicize their placement tools and results
- To provide an educational forum on a variety of state-of-art placement algorithms for future placement researchers

These two placement contests were huge success with participation from a number of academic placers and provided a common platform to evaluate various placement algorithms on the same set of realistic benchmarks. This book is the product of these academic efforts on placement contests and it can be considered as the year 2006 snapshot of state-of-the-art modern placement techniques employed in the field. The book provides in-depth description of the best practices of placement algorithms used in the research community today. Each book chapter provides detailed description of the underlying algorithm and implementation features of a placement tool that participated in the two contests, including the experimental results on ISPD placement benchmark circuits and the optimality analysis on PEKO-MS benchmarks.

This book is organized in four parts:

- Part I introduces placement benchmark suites. In Chap. 1, new industry design-driven ISPD 2005/2006 benchmark circuits are presented with contest results. Chapter 2 describes the details of PEKO-MS benchmarks that can be used for placement optimality analysis.
- Part II describes flat placement techniques, which formulate and solve the entire placement problem directly (although the numerical solvers used in these placers may use multilevel methods). Chapter 3 describes the most recent analytical placer DPlace that is an anchor cell-based quadratic placement engine. The Kraftwerk placement algorithm, the winner of ISPD 2006 placement contest, is presented in Chap. 4.
- Part III presents top-down partitioning-based placement techniques. It includes Capo, a congestion driven placer (Chap. 5) and the Dragon placer that combines simulated annealing optimization with a partitioning algorithm (Chap. 6).
- Part IV is about multilevel placement methods that have attracted significant attentions recently. It covers APlace (Chap. 7), which was the winner of the 2005 placement contest, the runtime efficient force-directed placer, FastPlace (Chap. 8), the mFAR fixed-point addition based placer (Chap. 9), and the multilevel non-linear optimization placer mPL (Chap. 10) that produced the highest quality solutions in the 2006 placement contest. Also, NTUplace3 (Chap. 11), a new analytical placer for large scale mixed-size designs, is presented here.

The idea of this book emerged in April 2006, right after the ISPD 2006 placement contest, as a way of capturing a technology snapshot of dominant placement algorithms. We sent out invitations to all placement contest participants, and every team agreed to contribute to this book. By February 2007, all chapter manuscripts were submitted. In fact, some of them included the latest progress they made after the 2006 placement contest. Therefore, the results reported in some of the chapters

are different (better) from the original placement contest results, which we provided at the end of Chap. 1 for reference.

The editors are well aware of the limitations of placement objectives used in the two contests. The 2005 contest uses wire length minimization as its sole objective function, while the 2006 contest uses a combination of wire length minimization, cell density control and runtime as its objective function (see Chap. 1 for more details). Real placement problems need to consider a number of other objectives, such as timing, power, and thermal optimization, as well as interaction with various physical synthesis operations, such as buffer insertion and gate sizing. A direct comparison of different placers under all these objectives and constraints may not be possible or meaningful, as each design has its own emphasis, and the final result is not determined by the placement algorithm alone. Many other steps, such as timing analysis, global and detailed routing, and various physical optimization operations can affect the final result. Therefore, we think that it is appropriate to use rather simple metrics in the two placement contests to measure the capability of the core wire length optimization engines employed in the different placers. As pointed in [4], a placer with good wire length minimization engine can be extended to handle other design objectives through weighted wire length minimization using various weighting functions.

This book is intended for graduate students, researchers, and CAD tool developers in the physical synthesis and physical design area. Each chapter is mostly self-contained and can be read independently. We hope that the readers can benefit from this collection of modern placement algorithms and potentially contribute to the field with new perspective. Please note this book is not intended to provide a comprehensive review of all available placement techniques, but to highlight the most successful techniques and practices used in modern placers. We refer the reader to [4] for a more comprehensive survey for the existing placement techniques.

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