Preface

"Engineering is the profession in which a knowledge of the mathematical and natural sciences gained by study, experience, and practice is applied with judgment to develop ways to utilize, economically, the materials and forces of nature for the benefit of mankind" —Engineers Council for Professional Development (1961/1979)

Functional verification has become an important aspect of the IC (Integrated Chip) design process. Significant resources, both in industry and academia, are devoted to bridge the gap between design complexity and verification efforts. SAT-based verification techniques have attracted both industry and academia equally. This book discusses in detail several latest and interesting SAT-based techniques that have been shown to be scalable in an industry context. Unlike other books on formal methods that emphasize theoretical aspects with dense mathematical notation, this book provides algorithmic and engineering insights into devising scalable approaches for an effective and robust realization of verification solution. We also describe specific strengths of the various approaches in regards to their applicability. This books nicely complements other excellent books on introductory or advanced formal verification primarily in two aspects:

First, with growing interest in SAT-based approaches for formal verification, this book attempts to bring various emerging SAT-based scalable verification techniques and trends under one hood. In the last few years, several new SAT-based techniques have emerged. Not all of these are covered by other books: Hybrid SAT Solver, Efficient Problem Representation, Customized SAT-based Bounded Model Checking, Verification using Efficient Memory Modeling, Distributed SAT and SAT-Bounded

Model Checking, Proof-based Iterative Abstraction, High-level Bounded Model Checking, SAT-based Unbounded Model Checking, and Synthesis for Verification Paradigm.

Second, and more importantly, due to the practical significance of these techniques, they are appropriate for direct implementation in industry settings. In this book, we describe how these techniques have been architected into a verification platform called *VeriSol* (formerly *DiVer*) which has been used successfully in the industry for the last four years. We also share our practical experiences and insights in verifying large industry designs using this platform.

We strongly believe that the techniques described in this book will continue to gain importance in the verification area, given that the verification complexity is growing at an alarming rate with the design complexity. We also believe that that this book will provide useful information about foundation work for future verification technologies.

The book expects the reader to have a basic understanding of formal verification, model checking and issues inherent in model checking. The book primarily targets researchers, scientists and verification engineers who would like to get an in-depth understanding of scalable SAT-based verification techniques that can be further improved. The book also targets CAD tool developers who would like to incorporate various SAT-based advanced techniques in their products. Currently, colleges do not emphasize adequately the algorithmic and engineering aspects of designing a verification tool. Such practices should be encouraged, as a good infrastructure is required to produce quality research. We strongly believe that this book will motivate such activities in the future.

Here is the outline of the book: With an introduction and background on current design verification challenges for model checking techniques in Chapters 1 and 2 respectively, we divide the rest of the book into five parts, each with 1-4 chapters. Part I describes the underlying infrastructure — efficient problem representation and SAT-solvers — to realize scalable verification algorithms. Parts II-IV describe SAT-based model checking algorithms for various verification tasks such as accelerated falsification, robust proof methods, and iterative abstraction/refinement, respectively. Part V gives detail of an industry tool *VeriSol* and several industry cases studies. It also covers future trends in SAT-based model checking such as, synthesis for verification paradigm, and high-level model checkers, to further improve the scalability.

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