



Figure A-10 Spacing rule overhead of sleep transistor with well-tapped standard cells

To reduce effect of the spacing overhead on the area efficiency, we can increase the size of the sleep transistor so as to reduce the ratio of the spacing overhead over the sleep transistor. This means that the horizontal size of the sleep transistor needs to be large enough to mitigate the effect of the spacing overhead at both sides of the cell and W should be large enough to avoid multiple rows so as to eliminate the diffusion spacing overhead. If the standard cell library is designed without individual well tap in a cell (tap-less cells), then the well spacing rule becomes not applicable to the normal body biased sleep transistor because the sleep transistor and standard cell share well taps and are biased at same voltage (permanent V_{dd}). Consequently, the boundary are overhead is only caused by the diffusion spacing rule.

It is worth noting that I_{on} linearly increases with W as shown by the dashed line in Figure A-8 on page 257. Consequently, I_{on}/W becomes constant at given L and V_{bb} which means that the area efficiency is mainly determined by the layout implementation of the sleep transistor once L and V_{bb} are defined.

<http://www.springer.com/978-0-387-71818-7>

Low Power Methodology Manual

For System-on-Chip Design

Flynn, D.; Aitken, R.; Gibbons, A.; Shi, K.

2007, XVI, 300 p., Hardcover

ISBN: 978-0-387-71818-7