

this reason we recommend placing the level shifters in the destination domain, as shown in Figure 3-3 and Figure 3-5.

As part of defining a level shifter strategy, the designer specifies rules for when level shifters are inserted. The designer can specify explicitly which blocks require level shifters, or the designer can specify a minimum voltage difference that requires level shifter insertion.

High-to-low level shifters should be inserted based on timing considerations. Using standard gates rather than level shifters at the interface of two different voltage regions causes an error in delay calculation, as mentioned above. If the voltage difference between the two domains is large enough then this timing error becomes unacceptable. In this case, level shifters are required. The exact voltage difference then depends on the library and the design objectives.

Low-to-high level shifters should be inserted based on power as well as timing considerations. If the voltage difference between two domains is large enough, the input stage of a standard gate in the higher domain will not turn all the way off, leading to excessive crowbar current.

Specifically, if the voltage difference is larger than the threshold voltage of the receiving PMOS transistor, the transistor will not completely turn off. In order to provide a reasonable noise margin, we should pad this number by 10% of the VDDH (the higher supply voltage). Thus, if

$$VDDH - VDDL > V_{TPMOS} - (0.1 * VDDH)$$

Then a level shifter should be used in order to shut off the receiving PMOS input transistor stage.

(Here V_{TPMOS} is the threshold voltage of the PMOS transistor, and VDDH and VDDL are the VDD supplies for the higher and lower domains respectively).

3.2.6 Level Shifter Recommendations and Pitfalls

Recommendations:

- Place the level shifters in the receiving domain – in the lower domain for High-to-Low shifters, in the higher domain for Low-to-High shifters.
- Low-to-High level shifters have significant delays that need to be understood and thoughtfully factored into RTL design partitioning for timing critical blocks.
- Ensure there is a defined relationship between different voltage domains such that the operating conditions make it clear whether an up- or down-shifter is required.

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