

In many applications, the power acknowledge signal is asynchronous – its timing depends on the switching fabric design. For this reason, the power controller needs to synchronize the acknowledge to its own clock before using it.

### 5.4.3 Recommendations and Pitfalls for power gating controllers

Recommendations:

- Design the control sequencers with request and acknowledge handshakes for the power gating control.
- Build in interlocks and synchronization to ensure a safe wake-up sequence.

Pitfalls:

- One critical case is when the controller tries to power the block up immediately after power down, and when in fact the power down is not complete. That is, the power up sequence starts while the power gating fabric is only partially powered down. Designers need to consider this case carefully in designing the power controller. Remember that the power down time is dependent on semiconductor process and temperature.

## 5.5 Power gating design verification – RTL simulation

We next consider the issue of verifying a power gated circuit at the RTL level. This is a challenge because Hardware Description Languages (HDLs) do not provide a mechanism for describing power connections at the RTL level. To simulate power gating we need to extend Verilog – either by modifying the code or by using a separate set of commands to describe power connections and power switching.

The Unified Power Format (UPF) defines both a language format and simulation semantics for power gating. Much of the UPF standard addresses the implementation of power strategies; this aspect is discussed in Chapter 11: Implementing Power Gating. Here we will limit our discussion the issue of simulating power gating.

EDA companies are moving rapidly to implement UPF and to provide the ability to simulate power gating automatically. For those who are using simulators that do not yet support UPF, it is possible to implement much of the UPF simulation semantics by adding special code to the RTL, either manually or by means of a script.

(Note: The script-based approach we describe here assumes a rigorous RTL coding style, such as that described in the *Reuse Methodology Manual*. It also depends on using a consistent naming scheme for clocks and resets.)

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