

The power controller for partial retention must therefore drive independent (named) resets to the appropriate portions of the subsystem. Some rigorous functional testing is required to ensure that there are no illegal combinations of states that might cause deadlock.

5.3.5 System Level Issues and Retention

A more subtle complication arises from a potential interaction with clock gating, which is implemented further down the design flow. All the state bits that make up the enable terms for clock gating need to be carefully managed: either retained or be re-initialized to a safe and restart-able condition. In this way, the contents of the transparent latch in the clock gating cells can cleanly be regenerated – without the requirement to add retention to the clock gating cells.

Similarly, using both edges of the clock can be a real problem. In the power down sequence, the clock is stopped in the “0” state. This leaves the clock gating latch transparent; when power and state are restored, the terms that form the clock gating control propagate through the latch, restoring the correct value to the inputs of the clock gated registers.

If both positive-edge-clocked flops and negative-edge-clocked flops are used in the same design, then there is no value that we can park the clock that will leave all the clock gating latches transparent. Thus, we will not be able to restore all the data correctly.

Retention also makes scan testing somewhat more complicated. In order to perform scan testing, we need to force the retention flops into their normal operating mode. Thus, when we enter scan mode (for the power gated block) we need to set the power controller so that save and restore are both de-asserted. When we enter scan mode for the power controller itself, we need to relax this constraint, so that scan can be used to test the generation of the save and restore signals.

5.3.6 Recommendations and Pitfalls for state retention

Recommendations:

- If partial retention is implemented then provide separate resets for the retained and the non-retained storage portions of the design. This allows clean verification of power on reset and restore/re-initialize operation.

<http://www.springer.com/978-0-387-71818-7>

Low Power Methodology Manual

For System-on-Chip Design

Flynn, D.; Aitken, R.; Gibbons, A.; Shi, K.

2007, XVI, 300 p., Hardcover

ISBN: 978-0-387-71818-7