

Chapter 2

Packaging Architecture and Assembly Technology

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Chapter 1 reviewed the variety of solder alloys and the general properties and behavior of these materials in relation to their role in electronic product life. We now investigate in more detail the architecture of electronic hardware. This will help us to understand the important role of solder alloys in product reliability. Clearly, the transition to lead-free soldering presents several challenges in structure and processes. Lead finishes, elements of the BGA and other emerging area-array technologies must change and yet remain compatible with processes. Changes in solder paste and flux must also be evaluated. We begin our discussion with the structural elements of packages that are most closely related to the solder joint.

2.1 Packaging Architectures

In general, an electronic product can be considered as an interconnection hierarchy, from the basic semiconductor to the printed wiring assemblies that make up the functional circuits of a product. As discussed in Chapter 1, various types of assemblies can be created and technology is making possible increased performance and functionality in ever-smaller product volumes. Packaging architectures range from leaded devices assembled to printed wiring boards by wave-soldering technology to ball-grid arrays and chip-scale devices assembled by surface-mount processes. Flip chips, in which semiconductors are assembled directly on the boards with no external packaging, are rapidly moving from a specialized form of packaging to high-volume packages as the market demands. Recalling Figure 1.1, we begin our discussion of leaded devices.

2.1.1 Leaded Semiconductor Packages

The many leaded package styles (Pecht, 1994) can be categorized into through-hole or surface-mount types. In either case, high manufacturing volumes employ

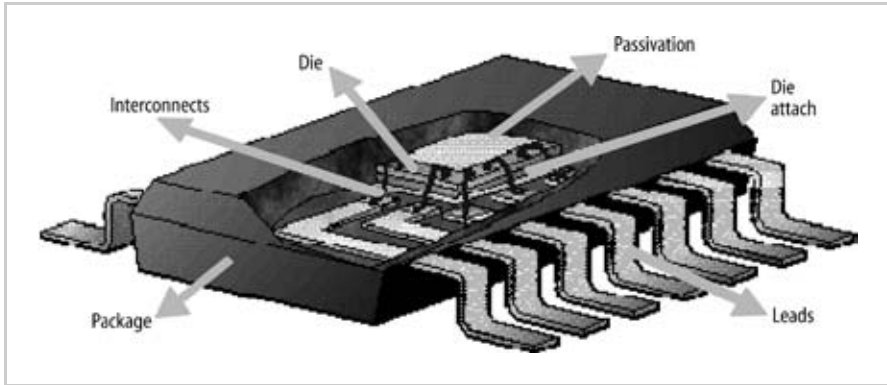


Figure 2.1. The basic structure of a plastic encapsulated leaded semiconductor package showing the die, lead frame, encapsulation and gull-wing leads for surface mounting (Courtesy of CALCE, University of Maryland <http://www.calce.umd.edu/>)

plastic encapsulated devices that have some common elements. As we see in Figure 2.1, the lead frame attaches the chip and provides the electrical pathways from it to its external environment. The leads of the package become an integral part of the solder joint during assembly.

2.1.2 Package and Lead Types

The leads are the most important structural element in the package architecture. Leads are self-supporting paths that connect the electrical component to the outside world (Abtew and Selvaduray 2000). They serve as power, ground and signal input and output (I/O) interconnections from the device to the electrical conductors on the printed wiring board, which is the mounting platform for the circuitry and devices. The leads also connect the package mechanically by being an integral part of the joint between the component and printed wiring board.

Leads may be of the through-hole or surface-mount type. Through-hole leads may be further classified as having uniform or nonuniform cross-sectional area. Pin-grid-array packages or packages of various axial leaded passive components typically have uniform cross section. Those with nonuniform cross-sectional area are typically dual in-line type packages in which a lead shoulder facilitates insertion into the board before assembly, and J-leaded chip carriers, in which the shoulders prevent interlocking during transport.

Surface-mount leads in production use are primarily of the gull-wing or J-lead type; other configurations include the butt-lead (or I-beam), S-lead, spider J-lead, and clip J-lead as shown in Figure 2.2. J-leads are formed under the package, so the package is more space efficient than the corresponding gull-wing configuration. Since the leads do not protrude from the package sides, potential damage during shipping is eliminated. The disadvantages of J-leads include their higher profile, difficulty in probe testing and solder joints that are only marginally visible.

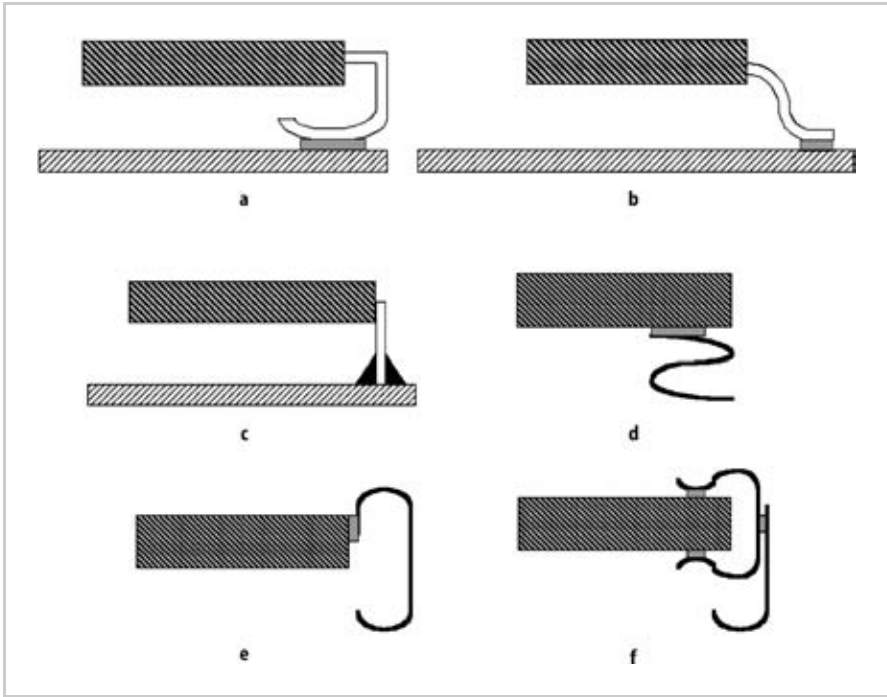


Figure 2.2. Surface-mount lead designs: (a) J-lead, (b) gull-wing lead, (c) butt-lead, (d) S-lead, (e) spider J-lead, and (f) clip J-lead. (From Michael Pecht, *Integrated Circuit, Hybrid and Multichip Module Package Design Guidelines*; Copyright © 1994 John Wiley & Sons. Reprinted with permission of John Wiley & Sons.)

The gull-wing lead is an improvement of the J-lead. The gull-wing lead configuration, used for packages with high input/output counts and closely spaced leads, provides a low profile, a visible solder joint, an electrical probe surface on top, and a stress-relieving stepped shape. Disadvantages of the gull-wing lead include extended leads that require a larger printed wiring board area for mounting. Production problems can arise with fine-pitch high-I/O packages, and the leads are easily bent and may create difficulty in cleaning under packages.

Butt leads join the package to the pad without any preformed configuration, as shown in Figure 2.2. This lead configuration neither attains the solder-joint strength characteristic of gull-wing or J-lead mountings nor yields the same solder-joint fatigue reliability. The S-lead, spider J-lead and clip J-lead configurations are attempts to build a more compliant surface-mount lead structure without making the lead too fragile. The clip lead has solder at the clip end that is reflowed to complete the attachment of the lead. The longer lead length does, however, degrade high-speed electrical signals. These alternatives are not widely used in production.

Conventional packages with these leads included quad-flat packs (QFPs) and thin small outline packages (TSOP). However, I/O and pitch limitations, relatively

long lead lengths with the associated inductances, capacitances, and resistances, as well as yield issues in soldering, have pushed area-array packages to the forefront of packaging architectures today.

2.1.3 Lead Finishes

The lead is critical in creating a reliable solder joint. The surface of leads must be wettable to molten solder, or *solderable*. The metallurgical processes of wetting and joint formation are discussed in detail in Chapter 3. The surface of the leads must remain solderable during testing, processing and storage of packaged semiconductor devices before assembly. Storage periods may be as long as a year or more, depending upon the device type and market demand.

The lead frames of the plastic encapsulated semiconductor devices used in production of electronic devices are typically made of copper alloys, since copper provides high conductivity while maintaining the necessary mechanical strength and formability. Various Cu alloys used for leads are shown in Table 2.1.

While copper is among the most solderable of metals, its susceptibility to surface oxidation makes it difficult to store and handle in electronic assembly, and heavy copper oxide buildup is not easily broken down with soldering fluxes. Various surface finishes are needed for long-term solderability. Electroplating with SnPb or dipping in molten SnPb solder have traditionally provided the best finish for production solderability, but this approach will likely be phased out in favor of Pb-free electroplated finishes. Alternative lead materials,

Table 2.1. Copper lead frame and FeNi-based lead materials

Material	Nominal composition	Solderability (scale of 1–4) with rosin flux	CTE (10 ⁻⁶ /K)	Thermal conductivity (W/m K)	Electrical resistivity (μΩ cm)
Cu alloy 194 [C-194]	2.35Fe/0.03P/0.12Zn/97.5Cu	2	17.4	260	2.54
Cu alloy 197 [C-197]	0.6Fe/0.2P/0.04Mg/99.16Cu	2	~ 17.4	320	2.16
Cu alloy 151 [C-151]	1.0Zr/99.0Cu	1	17.6	380	1.81
ASTM F-30 [Alloy 42]	42Ni/58Fe	4	4.0 ~ 4.7	16	70
ASTM F-30 [Alloy 52]	50.5Ni/48.5Fe	4	10.2	100	~ 45
ASTM F-15 [Kovar]	29Ni/17Co/54Fe	4	5.1 ~ 5.87	40	49

Solderability scale: 1 - BEST, 4 - WORST

Table 2.2. Common lead-finish systems

Lead material	Final finish options	Typical underplating options
Cu alloy lead frame or pin	60Sn40Pb	None or Cu strike plate
	90Sn10Pb	
	Sn	Cu or Ni
	Pd	Ni
FeNi alloy pin	Au	Ni or Cu
	Sn	Ni
		Electroless NiP
		Cu
Brass or bronze connector pins	Sn	Cu
	Au	Ni or Cu

as described below, are FeNi alloys, such as Kovar or Alloy 42, which are widely used in glass sealed packages for their low coefficient of thermal expansion. However, FeNi alloys have relatively poor solderability in comparison to copper, as shown in Table 2.2. For some applications, such as connectors, brass or bronze alloys may be used.

As previously mentioned, various finishes can be used to provide the necessary solderability for the handling and storage requirements of microelectronic manufacturing. Common finish systems for the materials mentioned are summarized in Table 2.2. Options with Pb, such as near-eutectic SnPb in electroplated or hot-dipped forms, as well as electroplated 90Sn10Pb, are likely to be phased out in favor of pure Sn (Nimmo 2002, Prasad 2002). While pure Sn has been used as a finish for many years, it presents some challenges in electronic assemblies, as detailed below. FeNi alloys require *underplating* prior to the final finish to insure solderability and adhesion. Several finishing schemes are used, including Au, Sn or SnPb final finishes with copper, nickel or electroless nickel-phosphorus underplatings. Less-common finishes include immersion coatings of Sn or electroplated coatings of palladium, rhodium or silver.

Finish thickness is extremely important in solder-joint reliability. Molten solders undergo *reactive wetting*: plated layers are partially or fully dissolved while in contact with the molten solder and intermetallic compounds are formed during this reaction. It is undesirable to expose a nonsolderable or poorly wetted subsurface layer. Finish thickness is usually not specified on leaded electronic devices; rather, solderability requirements are given in the form of accelerated aging and wetting test requirements. However, to meet storage requirements with good solderability, minimum thicknesses are needed. Typically, a final Sn-plated finish must be about 2.5–3.8 μm thick to provide good solderability; Au finishes require about 0.9–1.3 μm . Underplating must also be of adequate

thickness: typically, Ni layers should be about 1.3–2.5 μm , while Cu should be about 3.8 μm or more. The interfaces between the underplating and final finish may also come in contact with the solder and thus should be free of contamination and oxidation with good adhesion. Hence, plating processes must be tightly controlled to insure solderability.

2.2 Pure Sn Coatings – Tin Pest and Tin Whiskers

Electroplated Sn deposits have been used for many years to provide solderable surfaces on lead structures, shielding and various mechanical components that are soldered in electronic products. In general, Sn electrodeposits are classified by their appearance: bright (shiny) and matte (dull). This difference arises from the plating-bath chemistry: bright Sn is deposited from an acid-based bath with organic additives, while dull matte finishes are deposited from an alkaline-based chemistry. These differences, along with other process variables such as current density and agitation level, influence the surface texture of the deposit, which in turn influences the final appearance.

The term *texture* refers not only to the surface roughness and reflectivity of the deposit but also to its metallurgical properties. Bath chemistry influences the metallurgical texture, including the grain structure and preferred orientation of the metal crystals nucleated on the plated surfaces. The relative purity of the deposit is also affected: acid baths tend to have lower purity, with electrodeposits containing appreciable codeposited organic and metal impurities, whereas alkaline Sn is of higher purity. Overall, purity tends to influence solderability, so that matte-alkaline Sn deposits are more desirable for long-term, highly solderable surfaces. Plating-bath chemistry and process parameters also affect the residual stresses in the deposit: higher deposition rates and acid-bath chemistries can be prone to higher levels of residual stress.

Tin undergoes two metallurgical phenomena that influence its utility as a finish for long-term solderability. Pure Sn undergoes an allotropic transformation at 13°C that has devastating effects on the finish, which flakes off in circular patches called *whorts* or *tin pest*. In addition, Sn seeks to relieve any compressive stresses from the deposit by forming single-crystal extrusions called whiskers. The extension of whiskers between conducting elements leads to short circuits and systems failures.

2.2.1 Tin Pest – The Allotropic Transformation of Sn

Tin is subject to an *allotropic transformation* – a phase change driven by a change in crystal structure – within the temperature ranges in which a plated component may be required to serve. Above 13°C, Sn exists as a ductile metal – white Sn, with a preferred body-centered-tetragonal crystal structure. Below 13°C, gray Sn,

a cubic, brittle semiconductor, is energetically preferred. These two structures of course differ dramatically in the volume of the unit cell comprising the crystal. Hence, deposits can literally disintegrate when the allotropic transformation occurs in an electrodeposit, causing it to flake off in dark gray patches.

Fortunately, the white-Sn to gray-Sn transformation is easily impeded by the presence of impurities at even low concentrations. In practice, it is not observed in acid-based bright Sn or 90Sn10Pb. In addition, the transformation reaction is kinetically quite slow. At the equilibrium temperature, the transformation is normally not observed in practical implementation of pure tin deposits, and extensive supercooling below the equilibrium temperature is required to drive the reaction and observe tin whorls. The reaction tends to be fastest at about -40°C to -50°C . This may tend to preclude the use of pure tin from alkaline baths for low-temperature applications of lead finishes or other solderable surfaces where the presence of conductive metal particles may be of concern.

The susceptibility of a deposit to the allotropic Sn transformation can be tested by soaking near the temperature that produces the maximum rate of growth of gray Sn. The phenomenon has been observed to occur within 1000 h; it has also been observed in long-term thermal cycling tests conducted from -55°C to $+125^{\circ}\text{C}$ (Evans 1988). The transformation can be confirmed by diffraction studies of residual powders.

2.2.2 Extrusions – Whisker Growth

The formation of Sn extrusions may be of great concern in the application of electroplated Sn. It has long been known that Sn relieves residual stresses by developing metal extrusions called *whiskers*, a name derived from their peculiar morphology (Gaylon 2003). Thicker coatings, alkaline deposits and reflowed electrodeposits have been thought to reduce the risk of whisker formation, but experience shows that no risk-free coating of pure Sn exists. Additions of Pb have been most effective at reducing this problem, so that it may become more prevalent with Pb-free components.

A variety of components have exhibited whisker growth, including Sn-finished lead frames and Sn-finished terminations of multilayer chip capacitors. The optical microphotograph in Figure 2.3 shows whiskers extruded from the surface of a Sn-plated capacitor termination (Brusse 2003). However, here the terminations were not soldered, but attached with adhesive. Such structures, which can grow longer than 200 micrometers, can clearly cause short circuits if they reach between leads of a device or any conducting elements.

Tin-whisker growth is attributed to a reduction in residual stresses in which growth is fueled by dislocation climb and diffusion (Lee and Lee 1998). X-ray diffraction measurements show that residual stresses develop after the deposit has aged and that when whiskers develop, compressive stresses are relieved by nearly 40%. At the low temperatures at which Sn whiskers occur, grain-boundary

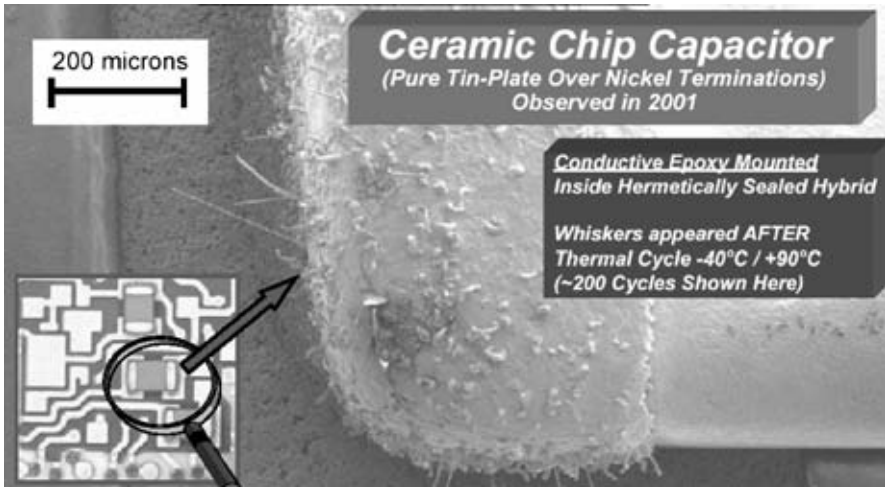


Figure 2.3. SEM observations of whiskers emanating from the Sn-plated surface of a chip capacitor termination (Courtesy of NASA Goddard Space Flight Center (<http://nepp.nasa.gov/whisker>))

diffusion is likely to play an important role in supplying the necessary Sn atoms for whisker development, along with dislocation motion. The optimal temperature for whisker growth is about 50°C. We can surmise that at temperatures above about 150°C, annealing of the Sn reduces the residual stresses and thus the likelihood of whisker development.

The primary factor in residual stress development is the formation of intermetallic compounds (Schetty 2002). In particular, the development of Cu_6Sn_5 causes increasing compressive stresses in the Sn coating. This accounts for the incubation period before whisker growth is observed, and may also account for the greater susceptibility of bright acid Sn: Cu may be codeposited in the plating, leading to the formation of Cu_6Sn_5 in the grain boundaries of the deposit and thus increasing residual stresses. In addition, the use of nickel underplating also reduces the potential for whisker development. The development and growth of intermetallics are covered in more detail in Chapter 5.

Other factors playing a role in whisker development include thin oxides on the Sn surface, metallurgical texture and grain structure. The presence of a thin oxide is necessary to support the development of the whisker (Choi *et al.* 2002); extrusions are thought to occur preferentially where the oxide of the Sn electroplate has sheared (Gaylon 2003). In addition, the orientation of the coating, as measured from diffraction studies, indicates that a resistant coating may have a preferred texture (Schetty 2002). Recall that reflowed (melted and solidified) Sn coatings tend to be more resistant to developing Sn whiskers. Sn coatings, after melting and solidification, have a preferred orientation on Cu of $\langle 220 \rangle$, similar to plated near-eutectic SnPb, which is also resistant to whisker formation. On the other hand, acid-based Sn coatings have a preferred $\langle 211 \rangle$ orientation on Cu. Finally, electroplated deposits can form a columnar grain

structure relative to their direction of growth, and this may also cause a propensity for extrusions.

As we can see, the formation of whiskers presents a difficult problem for using electroplated coatings of near-pure Sn or SnCu, which are prime candidates for replacing Pb-based finishes. Accelerated tests are desirable to evaluate specific applications and emerging technologies such as alternative plating-bath chemistries (Schetty 2002) or nonconventional finishes such as plated SnBi alloys or SnAg electroplated compositions (Yanada 1998). Diffusion-based phenomena can generally be accelerated by increasing temperatures above the application temperature of the equipment or device so as to promote intermetallic growth and grain-boundary diffusion. However, increasing temperatures also tend to reduce residual stresses, particularly above about 150°C for Sn. This tradeoff effect suggests an optimum temperature for whisker growth that may be near 50°C. The initiation of growth may, however, be highly sensitive to other factors.

2.3 Ball-grid Arrays and Chip-scale Packages

Peripherally leaded packages such as quad-flat packs (QFPs) are cost-effective vehicles for semiconductor devices until the pin count goes above 200. Area-array interconnection schemes take over above 200 pinouts (I/Os) because they take less board area, often with a much more relaxed I/O pitch. For years, pin-grid arrays (PGAs) were used for large advanced I/O devices. Now, however, the ball-grid array (BGA), the surface-mount analog of area-array packages, has become the package of choice for these devices (Baliga 1999).

A BGA package is intended for active devices for surface-mount applications utilizing all or part of the device footprint for the interconnection pattern. The interconnections are made of balls (spheres) usually of a solder alloy. Placement is usually far easier and more reliable than for fine-pitch QFPs, and BGAs usually produce a much higher assembly yield. The smaller package size or higher I/O count allows a further miniaturization step. Therefore, most microprocessors, graphic chips and ASICs that have too many I/Os for a peripherally leaded package, are packaged as BGAs.

Figure 2.4 schematically shows the cross section of a typical BGA package, an overmolded and wire-bonded chip attached to a carrier or substrate whose other side is attached to the solder balls responsible for the final interconnection to the printed-circuit board. The substrate is generally made of 0.25-mm bismaleimide-triazine BT laminate with 18 μm copper thickness. A variation is the tape or tab BGA (TBGA), based on a flexible polyimide film (tape) with copper metallization on both sides. For smaller sizes, various advanced BGA technologies or chip-scale packages (CSPs) may be employed. The “slightly larger than IC carrier” (SLICC) developed at Motorola has a ball pitch of 0.9 mm and ball diameter of 0.5 mm. Figure 2.5 shows the fine pitch and small size achieved with a CSP package.

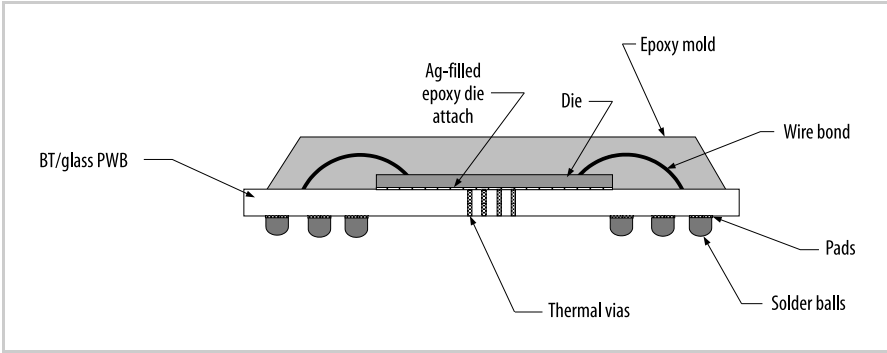


Figure 2.4. A cross section of a typical plastic overmolded BGA

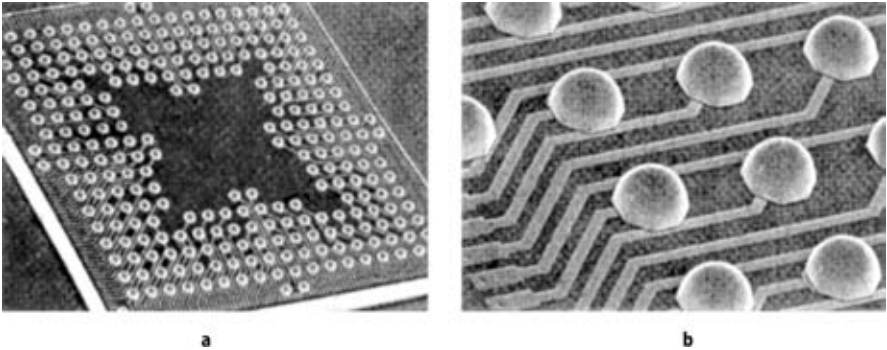


Figure 2.5. A micro-BGA with 275 pads 0.5 mm pitch (Treece, mini Ball Grid Array (mBGA) Assembly on MCM-L Boards in Electronic Components and Technology Conference, © IEEE 1994. Used by permission.)

2.3.1 Flip-chip Packaging

The flip-chip technique involves mounting a chip directly on a substrate using various interconnect materials and methods, with the chip surface facing the substrate (Lau 1996). The various configurations for flip chip are shown in Figure 2.6. The flip-chip interconnect is based on three fundamental building blocks: the bumps on the chip, the substrate and the method of joining the chip to the substrate (Boustedt 1998). Flip chips offer some very significant advantages over conventional packaging, including superior electrical performance, potentially higher reliability, reduced footprint, higher I/O counts, finer pitches, and potentially reduced cost.

There are many different technologies for joining flip chips: soldering, thermocompression joining, thermosonic joining, and adhesives. In the soldering process, solder-bumped chips are soldered onto the circuit board. Solder is usually, but not always, deposited onto the substrate pad areas. In thermocompression bonding, the bumps of the chip are bonded to the pads on the substrate by force and

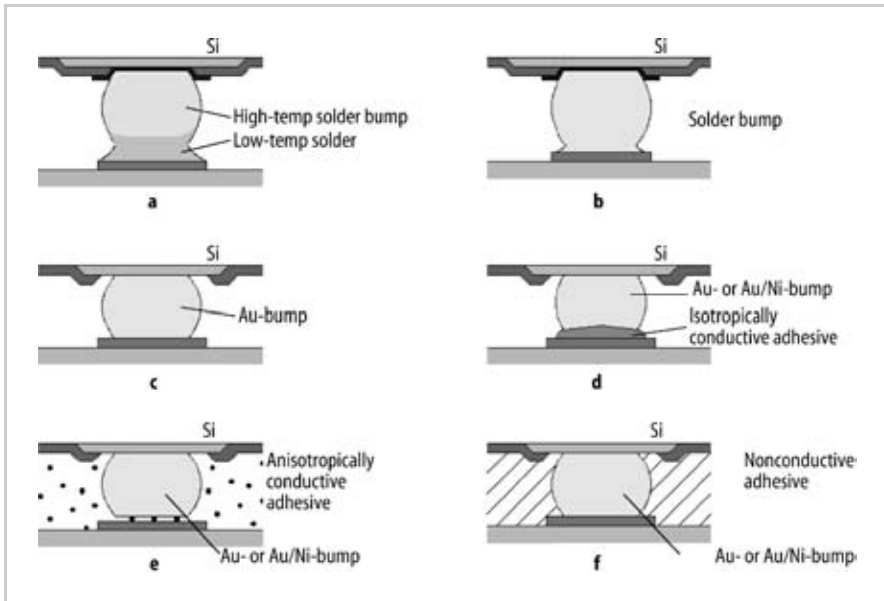


Figure 2.6. Different types of flip-chip joints (from Pecht, Integrated Circuit, Hybrid and Multichip Module Package Design Guidelines; Copyright © 1994 John Wiley & Sons. Reprinted with permission of John Wiley & Sons)

heat is applied. The process requires gold bumps on the chip or the substrate and a correspondingly bondable surface (*e. g.* gold, aluminum). Due to the high bonding forces and temperatures required, the process is limited to rigid substrates such as alumina or silicon. Thermocompression bonding can be made more efficient by using ultrasonic power to speed up welding; the ultrasonic energy softens the bonding material and makes it vulnerable to plastic deformation. The main benefits of this thermosonic method over thermocompression are lower bonding temperatures and shorter processing times. Adhesively bonded flip chips have the advantages of thin structures and cost effectiveness. Conductive adhesives have become a viable alternative to lead-tin solders in flip-chip joining, and anisotropically conductive adhesives can also connect fine-pitch devices. In addition, nonconductive adhesives can be used for flip-chip bonding; here the joint surfaces are forced into intimate contact by the adhesive between component and substrate.

The most important issue in flip-chip technology is reducing the cost of forming the flip-chip bump and underbump metallurgy (UBM). Therefore, thin-film deposition, electroplating, and screen printing are processes used to form bumps.

2.3.2 Pb-free BGA, CSP and Flip Chips

The challenges in array-area packaging are to develop appropriate solder-ball compositions and finishes for the package substrate. SnAgCu alloys are the

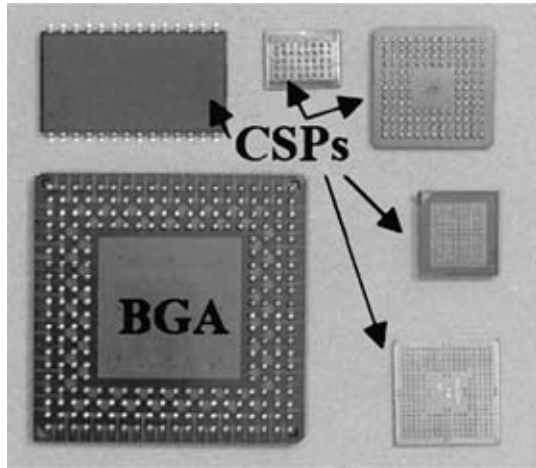


Figure 2.7. Comparison of various area-array package styles. (Courtesy of Reza Ghaffarian NASA JPL CIT.)

leading contenders to replace SnPb near-eutectic alloys for assembly. These materials have been successfully employed for BGA, CSP and flip-chip balls, and will be compatible with Pb-free assembly processes (Wojciechowski *et al.* 2001). Near-eutectic 96.5Sn4Ag0.5Cu and 96.5Sn3.5Ag1.0Cu alloys have also been used successfully for array packages of the types shown in Figure 2.7.

2.4 Assembly Technology

There are several critical processes in component assembly, as summarized in Figure 2.8. All these processes and their associated materials may in turn be impacted by usage of Pb-free alloys, particularly as the technology shifts to smaller joint spacing. We now turn our attention to assembly, discussing processes, key materials and issues in Pb-free transitioning.

2.4.1 Solder Paste

Solder paste is a widely used medium for putting down solder and flux in a single operation on a footprint for subsequent reflow soldering (Hutchins 1989). Solder paste is a homogeneous and kinematically stable mixture of solder alloy particles and flux (Hwang 1989a). Several critical properties of solder paste affect successful joint formation; among the most important are particle morphology, metal loading and rheological behavior, all of which in turn affect paste performance. Manufacturing performance depends on how easily and

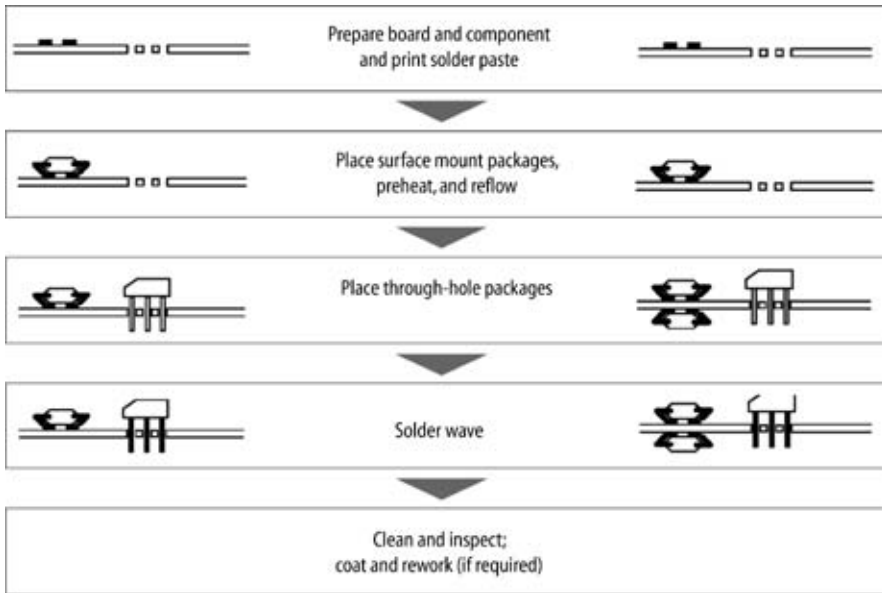


Figure 2.8. General flow of the assembly process (Courtesy of CALCE, University of Maryland <http://www.calce.umd.edu/>)

accurately the paste can be deposited, the slumping resistance, wettability to the substrate and solder-ball formation.

Solder pastes are normally made with fully alloyed solder powder. The shape and size distribution in this powder determines the surface condition, which affects the behavior of the paste during reflow soldering (Judd and Brindley 1992). The particle size is defined by the mesh size of the sieve through which the powder has been passed. The desirable particle morphology for solder powder includes a spherical shape, which yields the greatest reproducibility in rheological properties, and a smooth surface without satellites. As finer and finer pitches or pad spacings are implemented, particle size will be reduced, in turn affecting rheology. In addition, smaller particles have intrinsically greater oxide contents due to increased surface area per unit weight, and this may affect wettability during joint formation.

The rheology or flow behavior of solder-paste materials is complex (Evans 1987), since these materials exhibit both *thixotropy* and *pseudoplasticity*. Thixotropy implies that viscosity decreases over time under constant shear rates and decreases with increasing shear rates, behavior exemplified by the presence of a hysteresis loop in the shear stress versus shear rate curve for increasing and decreasing shear rates during viscometer measurements. Apparent viscosity also decreases with increasing shear rates. Excessive thixotropy is undesirable, since it causes the paste to fluctuate in viscosity over the course of a working day as the paste is agitated by mixing, handling and screening.

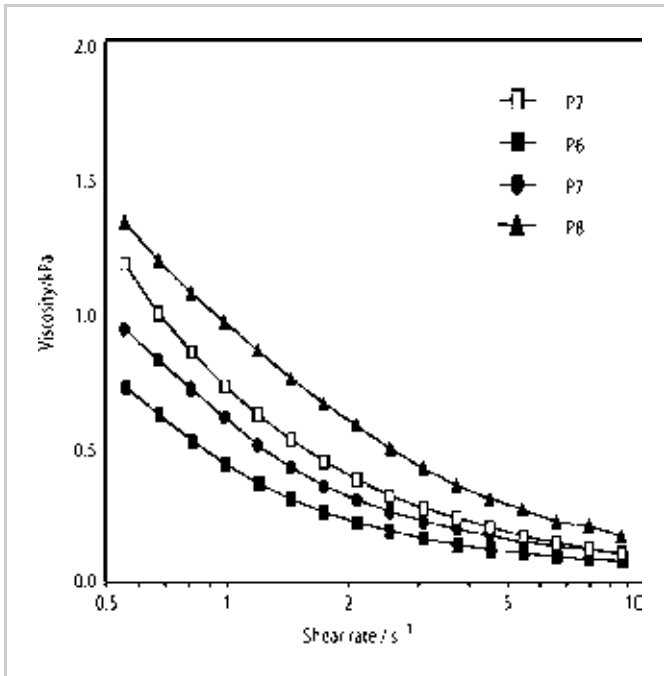


Figure 2.9. Apparent viscosity versus shear rate for SnAgCu solder pastes with similar flux vehicle, by increasing metal content, as shown with samples P6 (88%), P7 (89%), P8 (90%) (Jackson *et al.* 2002)

Thixotropy may also hinder reproducible viscosity measurements depending upon the duration of recovery time after initial agitation of the paste. Pseudoplasticity implies that paste viscosity drops dramatically on the application of shear stress and recovers on removal of the stress. This is desirable behavior since it facilitates passage of the paste through the application screen or dispensing syringe while allowing it to remain on the desired area after the application stresses are removed. Finally, thicker pastes may also exhibit yield-point behavior, implying that a minimum shear stress is required to cause the paste to flow.

Rheology is very important in applying the paste by stencil. While stenciling is a low-cost option for creating solder joints, it accounts for nearly 60% of all assembly defects. Thus rheology and its characterization are critical to the development of alternatives to SnPb solders (Jackson *et al.* 2002). A paste must flow evenly and must have consistent properties in order to achieve good-quality printing without defects. Consequently, unstable behavior due to high thixotropy is undesirable. Also, the organic vehicle must maintain the particles in suspension without excessive sedimentation or segregation; the relative viscosity level is also important, since thicker or more viscous materials require different squeegee pressures and shear rates during paste application.

Table 2.3. Solder paste properties and slumping behavior (Evans 1987)

Paste number	Equivalent spherical radius, R_e (μm)	Elongation factor E_F	Metal loading, M_L (w/o)	Apparent viscosity η_A (Kcps)	Slump factor S_L
1	34.5	4.9	86.3	645	13.0
2	34.3	1.92	82.6	540	3.43
3	9.7	3.61	85.4	570	9.14
4	7.2	0.67	85.5	655	11.05
5	26.1	2.99	88.3	900	1.52
6	25.8	3.18	82.6	200	12.95
7	27.7	3.99	78.9	1095	39.62
8	28.2	3.58	78.3	485	20.57
9	27.3	3.10	85.6	720	3.43
10	34.2	3.53	76.8	1800	14.86
11	34.4	3.50	78.1	340	11.05
12	8.6	1.90	84.4	1750	66.29
13	6.8	2.43	79.8	225	112.00
14	28.3	2.28	89.8	700	9.14
15	18.4	0.65	66.7	895	41.52
16	27.0	3.17	85.6	610	1.52
17	33.2	3.19	88.1	380	18.67
18	32.2	3.05	70.9	1435	104.38
19	8.5	2.16	88.0	480	152.00
20	7.9	1.75	88.5	710	39.62
21	32.3	5.48	84.3	450	1.52
22	21.5	0.84	85.1	1690	30.10
23	25.6	3.59	84.1	320	5.33
24	26.7	3.54	85.6	650	1.52

Several factors influence paste rheology. Spherical powders provide the most consistent rheological behavior. Increasing the metal content in a given vehicle tends to increase viscosity. Under constant metal loading and vehicle conditions, viscosity increases with decreasing particle size. Higher metal loads make screening more difficult because higher squeegee pressures are required. However, higher metal loads tend to reduce slumping or flowout when the solder paste is heated, so that the incidence of bridging or electrical shorting may be reduced.

Several different rotational viscometers are available to assess the rheological behavior of solder pastes. A Brookfield-type viscometer equipped with a spindle and a helical path stand is most often used, but cone-and-plate-type Ferranti-Shirely viscometers have also been used (Jackson *et al.* 2002) for accurate paste-flow measurement in stenciling. Since solder pastes are thixotropic, their shear history affects the measurements: a paste that has recently been agitated has a different viscosity at a specific shear rate from one that has had a significant recovery period. In addition, temperature fluctuations can significantly affect viscosity readings.

As the solder powder is likely to be contaminated with oxides from powder manufacture, effective fluxing is needed. The function of the various fluxes in solder paste (for example rosin, synthetic rosin, and organic solvents) is to assist wetting by chemically cleaning the surfaces of substrate and solder powder during reflow soldering (Hwang 1989b). Also, flux materials can be designed to remain on the board after reflow soldering without causing corrosion or lowering insulation resistance.

The transformation to Pb-free solders has a significant impact on pastes, particularly affecting wetting and rheology. Higher melting and reflow temperatures require alternative fluxes that may differ rheologically. In addition, SnAgCu alloys are less dense (for example, the density of 95.5Sn3.8Ag0.7Cu is 15% below that of near-eutectic SnPb), and this also affects the rheology (Jackson *et al.* 2002). Hence, Pb-free solders require surface-mount processes to be reoptimized in order to maintain low defect content.

2.4.2 Stenciling

Stencil printing is widely used to transfer solder paste onto boards or to create balls for area-array packages. The stencil is held at a small distance (“snap-off”) from the board being printed; the downwards pressure of the squeeze overcomes the snap-off and creates a line contact between stencil and board that traverses the board due to the elasticity of the stencil. The paste is deposited on the board through the stencil pattern and is left behind when the stencil lifts off the board. With solder-paste printing the squeegee is lifted over the leftover paste, more paste being added if necessary, and the next board is printed on the next squeegee stroke. The main factors involved in optimizing stenciling print quality include stencil thickness, pitch, aperture orientation, aperture aspect ratio, stencil snap-off distance, stencil down-stop, squeegee pressure and squeegee speed (Melton *et al.* 1994).

Stencil thickness is determined by the desired pitch of the printed pattern. Current surface-mount printed-circuit boards mostly consist of a mixture of land patterns, including BGA and QFP fine pitch. BGAs typically require a pitch far coarser than (fine-pitch) QFP and the stencil used can be thicker. Thus, it is actually not the BGA that determines the optimal stenciling parameters but

rather the fine-pitch components. However, the emerging flip chip may come to govern the critical stenciling parameters.

Placing the components on the paste requires careful alignment. The paste should have adequate *tack* or sticky consistency to hold the components in place during handling. Placement equipment is characterized as manual, semiautomated, or automated. For BGA, conventional placement systems can be employed, using either the package outline or the position of the solder spheres as a guide (Solberg 1999). A modern vision system should also be able optically to align a BGA package with corner balls removed and/or with additional thermal balls with no interference in the alignment procedure (Lau 1995).

2.4.3 Solder-paste Performance: Slumping

Good solder-paste performance in assembly is essential to high yields. Slumping in particular may be critical in characterizing new solder pastes for flip-chip and fine-pitch applications, particularly since rheological properties are expected to change with changing alloys and flux vehicles. We discuss an example in which 24SnPb paste samples, varying in apparent viscosity, metal loading, particle size, and shape, were evaluated for critical manufacturing performance parameters including slumping.

Slumping occurs prior to reflow, when the paste spreads outward from the pads on which it was deposited, as shown in Figure 2.10. The impact of this behavior may be enlarged solder balls and increased electrical shorts from pad bridging, both of which reduce yield. The importance of slumping is magnified as pad spacing decreases and more solder on pads is desired to improve joint height.

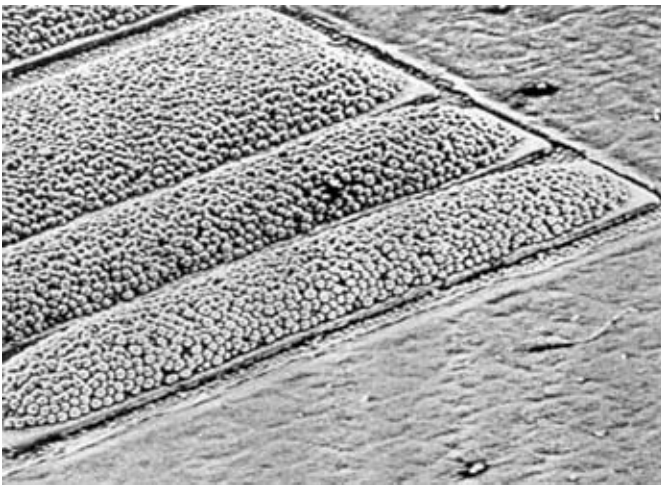


Figure 2.10. Slumping defect on fine-pitch pattern (Courtesy of Seoul National University)

The samples were characterized according to the methods developed by Evans and Beddow (1987). Slumping behavior was measured by stenciling the sample onto a pretinned copper coupon, heating and then evaluating the increase in the pattern diameter. The samples were heated to 80°C and held for 30 min to simulate the prereflow bakeout that removes volatile solvents from the paste. The coupons were evaluated at 5× magnification to determine the postbake diameter of the stencil pattern, and the slump S_L was then determined from Equation (2.1),

$$S_L = 100 \left[\frac{D_{\text{Stencil}} - D_{\text{Pattern}}}{2} \right] \quad (2.1)$$

where D_{Stencil} is the stencil opening diameter in mm and D_{Pattern} is the pattern diameter after baking, in mm. The resulting data were then analyzed by regression analysis, fitting the paste parameters to the slumping behavior using the linear model shown in Equation (2.2),

$$S_L = \beta_0 + \beta_1 R_c + \beta_2 E_F + \beta_3 M_L + \beta_4 \eta_A \quad (2.2)$$

The results of the analysis, given in Table 2.4, show that particle size and metal loading have a significant effect on slumping behavior: these two factors were statistically significant at a confidence limit of 90%. The negative sign of these parameters indicates that larger particle sizes and greater metal loading reduce slumping. However, these parameters interact with flow characteristics to define the minimum pitch that can be achieved when stenciling a particular pattern. While Equation (2.2) is not highly predictive, the significance of the effects is clear.

This study illustrates the need for adequate process characterization in relation to solder-paste performance and is particularly important as the technology shifts to reduced pitch in array packaging. In order to achieve adequate print resolution on the board, smaller particles are desired for stenciling and screening operations. In addition, screening and stenciling forces decrease with lower metal content, allowing thinner stencils for deposition and thus providing finer print definition. However, as shown by this study, reduced metal content and particle size can contribute to slumping, which can reduce assembly yields by causing bridging during reflow.

Table 2.4. Results of regression analysis for paste-slumping performance

Factor	Parameter	Parameter estimate	T-value
	β_0	263	2.2
R_c	β_1	-2.5	2.6
E_F	β_2	4.7	0.59
M_L	β_3	-2.3	1.7
η_A	β_4	0.0082	0.49

Minimum Student-t statistic = 1.7 for 90% confidence level

2.4.4 Reflow Soldering

The reflow soldering process entails heating the PCB and the solder paste so that the solder paste melts, kinetically wets and then solidifies to form the desired solder joints. Soldering can be achieved through different heat-transfer modes, including conduction, convection, focused and nonfocused infrared radiation (IR), infrared convection, vapor condensation, hot gas, resistance, induction, and laser beam (Dow 1989). Each soldering method has advantages and limitations in cost, performance, and operational efficiency depending upon product volume and materials constraints. Table 2.5 compares the various reflow methods. Typically, high-volume reflow processes for BGA and other types of components may be performed in several different ways using a combination of radiation heating via IR, in nitrogen or in air, with full or part convection (Lea 1988) to assist in uniform heating.

Many of the alternative Pb-free solders require higher soldering temperatures than eutectic SnPb, and board materials and components must be compatible with the higher temperatures to avoid damage. The appropriate reflow profile

Table 2.5. Reflow methods

Reflow method	Advantages	Limitations
Conduction	<ul style="list-style-type: none"> ✓ Low equipment capital ✓ Rapid temperature change ✓ Visibility during reflow 	<ul style="list-style-type: none"> ✧ Planar surface and single-side attachment required ✧ Limited surface area
Nonfocused infrared	<ul style="list-style-type: none"> ✓ High throughput ✓ Versatile temperature profiling and processing parameter 	<ul style="list-style-type: none"> ✧ Mass, geometry dependency
Vapor-phase condensation	<ul style="list-style-type: none"> ✓ Uniform temperature ✓ Geometry independence ✓ High throughput 	<ul style="list-style-type: none"> ✧ Difficult to change temperature ✧ Temperature limitation ✧ Relatively high cost
Hot gas	<ul style="list-style-type: none"> ✓ Low cost ✓ Fast heating rate ✓ Localized heating 	<ul style="list-style-type: none"> ✧ Temp. control ✧ Low throughput
Convection	<ul style="list-style-type: none"> ✓ High throughput 	<ul style="list-style-type: none"> ✧ Slow heating
Induction	<ul style="list-style-type: none"> ✓ Fast heating ✓ High-temperature capability 	<ul style="list-style-type: none"> ✧ Applicability to nonmagnetic metal parts only
Laser	<ul style="list-style-type: none"> ✓ Localized heating with high intensity ✓ Short reflow time ✓ Packaging crack prevention ✓ Superior solder joint 	<ul style="list-style-type: none"> ✧ High equipment capital ✧ Specialized paste requirement ✧ Limit in mass soldering

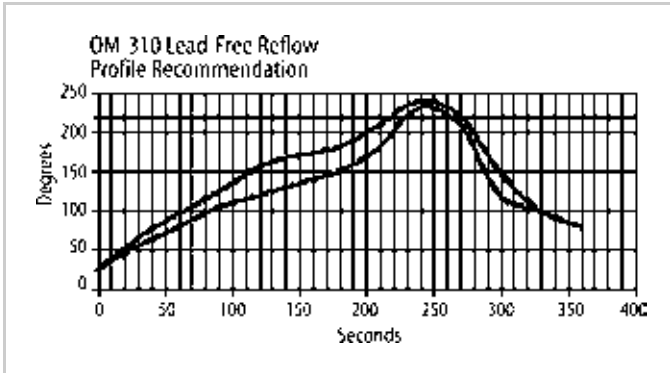


Figure 2.11. Reflow profile envelope recommended for Alpha Metals SnAgCu pastes. The profile can be achieved with appropriate combinations of IR and convection heating (Courtesy of Cookson Electronics, Alpha Metals)

must be utilized for the solder paste and alloy composition. Typically, the peak temperature must significantly exceed the melting point. Preheating ramp rates and ramp-up to melting are between 1–3°C per min to throughput without damage and with low defect rates. Figure 2.11 shows a typical reflow profile that is recommended for SnAgCu paste.

2.4.5 Wave Soldering

Wave soldering is used to create joints for through-hole configurations as well as to solder chip components. The process, shown diagrammatically in Figure 2.12, has been in wide use for many years with near-eutectic SnPb due to its cost advantages and high throughput for high-volume products. Preheating, wave temperature and wave exposure time are among the most important parameters. In addition, board attack angle, wave height and shape, wave oil content and the ambient atmosphere influence the defect content and throughput depending upon the alloy used.

Several alloys may be used for wave soldering to achieve Pb-free assemblies, including SnAgCu alloys, SnCu eutectic and SnAg eutectic as the leading candidates (Nimmo 2002). SnAgBi and SnAgCuSb have also been successfully used with low solid fluxes at wave temperatures of 250°C (Artaki *et al.* 1995). However, as discussed in Chapter 3, Bi alloys may suffer from segregation-producing defects.

Increasing temperatures and solubility limits may lead to increasing dissolution of Cu from leads and boards into the molten solder for the leading alloys, particularly for high Sn content Pb-free solders. In addition, with changing lead finishes, Au buildup may be of increasing concern in wave soldering in the future. Cu also produces greater drossing rates, as do SnZn alloys, factors likely to increase maintenance requirements and costs for wave soldering in the future (AIM Solder Report 2003).

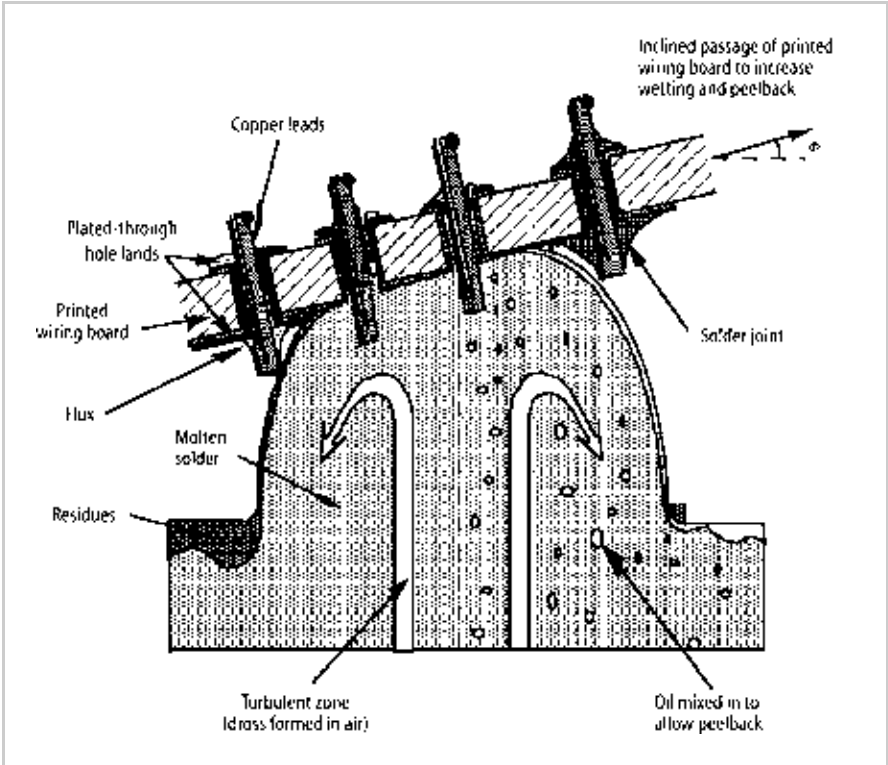


Figure 2.12. Diagram of wave soldering showing wave elements and board contact. (Reproduced from Malhotra, A., “Wave Soldering and Reflow Soldering” in *Soldering Processes and Equipment*, M. Pecht (ed.), copyright John Wiley and Sons, NY (1993). With permission of the publisher.)

Table 2.6. Common flux types and cleaning materials for removal

Cleaning medium	Flux type				
	Rosin (benign)	Rosin (aggressive)	WSF	SA	LSF
None (no-clean)	X	–	–	–	X
Chlorinated solvents or CFC-113 based	X	X	–	X	–
Aqueous (saponifier)	X	X	X	–	–
Semiaqueous (terpenes)	X	X	X	X	–

2.4.6 Cleaning

The objectives of cleaning are principally to remove ionic contaminants and flux residue. Wet-immersion methods are commonly used with organic solvents for rosin-based fluxes. Table 2.6 summarizes cleaning materials and flux types. With the advent of SnAgCu or other Pb-free replacements, changes in flux vehicles and increasing solder temperatures may require more aggressive cleaning processes.

References

- 1 Abtew, M., and Selvaduray, G.,(2000) "Lead-free Solders in Microelectronics", *Mat. Sci. Eng.*, Vol. 27, pp. 95–141.
- 2 AIM Soldering (2003), *Study of Lead-Free Wave Soldering*.
- 3 Alpha Metals, (2004), OM-300 Series Solder Paste, Product Manual.
- 4 Artaki, I., Finley, D. W., Jackson, A. M., Ray, U., and Vianco, P., (1995), *Wave Soldering with Pb Free Solders*, Surface Mount International.
- 5 Baik, K. Y., (2000), "Electronic Packaging Material", *Trends in Metals and Materials Engineering*, Vol. 13, No. 4, pp. 26–33.
- 6 Baliga, J., (1999) "Ball Grid Arrays: The High Pincount Workhorse", *Semiconductor International*, September 1999.
- 7 Banerji, K., (1994) "Development of the Slightly Larger Than IC Carrier (SLICC)", *Proceedings of NEPCPN West*, pp. 1266–1276.
- 8 Boustedt, K.,(1998), "GHz Flip Chip — An Overview", *Proceedings of Electronic Component and Technology Conference*, pp. 297–301.
- 9 Brusse, J., (2003) A Discussion of the Significance of Metal Whisker Formation to the High Reliability Community.
- 10 CALCE Center, (2003), "How to Prepare for Lead Free Soldering", CALCE Short Course, 2003.
- 11 Choi, W. J., Lee, T. Y., Tu, K. N., Tamura, N., Celestre, R. S., MacDowell, A. A., Bong, Y. Y., Nguyen, L., Sheng, G. T., (2002), *Structure and Kinetics of Sn Whisker Growth on Pb-Free Solder Finish*, 2002.
- 12 Davy, G., (2002) *Relay Failure Caused by Tin Whiskers*, 2002.
- 13 Dow, S., (1989) "Reflow Soldering Survey", *Circuits Manufacturing*, p. 42, 1989.
- 14 Dubravka Rocak, Vinko Stopar, and Janeta Fajfar Plut, (1995), "Solder Paste for Fine Line Printing in Hybrid Microelectronics", *J. of Microelectronics*, 26, 1995, pp. 441–447,
- 15 Evans, J., (1987) *Process Optimization of Solder Creams*, unpublished monograph, 1987.
- 16 Evans, J. and Beddow, K., (1987) *Characterization of Particle Morphology and Rheology in Solder Paste*, IEEE, 1987
- 17 Evans, J., (1988) unpublished studies.
- 18 Frear, D. R. (1999), "Materials Issues in Area-Array Microelectronic Packaging", *JOM*, Vol. 51, No. 3, pp. 22–27, 1999.
- 19 Gaylon, G. (2003), "Annotated Tin Whisker Bibliography", NEMI Monograph, July 2003.
- 20 Hinerman, J., Srihari, K., and Westby, G. R., "AART Process Development and Improvement Through Designed Experiments", (1997) *Proceedings of 2nd Annual International Conference on Industrial Engineering Applications and Practice*, vol. 2, pp. 621–626,
- 21 Hutchins, C., (1989), *Surface Mount Technology: How to Get Started*, Sugar Land, C. Hutchins & Associates.
- 22 Hwang, J. S., (1989a), *Solder Paste in Electronic Packaging*, Van Nostrand Reinhold, New York.
- 23 Hwang, J. S.,(1988), "Solder Paste Rheology — Principles and Practice", *Proceedings of EXPO SMT 88*, pp. 171–177.

- 24 Hwang, J. S., (1989b), "Soldering and Solder Paste Prospects", Surface Mount Technology, p. 56.
- 25 Jackson, G.J., Durairaj, R., Ekere, N.N. "Characterisation of lead-free solder pastes for low cost flip-chip bumping", Electronics Manufacturing Technology Symposium, 2002. IEMT 2002. 27th Annual IEEE/SEMI International pp: 223–228
- 26 Judd, M., and Brindley, K., (1992) Soldering in Electronics Assembly, Newness, Oxford.
- 27 Klein-Wassink, R. J., (1989), Soldering in Electronics, Electrochemical Publications, University of Maryland.
- 28 Lau, J. H., (1995), Ball Grid Array Technology, McGraw-Hill, New York.
- 29 Lau, J. H., (1996), Flip Chip Technologies, McGraw-Hill, New York, NY.
- 30 Lea, C., (1988), A Scientific Guide to Surface Mount Technology, Electrochemical Publications, Ayr, Scotland.
- 31 Lee, C., Gopalakrishnan, R., Nyunt, K., Wong, A., Tan, R. C.-E., and Ong, J. W.-L., (1999), "Plasma cleaning of plastic ball grid array", Microelectronics Reliability 39, pp. 97–105.
- 32 Lee, B. Z., and Lee, D. N., (1998), "Spontaneous Growth Mechanism of Tin Whiskers", Acta Metallurgica, 46(10), pp. 3701–3714.
- 33 Malhotra, A., (1993), "Wave Soldering and Reflow Soldering" in Soldering Processes and Equipment, M. Pecht (ed.), John Wiley and Sons, NY.
- 34 Melton, C., Klosterman, D., and Mei, Y., (1995), Lead-Free Solder Fine Pitch Stencil Printing, SMI.
- 35 Nguty, T. A., and Ekere, N. N., (2000), "Modeling the effects of temperature on the rheology of solder pastes and flux system", J. of Materials Science: Materials in Electronics 11, pp. 39–43.
- 36 Nimmo, K., "Review of European Legislation and Lead Free Technology Roadmap", Proceedings of International Conference on Lead-Free Electronic Components and Assemblies, San Jose, CA, 2002.
- 37 Pecht, M., ed. (1991), Handbook of Electronic Package Design, Marcel Dekker, New York.
- 38 Pecht, M., ed. (1994), Integrated Circuit, Hybrid, and Multichip Module Package Design Guide-line: A Focus on Reliability, John Wiley & Sons, New York.
- 39 Prasad, S., (2002), NEMI Consortia Efforts on Tin Whiskers and More, Proceedings of International Conference on Lead-Free Electronic Components and Assemblies, San Jose, CA, 2002.
- 40 Ramakrishnan, S., and Srihari, K., (1998), "A Decision Support System for The Alternative Assembly and Reflow Technology Process", Computers Ind. Engng., 35, pp. 61–64. "Repasivation Design Guide", Kulicke and Soffa Flip Chip Division, Revision B, (November 2001).
- 41 Riemer, D. E., (1988) "Analytical Engineering Model of the Screen Printing Process", Solid State Technology, p. 85.
- 42 Schetty, R., (2002), "Tin Whisker Growth and the Metallurgical Properties of Electrodeposited Tin," Proc. International Conference of Lead-Free Electronic Components and Assemblies, IPC.
- 43 Short, R. H., and Lee, N. C., (1989), "Fine Pitch Technology: Optimizing the Role of Solder Paste", Proceedings of EXPO SMT89, Nashville, pp. 83–85.
- 44 Solberg, V., (1999) "CSP Package Development: The 4.0 Manufacturing Process for μ BGA", IEEE, pp. 91–103.
- 45 Treece, R. K., (1994), "mBGA Technology Overview", Proceedings of ELECTRECON, pp. 2-1–2-7.
- 46 Vardaman, J., (1992), Surface Mount Technology, IEEE Press, 1992, IEEE.
- 47 Wicker, T., (2002), "Manufacturability of Lead-Free Solder Paste", Proc. International Conference on Lead-Free Electronic Components and Assemblies, IPC.
- 48 Wojciechowski D., Chan M., Martone F., " Microelectronics Reliability", Volume 41, number 11, November 2001, pp 1829-1839 (11).
- 49 Yanada, I., "Electroplating of Lead-Free Solder Alloys Composed of Sn-Bi and Sn-Ag", Proc. Of the IPC Printed Circuits Expo, Long Beach USA: pp. S11-2 to S11-2- 7, April 1998.

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