
Preface

The foundations of nanotechnology have emerged over many decades of research in various fields. Over the years, computer circuits have been becoming smaller and chemicals have been getting more complex. Biochemists have learned more about how to study and control the molecular basis of organisms. Mechanical engineering has been getting more precise which resulted in, for instance, emerging nanoelectro-mechanical systems (NEMS). Computer engineering have been getting a great deal of knowledge on how to design circuits with defective components. Today, in the young field of nanotechnology, scientists and engineers of various fields are taking control of atoms and molecules individually, manipulating them and putting them to use with an extraordinary degree of precision which was considered impossible many years ago. Word of the promise of nanotechnology is spreading quickly, and the air is thick with news of nanotech breakthroughs especially over the last few years. Public awareness of nanotech is clearly on the rise, too, partly because references to it are becoming more common in popular culture and everyday life.

The wires and switches inside computer chips have been getting steadily smaller for decades. They have already crossed the 100-nm threshold, sufficient to be considered nanotechnology by the National Nanotechnology Initiative (NNI) definition. As they continue to shrink, quantum effects will become increasingly important, and future designs will stop working if not carefully taken into consideration. Researchers in academia and industry are working on various technologies, but among those there are few nanoscale technologies that could potentially take over in near future. One is molecular electronics: the use of single molecules (or sometimes, small clusters of molecules) to build wires and switches. Another is quantum dots: instead of letting electrons flow through wires, the electrons are tethered in place and only shift back and forth. This shift causes nearby electrons to shift also, which is useful for signaling and computation. Finally, carbon nanotube (CNT) based interconnects and transistors; CNTs have shown promising electrical behavior compared to copper used in Complementary Metal Oxide Semiconductor (CMOS) technology.

Technology Scaling Challenges and Effects

As functional density and operating frequency increase, the number of interconnects and length of interconnects are expected to increase as well. Over the years, the number of metal layers has incrementally increased from the original one. Using six to ten metal layers in industry is a common practice nowadays. Increasing number of metal layers in turn increases the number of vias where it is proven that vias are the main sources of defects. The situation will grow worse since the number of metal layers will even further increase going up to 12 within the next few years.

The material of the layers used in fabrication processes has also undergone a major change from aluminum to copper. Using copper provides a better scalability compared to aluminum. As technology scales and more transistors are integrated on a chip, the interconnects become longer. For high-speed nanometer technology designs the interconnect delay dominates gate delay. It is predicted that in the near future the longest path in the design will be the critical one not the paths with more gates. In nanometer technology era, crosstalk will be a major contributor to interconnect delay. To keep the resistance of the wires low as technology scales, the interconnects are becoming narrower and taller. This results in large cross-coupling capacitances which are now dominating substrate capacitances.

To reduce the power and minimize the negative impact of hot carrier, which causes reliability issues overtime, the power supply is reduced. However, the transistor voltage threshold is not scaling proportionally which results in increase in the circuit sensitivity and reduction in noise margin. The scaling also increases the leakage current. In 65 nm technology, the static power consumption contributes to 50% of total power consumption while it is expected to further increase in 45 and 32 nm technologies. Negative bias temperature instability (NBTI) is considered a growing threat to device reliability in sub-100 nm technologies as well.

Technology scaling also poses many challenging design and test issues. The power and speed are two important parameters in today's designs. The low power supply has increased circuits sensitivity to noise caused by IR-drop, crosstalk, and process variations. The voltage threshold does not scale proportionally resulting in reduced noise margin. The wavelength of the light used for imaging the geometries is longer than the geometry desired for printing. For example, a designer uses an almost 200 nm light source for a 130 nm gate length. The circuit speed will be limited by quantum effects along with high power and temperature in future designs. Temperature variation can significantly affect circuit performance. The process variation increases clock skew resulting higher switching activity, hence higher temperature and power supply noise. The continuous decrease in transistor feature size has been pushing the CMOS process to its physical limits caused by ultra-thin gate oxides, short channel effects, doping fluctuations, and the unavailability of lithography in nanoscale range. To be able to continue the size/speed improvement trends

according to Moore's Law, research investments are growing on a wide range of emerging devices and technologies.

Emerging Technologies

This book covers various technologies that have been suggested by researchers over the last decades such as chemically assembled electronic nanotechnology, Quantum-dot Cellular Automata (QCA), nanowires (NWs), and carbon nanotubes (CNTs). Each of these technologies offers various advantages and disadvantages. Some suffer from high power, some work in very low temperature and some other need indeterministic bottom-up assembly. These emerging technologies are not considered as a direct replacement for CMOS technology and may require a completely new architecture to achieve their functionality.

Molecular logic devices are based on electron transport properties through a single molecule. Two terminal molecular devices currently being explored consists of thousands of molecules operating in parallel as digital switches or analog diodes. In both cases, a voltage applied to a molecular layer (group of molecules in parallel) results in reconfiguration of the molecular components. This creates a nano-switch where the reconfiguration capability provide us with the opportunity for computing. A near term opportunity of molecular electronics is in integration of molecular devices with sub-50 nm CMOS components to form a hybrid system. A full-molecular system is considered a potential long-term opportunity. In addition to two terminal switches, few other molecular components emerged over the past few years, e.g. bistable switch, molecular NEMS, and spin-based molecular devices.

Carbon nanotube is a subset of molecular electronic materials. It is a cylinder formed from an atomic sheet of carbon atoms. The carbon atoms are bounded together into an array of hexagons which forms a planar sheet. This sheet is rolled up to form a tube. Carbon nanotubes can have diameters up to 15 nm and lengths up to few microns. The diameter and the way the sheet is rolled up determine whether the carbon nanotube has metal or semiconductor properties. The semiconductor tube can be doped n-type and p-type, making it possible to create n-p junction. Carbon nanotubes have shown strong current capability which makes it interesting to IC designers to replace copper with carbon nanotube, however, the integration will be expensive.

A novel mechanism for transmitting and processing information has been extensively investigated in theoretical work on quantum-dot cellular automata (QCA). This work assumes arrays of cells built from quantum dots, on a molecular scale, from individual redox centers. The charges move within the cells in response to external electric fields. It is fascinating that based on such scheme, there is no need to let charges flow through the cells. Wires, AND/OR gates, clocked QCA cells, QCA memory cell, and a shift register are the components that have been successfully demonstrated. Today, standard solid state Quantum-dot Cellular Automata cell design considers the distance between quantum dots to be about 20 nm, and a distance between cells of about 60 nm. Compared to CMOS technology, QCA is expected to present less variability at this scale.

Digital microfluidics is an alternative technology for lab-on-a-chip systems based upon micromanipulation of discrete droplets. Microfluidic processing is performed on unit-sized packets of fluid which are transported, stored, mixed, reacted, or analyzed in a discrete manner using a standard set of basic instructions. Recent advances in microfluidics technology have led to the design and implementation of miniaturized devices for various biochemical applications. These microsystems have shown promises to revolutionize biosensing, clinical diagnostics, and drug discovery. Such applications can benefit from the small size of biochips compared to conventional laboratory methods.

Developments in these nanoscale technologies provide the hope that current trend of integration of electronic devices can be continued. Due to their small feature sizes and self-assembly-based fabrication methods, nanoscale devices present many challenges in the area of testing, defect tolerance, and reliability. As nanoscale fabrication technologies evolve over the next few years, testing and reliability are expected to emerge as major roadblocks to system integration.

Most of the suggested technologies offer very high defect density (up to 10%). Increasing defect density decreases yield and with such a high defect density in nano-devices the manufacturing cost can be prohibitively high and discarding a defective nano-chip will no longer be possible. As a result, to achieve high reliability, nanoscale devices must be thoroughly tested, diagnosed and the location of defects must be found. Novel defect tolerance methods and architectures must be developed to deal with such high defect densities. For example, architectures similar to field programmable gate array (FPGA) have been suggested to use crossbars built from nanowires/nanotubes. Such crossbars can be programmed and the defects can be avoided if the location of defects is known. Similarly, in other nano-devices and architectures, a reliable system can be created using defective devices.

This book is divided into five sections. Section 1 includes five chapters that discuss different aspects of test and defect tolerance for crossbar-based nanoscale devices. The reconfiguration feature of the proposed nano-architectures provides an ability to test these devices and avoid the defective ones. Section 2 contains four chapters focusing on test, defect tolerance and reliability for QCA circuits.

There are two chapters in Sect. 3 which present methods for testing and diagnosis of realistic defects in digital microfluidic biochips. Due to the underlying mixed-technology and mixed-energy domains, biochips exhibit unique failure mechanisms and defects. Finally, Sect. 4 contains three chapters dealing with reliability of CMOS scale devices, developing nanoscale processors and future molecular electronics-based circuits.

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