

Chapter 2

Integrated Circuits Beyond CMOS

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Semiconductor microelectronics, based on silicon CMOS circuits, is arguably the most successful technology ever developed by mankind because it sustained its fast, exponential (*Moore's Law*) progress for several decades. As a result, this technology has become the basis of all current information technology revolution. However, now scientists and engineers agree that this progress will run into what is called the *red brick wall* of physical, technical, and economical limitations some time during the next decade. Optimists believe this crisis may be deferred until the 22-nm ITRS technology node, to be reached by 2015 or so, while the pessimists like myself do not see any realistic way for the technology to go beyond the 32-nm node, to be reached by 2013 or maybe even a year or two earlier. In any case, the range of opinions (of well-informed professionals) is rather narrow, and continues to shrink.

The negative impact of running into the red brick wall for the high-tech economy may be hardly exaggerated. Sure, whatever happens after that point, there will be more and more silicon chips fabricated each year. However, if the exponential progress of the key metrics, most notably the circuit cost per unit device, has been stopped or slowed down to a crawl, the integrated circuit manufacturing, as virtually all mature manufacturing industries, will most probably be outsourced to countries with cheaper labor. The current electronics industry giants, which currently live on innovation, will face a survival challenge. This is why the extension of Moore's Law into the sub-10-nm range is such a vital task. As usual, there are both good and bad news from the current battle on this *nanoelectronic* frontier.

On the positive side, both the federal government and electronic industry leaders now recognize the necessity and urgency of research in this direction. On the negative side, the efficiency of those efforts is very much questionable. Large electronic companies, being extremely efficient at moving up an evolutionary path such as semiconductor microelectronics, have serious problems with adapting revolutionary (*disruptive*) technologies like nanoelectronics. As a

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result, the substantial resources thrown onto the problem by the companies, some states, and federal government (within the \$1B/year-scale National Nanotechnology Initiative) are not, in my humble opinion, being spent effectively. Most of this money goes to groups studying various nanoscale objects (carbon nanotubes, semiconductor nanowires, DNA molecules, you name it) with little or no attempt to understand how exactly these objects would work as electron devices, and how these devices might be incorporated into an integrated circuit. It comes without saying that at such approach the vital questions about the possible fabrication cost and performance of future nanoelectronic circuits may not be even asked, leave alone answered.

Fortunately, the past year evidenced the emergence of a more systematic approach to nanoelectronics by a few (for now, just few) academic and industrial groups. Such approach naturally starts with the determination of the main reasons for the anticipated crisis. In contrast to what some industry captains declare, it is certainly the exponentially growing fabrication tool cost, dominated by that of circuit patterning equipment. Indeed, the workhorse device of CMOS circuits, the silicon MOSFET, requires an accurate lithographic definition of several dimensions including the length and width of its conducting channel. As these devices key are scaled down, arising quantum mechanical effects require the definition to be much more precise, which in turn requires much more expensive lithography tools. At some point, the scaling will start bringing diminishing returns. (The reason why this situation is not evident to everybody in the electronics industry is that the major chipmakers had outsourced the development of better patterning techniques to the fabrication equipment producers long ago, and right now those companies are probably not very interested in revealing the real, rather gloomy situation with tool progress to their customers.)

Another necessary component of the systemic approach to the microelectronics is a candid estimate of nanoelectronic devices. Unfortunately, such evaluations show that the nanodevices comparable in their functionality to silicon MOSFETs either run into similar fabrication problems, or cannot be assembled into integrated circuits, or both. The much-heralded *bottom-up* approach (e.g., device self-assembly) also has not given any encouraging results yet.

Fortunately, among all this doom and gloom there is a glim of hope. During the past several years, several groups, including our Stony Brook team, have simplified the decade-old idea of hybrid CMOS/nanoelectronic circuits in which the CMOS stack is augmented with a back-end nanoelectronic add-on. Most recent work in this field is focused on nanowire crossbar add-ons, with simple bistable two-terminal devices formed at each crosspoint, and area-distributed CMOS/nano interfaces – see, e.g., the detailed review article by D. B. Strukov, and a brief write-up by R. S. Williams in this collection, and references therein.

The basic idea of such hybrid circuits is to combine the advantages of CMOS technology (including its flexibility and high fabrication yield) with the enormous density of simple (two-terminal) nanodevices which may be fabricated

reproducibly, at reasonable cost, and naturally incorporated into the nanowire crossbar fabric. However, the main motivation for the hybrid circuit concept is that the nanowire crossbars, including the crosspoint devices, may be fabricated using advanced patterning techniques (such as nanoimprint, EUV interference lithography, block-copolymer lithography), while removing from these techniques the requirement of precise layer alignment. It is believed that the removal of this burden may enable, within the next 15–20 years, an improvement of the resolution of these techniques down to a few nanometers.

Recent detailed simulations have shown that the hybrid circuits with such fine features (though employing much larger MOSFETs fabricated using the ordinary photolithography) may provide at least a two-orders-of-magnitude advantage over purely CMOS ICs in such basic metrics as memory density, logic delay-by-area product, and image processing speed, at manageable power density and high defect tolerance. This leading edge is equivalent to the extension of the Moore's Law progress of microelectronics by approximately 10–15 years beyond the "red brick wall".

Simulations have also shown that the hybrid circuits may be used for operations in the mixed-signal mode as bio-inspired neuromorphic networks ("Cross-Nets") which can be used for performing several important information processing tasks (such as online recognition of a particular person in a large crowd) much more efficiently than digital circuits implementing the same algorithm. Moreover, estimates show that in the long run, CMOL CrossNets may challenge human cortical circuitry in density, far exceeding it in speed, at realistic power. Of course, in order to map these advantages on performing really intelligent information processing tasks, much work has to be carried out by interdisciplinary teams of theoretical neurobiologists, computer scientists, and electrical and computer engineers, but the possible technological and societal impact of such development may hardly be overestimated.

Of course, it may happen that other approaches to nanoelectronics will prove to be more fruitful than the hybrid circuit concept. However, I am confident that only the systemic approach to the problem, taking into account all its aspects, may lead us to success. Let me hope that this collection will be an important step in this direction.

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