

# Preface

Tutorial lectures given by world-renowned researchers have become one of the important traditions of the first two days of the *Nano and Giga Challenges* (NGC) conference series. Soon after preparations for the first forum in Moscow, Russia, had begun, the organizers realized that publication of the lectures notes from NGC2002 would be a valuable legacy of the meeting and a significant educational resource and knowledge base for students, young researchers, and experts alike. Our first book was published by *Elsevier* and received the same title as the meeting itself – *Nano and Giga Challenges in Microelectronics* [1]. Our second book, *Nanotechnology for Electronic Materials and Devices* [2] based on the tutorial lectures at NGC2004 in Krakow, Poland, and the current book from NGC2007 in Phoenix, Arizona, have been published in Springer's *Nanostructure Science and Technology* series.

Nanotechnology as the art (i.e., science and technique) of control, manipulation, and fabrication of devices with structural and functional attributes smaller than 100 nm (0.1  $\mu\text{m}$ ) is perfectly suited to advanced CMOS technology. This technology holds the capacity for massive production of high-quality nanodevices with an enormous variety of applications from computers to biosensors, from cell phone to space shuttles, and from large display screens to small electronic toys.

Exponential growth of the number of transistors in commercial integrated circuits (ICs) was first identified as a trend in 1965 by G. Moore, Intel's co-founder. Later recognized as *Moore's law*,<sup>1</sup> this trend has become an imperative and, until recently, almost a religious prophecy as documented in the International Technology Roadmap for Semiconductors (ITRS).<sup>2</sup> However, scaling of transistors and other devices to smaller and smaller sizes, which has provided the basis for this exponential growth, has limits, physical (size of the atoms), technological (lithography) and economic (see articles of K. Likharev and S. Williams), which will be

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<sup>1</sup> The number of transistors that can be placed on a commercial integrated circuit is increasing exponentially, doubling approximately every 2 years: G.E. Moore, *Electronics*, vol. 38, No. 8, 1965.

<sup>2</sup> <http://www.itrs.net/>

reached by CMOS technology in the next decade. The exponential growth will converge into an S-curve, a well-known trend in biology and economics.

Will this pessimistic forecast result in decreasing interest in society (and in funding!) for electronics research? Is any feasible alternative to CMOS technology available in the near future from photonics, molecular electronics, or revolutionary engineering solutions, such as departure from two-dimensional ICs on the surface of silicon wafers to three-dimensional structures? All these *gigantic challenges* and potential *nanotechnology solutions* are actively debated at *Nano & Giga Forums*. We invite you to *google* the date and location of our next meeting and join us in learning, active discussion, information exchange, and networking in the vibrant and dynamic atmosphere of next NGC forum!

The success of the NGC2007 conference in Arizona, which resulted in the publication of this book and in other contributions making up special issues of *Nanotechnology*<sup>3</sup> and *Solid State Electronics*,<sup>4</sup> would have not been possible without generous support from many sponsors and research institutions. We gratefully acknowledge the contributions and support of Arizona State University (conference host and co-organizer), International Science and Technology Center (ISTC), National Science Foundation (NSF), Defense Advanced Research Agency (DARPA), Office of Naval Research, Army Research Office, Computational Chemistry List (CCL), Springer, City of Tempe, STMicroelectronics, Quarles & Brady LLP, Oak Ridge National Lab, Canadian Consulate in Phoenix, Salt River Project (SRP), and many other local, national and international, and individual supporters.

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and president of Nano and Giga Solutions, Inc.

## References

1. J. Greer, A. Korkin, J. Labanowski (eds) *Nano and Giga Challenges in Microelectronics* (Elsevier, Amsterdam, Netherlands, 2003).
2. A. Korkin, E. Gusev, J. Labanowski, S. Luryi (eds) *Nanotechnology for Electronic Materials and Devices*, (Springer, New York, 2007).

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<sup>3</sup> Selected and invited papers from NGC2007 symposium on nanoCMOS technology (guest editors S. Goodnick, A. Korkin, T. Naito, and N. Peyghambarian) published in *Solid State Electronics*, vol. 51, No. 10, 2007.

<sup>4</sup> Selected and invited papers from NGC2007 symposium on molecular and bioelectronics (guest editors P. Krstic, E. Forzani, NJ Tao, and A. Korkin) published in *Nanotechnology*, vol. 18, No. 42, 2007.

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