Full-Wave Simulation of Integrated Circuit Packages on a Parallel Architecture

Erion Gjonaj, Andreas Barchanski, Peter Thoma and Thomas Weiland

Abstract The time domain electromagnetic field simulation based on massive parallelization is presented as a tool for the signal integrity analysis of complex IC packages. The simulations are based on a specialized domain partitioning method which allows for highly balanced parallel computations. As a real-world example the analysis of a large computer chip spreader is performed. Numerical results including signal wave forms and delay times are given.

1 Introduction

With increasing demands on speed and package density in Integrated Circuit (IC) technology, the trend continues to move toward more complex designs and higher operation frequency. In view of the fast development in semiconductor technology, with chip devices of clock speeds close to 4 GHz, the industry is working on interconnects and packages capable of supporting high frequency signals without loss of signal integrity. The traditional design process is based on low frequency models with lumped elements, used within the framework of circuit simulators. However, as the operation frequency is increased and the package dimensions are reduced, field interference effects within the circuitry become important. Typical EMC concerns

Erion Gjonaj
Institut für Theorie Elektromagnetischer Felder, Technische Universität Darmstadt, Schlossgartenstr. 8, 64289 Darmstadt, Germany, e-mail: gjonaj@temf.de

Andreas Barchanski
Institut für Theorie Elektromagnetischer Felder, Technische Universität Darmstadt, Schlossgartenstr. 8, 64289 Darmstadt, Germany, e-mail: barchanski@temf.de

Peter Thoma
Computer Simulation Technology GmbH, Bad Nauheimerstr. 19, 64289 Darmstadt, Germany, e-mail: peter.thoma@cst.com

Thomas Weiland
Institut für Theorie Elektromagnetischer Felder, Technische Universität Darmstadt, Schlossgartenstr. 8, 64289 Darmstadt, Germany, e-mail: thomas.weiland@temf.de

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at high frequencies, such as radiation, larger delays and mutual coupling should be taken into account in the design of modern ICs.

Attempts have been made to account for high frequency effects in the simulation of IC packages. As an example, in [1] a macromodel approach is proposed, in which first the high frequency characteristics (S-parameters) of IC-subnetworks are extracted and then a reduced order equivalent circuit model for the overall system is derived. The validity of such approximations is, however, difficult to be verified over the whole range of device parameters. Additionally, most of the simulation approaches are applied to small and/or simplified parts of IC devices. Therefore, 3D electromagnetic simulation becomes more and more necessary, as package complexity and operating frequencies increase [2]. Because of the geometrical complexity of IC packages containing thousands of through-hole vias and planar signal traces mounted on several layers, it is a widespread belief that a full-wave simulation taking into account all effects and geometric details is impossible. However, recent algorithmic progress makes such simulations possible, and fully reliable. The key concept is the massive parallelization of field solvers. The use of distributed computing provides sufficient computational resources for the simulation of complete ICs in full 3D geometry within short to moderate simulation times.

In this work, a time domain, full-wave simulation procedure and the results obtained for a very complex computer chip spreader are presented. The work is organized as follows: In Sect. 2, the discretization technique used in the simulations, the Finite Integration Technique, is described. In Sect. 3, the parallelization strategy based on a balanced domain partitioning technique is introduced. In Sect. 3.1 the numerical performance of the parallelization algorithm is investigated using a geometrically simple example, while details of the simulated structure are presented in Sect. 4. Finally, in Sect. 5, a signal integrity study, including computed delay time and transmission/crosstalk waveforms is presented.

2 Discrete Maxwell Equations

The framework for the time domain simulations presented here is provided by the Finite Integration Technique (FIT) [3]. The spatial discretization of FIT utilizes a pair of dual-orthogonal staggered grids $(G, \widetilde{G})$. Denoting by $(\widehat{\mathbf{e}}, \widehat{\mathbf{h}})$ the electromagnetic degrees of freedom and by $\widehat{\widetilde{\mathbf{j}}}$ the source currents, the time discrete update equations of FIT read

$$\begin{pmatrix} \widehat{\mathbf{e}}^{n+1} \\ \widehat{\mathbf{h}}^{n+\frac{1}{2}} \end{pmatrix} = \begin{pmatrix} 1 - \Delta t^2 \mathbf{M}_\varepsilon^{-1} \widetilde{\mathbf{C}} \mathbf{M}_\mu^{-1} \mathbf{C} & \Delta t \mathbf{M}_\varepsilon^{-1} \widetilde{\mathbf{C}} \\ \Delta t \mathbf{M}_\mu^{-1} \mathbf{C} & 1 \end{pmatrix} \begin{pmatrix} \widehat{\mathbf{e}}^{n} \\ \widehat{\mathbf{h}}^{n-\frac{1}{2}} \end{pmatrix} - \begin{pmatrix} \Delta t \mathbf{M}_\varepsilon^{-1} \widehat{\widetilde{\mathbf{j}}}^{n+\frac{1}{2}} \\ 0 \end{pmatrix} \quad (1)$$

where the unknowns $(\widehat{\mathbf{e}}, \widehat{\mathbf{h}})$ are the integrals of the electric and magnetic fields along the edges of G and $\widetilde{G}$, respectively. The curl-operators $(\mathbf{C}, \widetilde{\mathbf{C}})$ are of pure topological nature, whereas the metric information obtained by discretization is contained in the symmetric positive definite material matrices, $(\mathbf{M}_\varepsilon, \mathbf{M}_\mu)$. A detailed

description of the FIT method applied in time and frequency domain simulations is found, e.g., in [3].

The compact writing in terms of matrix operators reveals that the only critical computation to be performed is a sparse matrix-vector multiplication. This can be very efficiently implemented, e.g., by employing specialized algorithms which make best use of local memory operations (cf. [4]).

3 Parallization Strategy

The huge amount of degrees of freedom needed for the 3D discretization of the full IC structure can only be handled in a parallel computing environment.

The parallelization model used in this work is based on the distribution of computational tasks and data among a number of memory independent processors (multiple-instruction-multiple-data). In this model, there are three main factors which do affect the efficiency of the parallel computation.

- **Interprocessor communication**: this is the additional overhead in parallel computations related to the necessity of exchanging field data between the processors involved in the simulation.
- **Workload per processor**: ideally, the computational time needed to perform its own task by an individual processor.
- **Workload balancing**: the workloads assigned to each processor need to be well balanced, in order to avoid idle times of the less loaded processors, waiting for the ones with heavier workloads to finish their task.

We perform a geometric partitioning of the computational domain into subdomains, such that the above criteria are optimally taken into account. Each subdomain is assigned to a single processor (node in the cluster) which is responsible for the solution of (1) within the subdomain (cf. [5]).

The idea of the parallel partitioning approach is shown schematically for a three-node cluster of computers in Fig. 1. Starting with the whole computational domain, an orthogonal recursive domain bisection is applied. The procedure results in a binary tree structure, whose internal nodes are *intermediate* subdomains, whereas the leaf nodes correspond to the *active* subdomains which are used in the computation. Each processor is responsible for two types of operations:

- performing the electromagnetic update equations (1) for the grid cells contained within the own subdomain, and
- exchanging field data with processors assigned to neighboring subdomains.

Because of the local nature of the discrete operators in (1), only field degrees of freedom residing at the boundaries of active subdomains need to be exchanged between the processors. In particular, for regular hexahedral meshes, the orthogonal decomposition approach yields the smallest number of such boundary cells and, therefore, it minimizes the communication overhead in the simulation. The recursive bisection procedure is performed on the basis of *computational weights*, W_i, which are

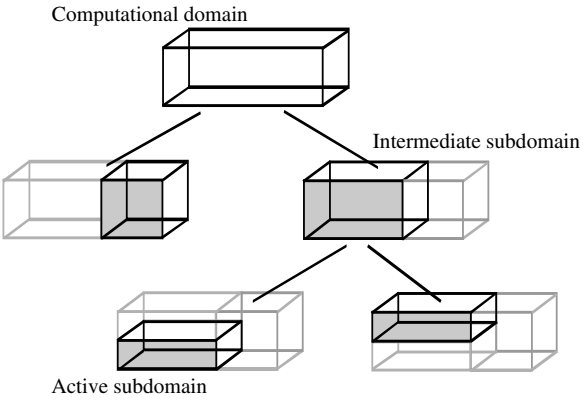

Fig. 1 Example of the orthogonal domain bisection procedure on a three-node cluster

assigned to each grid cell and represent the total number of floating point operations needed for a time-update of the cell's unknowns. The total computational load associated with an intermediate subdomain is, thus, $W = \sum W_i$, where the summation includes only grid cells contained within the subdomain. If the subdomain has to be distributed among N processors, the bisection boundary is chosen such that

$$\frac{W_{\text{left}}}{W_{\text{right}}} = \frac{N_{\text{left}}}{N_{\text{right}}}, \tag{2}$$

with

$$\begin{aligned} N_{\text{left}} &= \frac{N}{2} \\ N_{\text{right}} &= \frac{N}{2} \\ N &= N_{\text{left}} + N_{\text{right}}. \end{aligned} \tag{3}$$

where $(W_{\text{left}}, W_{\text{right}})$ and $(N_{\text{left}}, N_{\text{right}})$ are the computational weights and the number of processors, respectively, associated with the two subdomains created by subdivision.

The above algorithm allows for an almost ideally balanced distribution of computational workloads. In addition, it can be applied to simulations involving an arbitrary number of processors. Furthermore, by selecting appropriate cell weights in (2), well balanced parallel computations can be performed on *arbitrary, heterogeneous clusters*.

3.1 Test Example

In order to assess the performance of the algorithm, a simple example is considered. It consists of a rectangular cavity homogeneously filled with air and discretized with

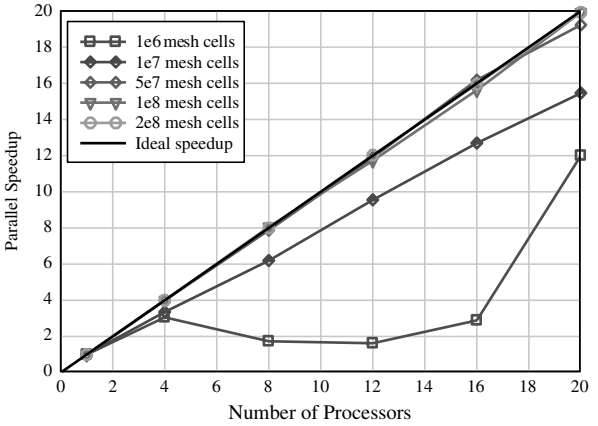

Fig. 2 Parallel speedup of the partitioning algorithm for different grid sizes and number of processors

a regular hexahedral mesh. Different discrete models, leading to meshes containing between 1 million and 200 million mesh cells, were used in the simulation tests.

The algorithm's performance in terms of parallel speedup, for the different grid sizes, is demonstrated in Fig. 2. The speedup curves show a perfect behavior, lying almost on the theoretical limit. Exceptions are the "tiny" discrete models of 1 million and 10 million grid cells, respectively. As expected, in these cases the interprocessor communication dominates the computational workload of the individual processors. Since the interprocessor communication increases with increasing number of processors, the performance speedup for the small models deteriorates faster than for the larger ones. The simulations shown in Fig. 2 were performed on a 20-node cluster of 3.4 GHz Intel processors and a conventional 1 Gbit/s Ethernet network, using the MPI standard. Note that, in this simple performance test neither absorbing boundaries nor conductivity currents or excitation signals were considered. Such additional computations may slightly affect the parallel performance in real-world simulations.

4 The IC Package

The package considered in the following is a multilayer computer chip spreader. It connects the semiconductor die with its larger support which in turn is soldered into the printed circuit board (PCB). A schematic view of the stack-up is shown in Fig. 3. The structure contains 8 metallization layers embedded into a dielectric substrate. The metallization is copper and the dielectrics used for the substrate are ABF-GX13 ($\varepsilon_r = 3.2$) and BT-679FG ($\varepsilon_r = 4.2$). Most of the signal traces propagate on the layer FC3. The signal is connected on the top layer to these traces by via and then routed almost directly to the solder points on the PCB side of the package.

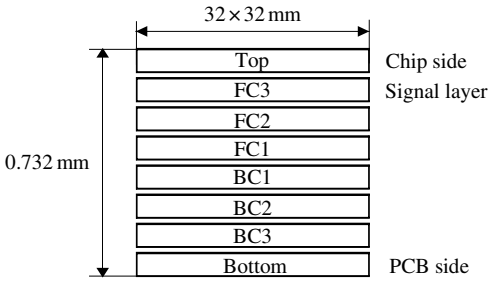

Fig. 3 Schematic view of the 8 metallization layers and the total dimensions of the package

The geometry of the package was provided to the authors by the IBM Thomas J. Watson Research Center [6] in form of a Cadence Allegro design layout. The data consisted of more than 40,000 2D-polygonal elements (pins, vias, traces, etc.). The CAD model of the fully 3D geometry was extracted from these data using the CST STUDIO SUITE software [7]. This step turned out to be the most challenging in the simulation procedure. Besides the huge size of the data to be processed, the main difficulty in extracting the geometry results from the errors contained in the input data. Typically, Allegro design layouts contain a small but non-negligible number of self-intersecting polygons. These errors had to be fixed manually, with considerable effort, in order to generate a consistent 3D-geometry description. Figure 4 shows the complete view of the 3D package geometry.

The geometrical complexity of the device is demonstrated in the detailed view of Fig. 5. In order to give an idea about the proportions: the approximate area of the zoomed-in section is 2×3.5 mm, representing only about 0.7% of the total device area. In the Figure, the 6 signal traces used in the simulations (see Sect. 5) are shown in blue/dark color. The width of these traces is $25\,\mu$m with a minimum trace-to-trace

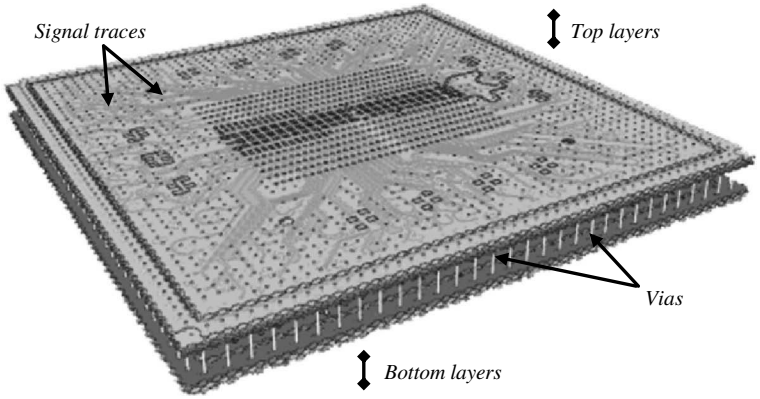

Fig. 4 Complete view of the package including the 8 layers, signal traces and vias (the vertical size is not to scale as the structure is extremely flat)

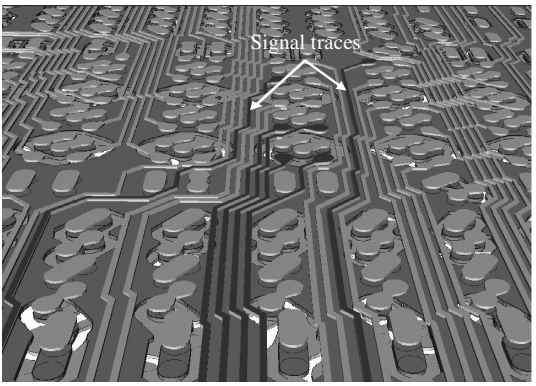

Fig. 5 Chip side view of a small section of the package. Six selected signal traces, used in the simulations are shown in blue/dark color

spacing of only $20\,\mu$m. The thickness of the single layers varies between $13\,\mu$m and $21\,\mu$m. The overall aspect ratio of largest-to-smallest geometrical dimension is, thus, higher than 1000:1. As shown in Sect. 5, in order to resolve all geometrical details of the structure, a huge computational mesh of several hundred millions of cells is needed. Simulations of this size can hardly be handled on a sequential computing platform.

The third step in the geometric modeling phase includes meshing, i.e., the recognition of the electromagnetic material distribution by the discretization grid and the generation of the material operators in (1). Because a huge number (of several hundred millions) of mesh cells are needed in the simulation for resolving the geometrical details of the structure, this step can be hardly performed on a sequential computing platform.

On the other hand, since meshing is a purely local operation, it can be very effectively implemented in a parallel scheme. Using the domain partitioning approach of Sect. 3, only the fractions of geometry data and mesh cells relevant to each partition are actually used in local computations. Thus, the more processors are included in the parallel simulation, i.e., the smaller are the partition domains the less critical becomes the meshing procedure (cf. also Table 1).

Table 1 Main parameters of the full-wave simulation

Parameter	Value
Signal rise time	39.5 ps
Signal duration	600 ps
Total number of cells	594,000,000
Total number of unknowns	3,564,000,000
Number of processors	20
Peak memory/processor	7.5 GB
CPU time for meshing	$\approx$ 3 hrs
Simulation time/signal	$\approx$ 68 hrs

5 Simulation and Results

The full IC package was discretized using a regular Cartesian grid. In order to resolve the smallest geometrical details of the structure, a minimum grid step of $8\,\mu$m in the vertical plane was used. In the horizontal plane a uniform grid of $10\,\mu$m step was applied. This choice assured a discretization with 2–3 grid cells within the cross-section of the signal traces ($25\,\mu$m in width), which are the most critical geometrical components in the simulation. The whole discretization procedure resulted in a grid of ca. 600 million cells distributed mainly along the metallization planes.

An exemplary domain partitioning of the model on a 15-node cluster is shown in Fig. 6. The distribution of active partitions is seemingly irregular. However, all partitions do contain (approximately) the same number of mesh cells, as required for parallel coherence.

Table 1 gives a summary of the main parameters in the actual simulations. Note that only 3 hrs were needed in the meshing phase as compared to 38 hrs needed in the transient simulation. This figure scales down linearly with the number of processors used in the simulation.

Figure 7 shows the normalized absolute value of the electric field on the signal layer (FC3) shortly after the excitation is applied on line 1. Apart from the signal propagation along the trace, the near-end crosstalk to one of the neighboring pins is clearly seen.

Figure 8 shows the recorded wave forms obtained when exciting trace 2. The displayed signals are the input signal, the transmitted signal, as well as the near-end (NE) and far-end (FE) cross-talks with traces 3 and 6.

Figure 9 shows similar voltage curves when the input line is trace 6. The signal delay time seen at the half-widths of the signal rise times for the input and transmitted curves, respectively, amounts to 119.9 ps, which is in good agreement with

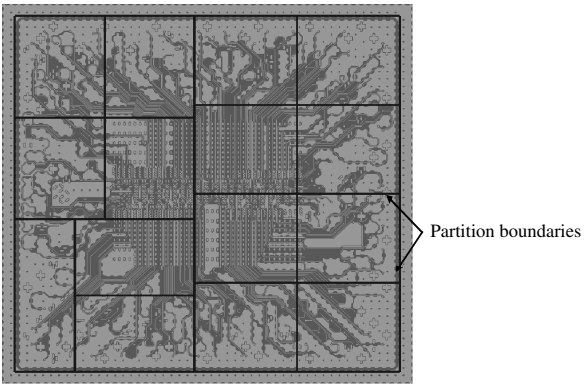

Fig. 6 Exemplary domain partitioning of the model on a 15-node cluster. The partition boundaries are shown as black lines

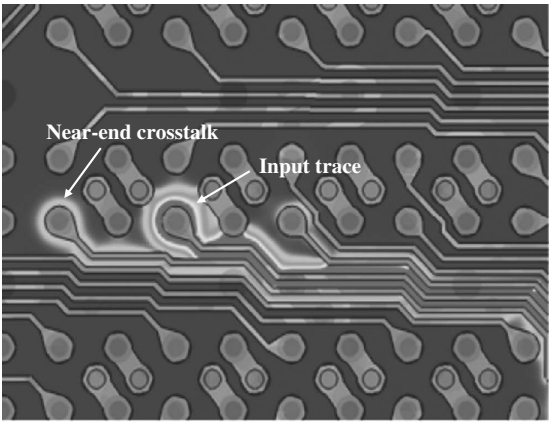

Fig. 7 Electric field strength (a.u.) on the FC3 layer, 30 ps after the start of the pulsed excitation at trace 1

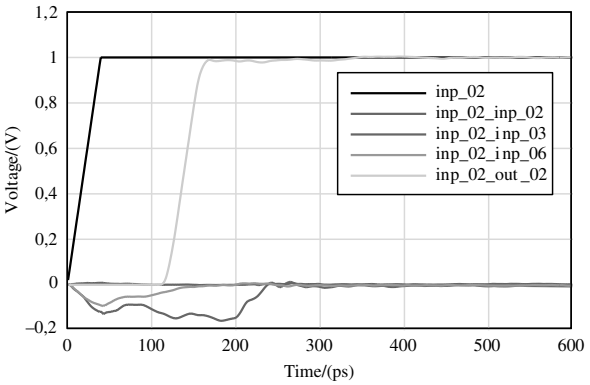

Fig. 8 Some of the voltage profiles at the input (labeled "inp 02 inp 0x") and output ("inp 02 out 0x") ports when the excited line is trace 2

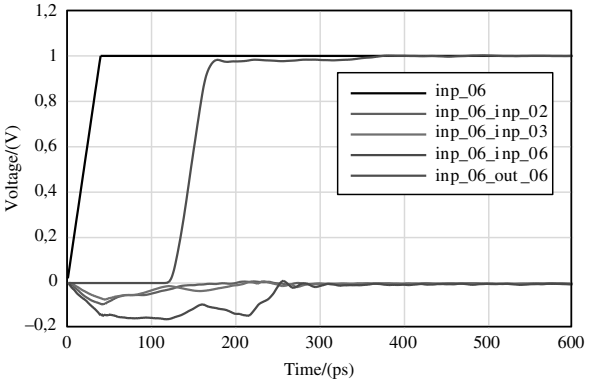

Fig. 9 Some of the voltage profiles monitored at the input and output ports when the excited line is trace 6

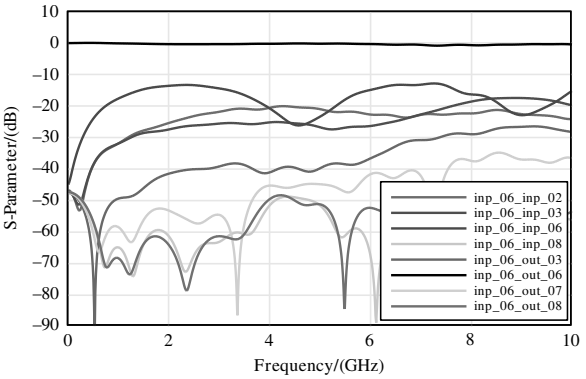

Fig. 10 S-parameters extracted from a time domain simulation with a pulsed excitation using trace 6 as the excitation line

the measured value of 119.3 ps [6]. Additionally, note the reciprocity of the voltage profiles obtained, e.g., for the near-end crosstalk between traces 2 and 6.

Figure 10 shows the S-parameters of the device in the range from 0 to 10 GHz using trace 6 as the excitation line. The far-end coupling is also here (except for trace 3) negligible. The strength of the near-end coupling with traces 2 and 3, however, is close to 20 dB. This effect becomes slightly stronger with increasing frequency.

6 Conclusion

A large scale, full-wave simulation of a complete IC package is presented. The use of distributed computing with a specialized domain partitioning approach provides sufficient computational resources for overcoming the simulation burdens related to the geometrical modeling and to the huge number of field degrees of freedom involved. In view of the ever-increasing need for high speed/high density packaging, the method has the potential of becoming a standard tool in the design of modern ICs.

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