Chapter 5
Flexible Transition Metal Oxide Electronics and Imprint Lithography

Warren B. Jackson

5.1 Introduction

The previous chapters have discussed inorganic low-deposition temperature materials suitable for flexible applications, such as amorphous and nano-crystalline-silicon (Si) and organic conductors. This chapter presents the results of a recently developed inorganic low-temperature materials system, transition metal oxides (TMOs), that appears to be a very promising, new high-performance flexible electronic materials system. An equally, if not more, important part of this chapter, is the presentation of self-aligned imprint lithography (SAIL) a new fabrication method for flexible substrates that solves the layer-to-layer alignment problem.

The new *materials* system is TMO based consisting of one or more transition metals and oxygen. Some of the more common examples include zinc oxide, zinc tin oxide (ZTO), indium gallium zinc oxide (IGZO) and zinc indium oxide (ZIO). These low-temperature amorphous materials can form the active material for transistors with a performance that significantly exceeds that of amorphous and nanocrystalline Si and approaches that of larger grain poly-Si without the complexities and uncontrolled variability of polycrystalline materials. Thus, this technology can be used to drive organic light-emitting diodes (OLEDs) as well as create electronic circuits, such as shift registers, ring oscillators, and multiplexers on chip. An added feature is the possibility of creating transparent electronics with such materials systems. The entire transistor including the electrodes and the active material can have visible transmittances of 70% or greater. Thus, for applications such as displays, the active electronics would not impact the visual appearance of device and the fill factor of displays with such electronics could approach 100%. Finally, there is the possibility of creating p-type transistors that would permit fabrication of complementary metal oxide semiconductor (CMOS) circuits for flexible applications. Hence, the TMO material system possesses a number of intriguing new possible applications.

W.B. Jackson (✉)
Hewlett-Packard Laboratories, 1501 Page Mill Road, Mail Stop 1198, Palo Alto, CA 94304, USA
e-mail: warren.jackson@hp.com

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For the purposes of this chapter, the most remarkable feature of the TMO transistors is that these features and performance can be achieved in devices with a maximum processing temperature that is compatible with flexible polymer substrates, such as polyimide (Glass transition temperature (T_g) = 300°C) and polyethylene naphthalate (PEN) (T_g = 200°C). Although most metal oxide work published thus far has been accomplished on higher temperature and rigid substrates, such as glass and c-Si, recent work has demonstrated large mobilities for flexible metal oxide transistors using photolithography and standard batch etching processes. However, flexible substrates are not dimensionally fixed during processing, making it virtually impossible to have precise layer-to-layer micron-scale alignment for large dimensionally variable substrates. This important problem of layer-to-layer registration on flexible substrates has been solved using SAIL, a solution that extends the TMO technology as well as amorphous and poly-Si to higher performance short channel devices.

This chapter presents the results in the field of TMO transistors relevant for the emerging field of flexible electronics in the following sections:

(1) A brief discussion of the history of work and background information in the general area of metal oxide transistors relevant for flexible electronics.
(2) The general properties of some of the leading TMO materials.
(3) The device structures used in TMO and flexible electronics along with a description of SAIL
(4) One of the most important sections presents SAIL and amorphous silicon (a-Si) results, indicating that the method can fabricate working devices.
(5) Resulting TMO thin-film transistors (TFTs) on rigid substrates using shadow masks and photolithography on both flexible and rigid substrates along with TMO SAIL results on rigid substrates
(6) Finally, future areas of research for improved large-area flexible electronics.

5.2 Previous Work

TMO materials have been used in transistors for quite some time. One of the first ZnO transistors was made in the 1960s [1]. However, little progress ensued using TMOs as semiconductors although ZnO found uses in surface acoustic devices [2], varistors [3], transparent PN diodes [4], and as a transparent conductor [5]. Interest in ZnO as transistors was revived in about 1997 by Prins et al. [6] and later in Kawasaki et al. and Ohtomo et al. [7, 8], where transistors with mobilities of 100 $cm^2\ V^{-1}\ s^{-1}$ were fabricated using spin-on glass as the insulator on glass substrates. Subsequently, there have been many different experiments investigating various aspects of metal oxide transistors.

The current interest in TMO transistors started with Ohya et al. [9] and in the thesis by R. Hoffman 2002 [10], Masuda [11], Nomura [12], Hoffman [13], Nishii

[14], and Carcia [15]. These references led to the current interest in TMO transistors and established convincingly that these materials not only had high Hall mobilities but could actually produce high-performance transistors. Typical mobilities for these initial efforts were on the order of 0.1–1 $cm^2\ V^{-1}\ s^{-1}$ when fabricated using low-temperature dielectrics and 80 $cm^2\ V^{-1}\ s^{-1}$ for high-temperature thermal oxide dielectrics on c-Si. The latter work indicated that transistors with performances approaching that poly-Si were possible using TMO materials as the active layer. Following this initial group of publications, the field has expanded greatly with dozens of papers detailing various aspects of TMO transistors. Various methods of deposition, dielectrics, and TMO combinations were investigated. A list of many of the various results is summarized in Table 5.1 and in [17].

The primary emphasis of most TMO transistor work is to create transparent semiconductors. One important result was that high-performance ($\mu = 20\ cm^2\ V^{-1}\ s^{-1}$) transparent transistors could be fabricated at room temperature on glass using silicon oxynitride dielectrics [21] and using atomic layer deposition (ALD) of Al_2O_3/TiO_2 superlattice dielectric [36] (Fig. 5.1). The resulting output curves are very flat and the on–off ratio is very good. This work demonstrated that high-performance TMO transistors on flexible substrates are possible.

Another theme of research in the TMO field is the expansion of candidate TMO material systems used in transistors. The range of viable transistor materials has been enlarged to include materials such as ZnO, ZnSnO, ZnInO, ZnInGaO, and InGaO among others (see Table 5.1). The oxide systems have achieved different levels of performance at a variety of maximum fabrication temperatures and have unique attributes that make them suitable for various applications. The thrust of this work is to decrease the high-temperature annealing step required to reduce the carrier concentration of the TMO. The initial ZnO transistors had limited performance unless the samples were subjected to anneal temperatures exceeding 400°C. The addition of Sn to ZTO has produced stable transistors with reasonable performance using anneal temperatures of 210–250°C [13, 21]. This temperature range is compatible with polyimide but not typical transparent substrates, such as PEN and polyethylene terephthalate (PET). The addition of In into the ZIO devices and IGZO (the addition of Ga) has lowered the temperature needed to produce high-performance devices to below 200°C [21]. Unfortunately, the addition of In and the low temperature of annealing appear to introduce instabilities in the devices that remain poorly understood. A summary of some of the more prevalent material systems and their properties is shown in Table 5.2. A general summary of the trends is that the inclusion of In, Ga, and Sn lowers the maximum processing temperature needed to obtain higher mobilities in part because of the generally higher diffusivities of these metal cations.

Most of the previous TMO work has emphasized the transparency and high mobilities that could be obtained using TMO transistors. For the purposes of this book, the work relating to TMO for flexible electronics is more important. Some of the first work that explicitly addressed issues relevant for the application of TMO to flexible electronics, which reduced the maximum processing temperature of ZnO to 150°C, is Ref. [20]. Later this group produced ZnO transistors on

Table 5.1 Summary of various TMO transistors with properties

Reference No.	Oxide	Substrates	Max. temp (°C)	Deposition method	μ ($cm^2\ V^{-1}\ s^{-1}$)	On–off ratio	V_t (V)	Gate dielectric	Contacts
[11]	ZnO	c-Si	450	PLD	0.03–1	10^5	(−1)−2.5	SiO_2/SiN	
[13]	ZnO		700	IBS	0.3–3	10^7	10–15		
[12]	$InGaO_3(ZnO)_5$		1,400	PLD	80	10^6	3	HfO_2	
[15]	ZnO		25	RMS	0.3–2	10^5–10^6	0		
[16]	ZnO		300	PLD	<4				
[18]	ZnSnO	Glass	600	RMS	14	6×10^6	−4.6	Al_2O_3–TiO_2	
[19]	ZnSnO	Glass	300	RMS	5–15	10^7	0–15	ATO	
[6]	SnO2:Sb							$PbZr_{0:2}Ti_{0:8}O_3$	
[10]	ZnO	Glass	600	IBS	0.3–2.5	10^7	10–20	ATO	
[14]	ZnO	Glass	150–300	PLD	7	10^7		$SiN/CaHfO_x$	
[9]	ZnO								
[20]	ZnO	Polyester polyimide	RT	RMS	0.4	10^4	7.5	fluoropolymer dielectric	
[20]	ZnO	Glass	RT	RMS	28	3×10^5	19	SiON	GZO
[21]	ZnO	Glass	RT	RMS	20	5×10^5	1.8	SiON	
[22]	ZnO	Polyimide	<120	EB	50	10^5	3.2	Al_2O_3	
[23]	ZnO		750	PLD	12	10^3	–3	$SrTiO_3$	
[24]	ZnO	Si	250	MOCVD/ ALD	0.95	10^6	1.7	SiO_2/AlO_x by ALD	
[25]	ZnO	n-c-Si	125, 200, 300, 400, 450	RMS	17	10^5	6	HfO_2, Al_2O_3	
[26]	ZnSnO	Polyimide	250	RMS	14	10^6	−17	SiON, SiO_2, SiN	
[27]	ZnSnO	c-Si	300	RMS	20	10^6	0	SiO_2	
[28]	ZnSnO	Polyimide	250	RMS	14	10^6	−8.5	SiON, SiO_2, SiN	ITO

(continued)

Table 5.1 (continued)

Reference No.	Oxide	Substrates	Max. temp (°C)	Deposition method	μ ($cm^2\ V^{-1}\ s^{-1}$)	On–off ratio	V_t (V)	Gate dielectric	Contacts
[29]	IGZO	PET	RT		8	10^3		Y_2O_3	
[30]	ZIO	c-Si	RT	RMS	20	10^8	−3.2	SiO_2	
[31]	ZnO	Glass	RT	RMS	20	10^5	21	Al_2O_3 TkO_3	
[32]	Tetracene	Mylar	RT	EV	5×10^{-4}			Mylar	
[33]	Organic	Mylar	RT	EV	1×10^{-4}	10^4		Mylar	
[34]	Organic	Mylar	RT	EV	1×10^{-4}	10^4		Mylar self-aligned	
[35]	IGZO	YSZ	350	R-SPE	80	10^8	5	HfO_4	IZO
[36]	ZnO	glass	RT	RF	27	3×10^5	19	Al_2O_3 TiO_3 e ALD	
[37]	IGZO	PET	RT	PLD	10	10^6	3.2	Y_2O_3	ITO

PLD,Pulsed Laser Deposition; IBS,Ion Beam Sputtering; RMS,Radio frequency Magnetron Sputtering; EB,Electron Beam Sputtering; MOCVD,Metal-Organic Chemical Vapor Deposition; ALD,Atomic Layer Deposition; R-SPE, Reactive solid phase epitaxy; EV,evaporation.

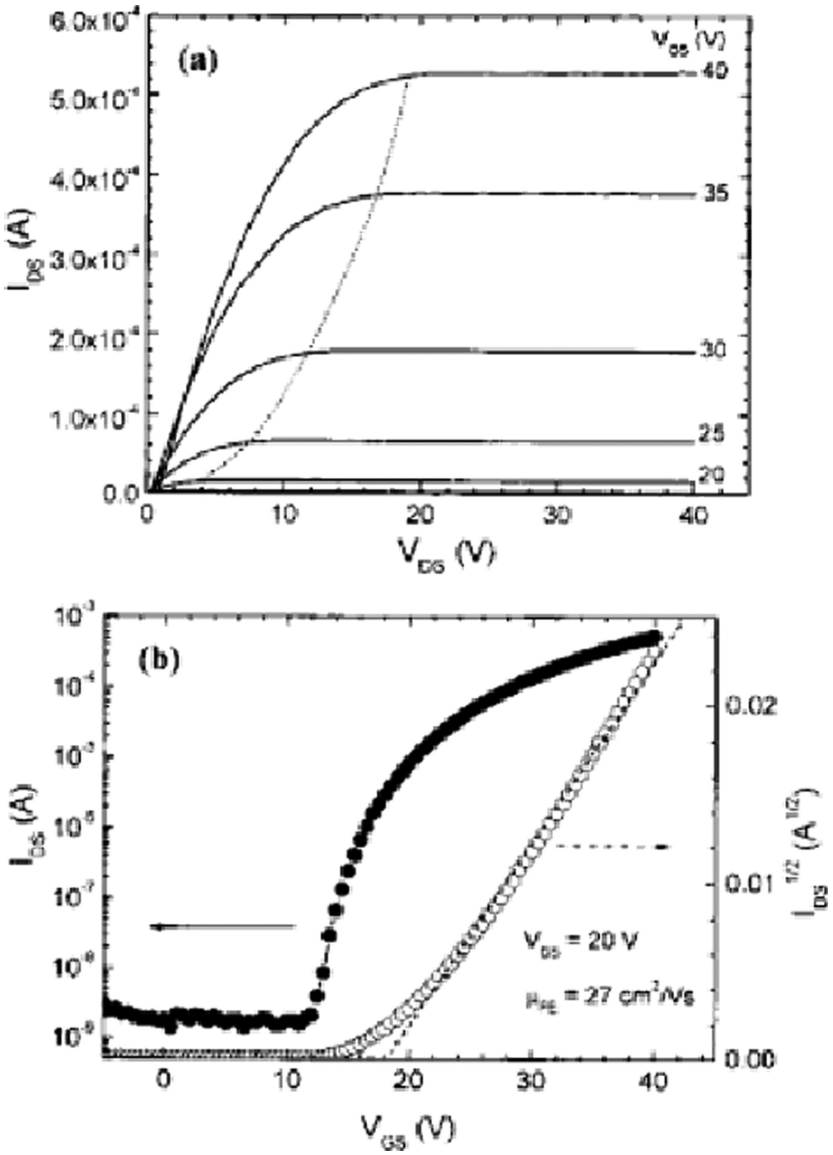

Fig. 5.1 ZnO transistor characteristics on an ITO-coated glass, ALD-deposited Al-Ti-O dielectric, and GZO contacts from [36]. W/L = 1.4

polyester and polyimide substrates [15, 22] using organic fluoropolymer dielectrics and obtained transistors with field effect mobilities of about 0.4 $cm^2\ V^{-1}\ s–^1$, on–off ratios of about 10^4, and threshold voltages (V_T) of 7.5 V. They then replaced the fluoropolymer dielectric with the inorganic dielectric of atomic layer deposited Al_2O_3 and obtained devices with mobilities of 50 $cm^2\ V^{-1}\ s^{-1}$, on–off ratios of

Table 5.2 Electronic properties of Zn TMOs

Material	E_g (eV)	μ_H ($cm^2\ V^{-1}\ s^{-1}$)	ρ (Ω cm)	n (carriers cm^{-3})	References
ZnO	3.2–3.3	5–50	10^{-4}	10^{21}	[38–40]
$ZnSnO_3$	3.5	7–12	5×10^{-3}	10^{20}	[40–42]
Zn_2SnO_4	3.3–3.9	12–26	$1–5\times10^{-2}$	$6–30\times10^{18}$	[43–45]
$Zn_2In_2O_5$	2.9	12–20	$1–4\times10^{-3}$	3.6×10^{20}	[43, 40, 46]
ZnInGaO	3.0	10		10^{20}	[29]

10^5, and $V_T = 3.2$ V. These devices were deposited using electron beam evaporation through shadow masks. The ALD deposited dielectrics of these transistors are difficult to migrate to a production environment. More recently, ZTO transistors deposited on polyimide using shadow mask patterning have achieved mobilities of 15 $cm^2\ V^{-1}\ s–^1$, on–off ratios of 10^6, on-currents as high as 1.5 mA, and threshold voltages of -17 V [26]. These devices have been obtained using typical production compatible dielectrics such as radio frequency (RF) discharge produced SiN, SiO_2, and SiON, and shadow mask patterning, and processing temperatures below 250°C. This work highlighted the need for appropriate contacts such as indium tin oxide (ITO) or Al for high-current applications. Recent work has also been made on applying more flexible substrate-appropriate patterning methods such as SAIL for ZTO [28]. Issues such as channel length scaling and contact resistance have been investigated.

5.3 Properties of Transistor Materials

5.3.1 Semiconductors

The TMO materials space has many possible combinations of transition metals and oxygen each with a unique combination of electronic and materials properties. Many of these combinations in the TMO material space have not been fully investigated particularly the various ternary compounds (those with two or more transition metals). The Zn-based compounds however, are currently generating the most interest and serve as a good representative subclass of the larger TMO group.

The properties of ZnO and related compounds are shown in Table 5.2. The valence band is formed by hybridized Zn 4*d* levels and O 2*p* levels. The conduction band is formed predominately by Zn 4*s* levels. The bandgap is direct and has a value of 3.2–3.3 eV for ZnO and increases to 3.5–3.9 eV with the addition of Sn (Table 5.2). The addition of In tends to lower the bandgap to 2.9 eV. These values are large enough that the material is transparent without much coloration. Hence, they make good candidates for transparent electronics.

The properties of TMOs make them uniquely suited for flexible electronics where low-temperature non-single crystalline materials must be used. The Hall mobility

(μ_H) of single crystalline ZnO is 200 $cm^2\ V^{-1}\ s^{-1}$ and the saturation velocity is large, making high-mobility devices feasible. The measured Hall mobilities in amorphous TMOs are around 5–50 $cm^2\ V^{-1}\ cm^{-1}$, and the achieved field effect mobilities are roughly of comparable magnitude (Table 5.2). With field effect mobilities of 10–100 $cm^2\ V^{-1}\ s^{-1}$, milliamp on-currents for flexible devices are obtainable using typical TFT parameters. The high mobility for electrons in the disordered amorphous TMOs arises because of the overlap of the nondirectional 4**s** orbitals of Zn (or other transition metal cations) creating a conduction band regardless of the angle between nearest neighbors (Fig. 5.2). Hence, the mobility is relatively unaffected by

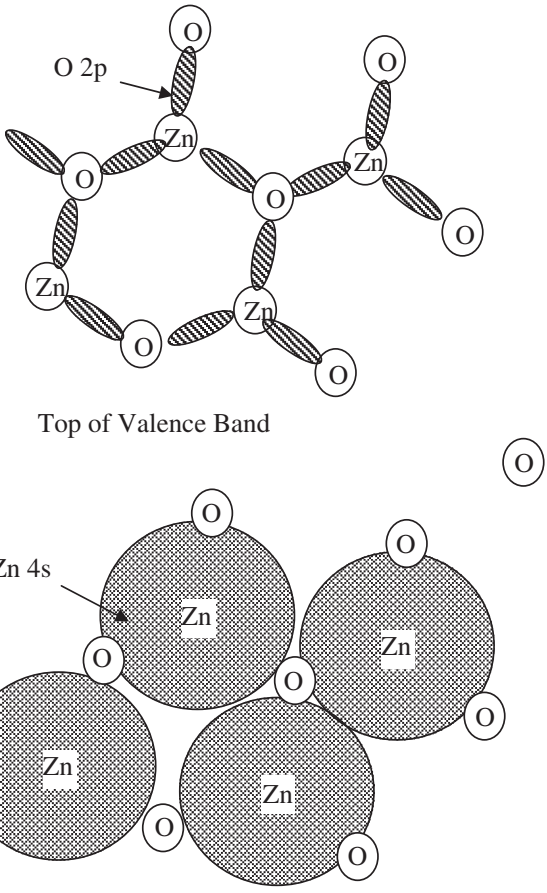

Fig. 5.2 Schematic of electron wavefunction structure for the *top* of the valence band (primarily O 2**p**) and the *bottom* of the conduction band (Zn 4**s**). The large overlap with neighboring Zn and spherical symmetry of the Zn 4**s** levels minimize sensitivity to disorder for the conduction band

Table 5.3 Various miscellaneous properties of ZnO [50]

Density (g cm^{-3})	5.6
Dielectric constant	8.6
Refractive index	2.0
Average thermal expansion Coeff. (/K)	4×10^{-6}

bond angle disorder. Moreover, the ionic nature of the transition metal oxide bonds causes the bonds to be less directional than the typical covalent bonds found in the usual Group IV or III–V semiconductors. Therefore, the large bond angle distortions found at grain boundaries are less apt to result in grain boundary gap state defects. The lack of gap states associated with deformed bonds results in large subthreshold slopes and small turn-on voltages in low-temperature transistors.

A further consequence of the lack of bandgap states and high electron mobility is that the materials often can be easily degenerately doped n type yielding small resistivities, ρ, below 10^{-2} (Ω cm) (Table 5.2). The doping of ZnO occurs by substitutional dopants, Zn interstitials, O vacancies, and/or interstitial H. The typical substitutional dopants include N and P. Oxygen vacancies are used to make the materials highly conductive for use as transparent electrodes for solar cell and photosensor applications. The oxygen vacancies can readily be created by sputtering in an O poor atmosphere. In fact, in TMO transistor fabrication, care must be taken to keep the O-vacancy concentration low so that the channel is sufficiently resistive for enhancement mode transistor operation [15, 22]. There is increasing evidence that the O vacancies may be somewhat mobile resulting in some long-term device instabilities to be discussed later.

There also is evidence that H interstitials act as n-type dopants [47–49]. Exposure of semiconducting ZTO to an H plasma results in a significant enhancement of the conductivity while exposure to an Ar or O plasma does not. Moreover, the H diffusion rate is large even at 200°C. Thus, unintentional H doping during fabrication etching is a concern and must be controlled.

Other useful parameters for ZnO are shown in Table 5.3 [50]. Note that the dielectric constant is somewhat lower than that of a-Si. The values for other TMO are generally similar in magnitude.

5.3.2 Dielectrics

Dielectrics are often one of the most critical materials necessary for a transistor technology. In most electronic applications, shorts are extremely undesirable defects, particularly in array applications. Shorts not only cause the shorted device to fail but often result in failure of any connected device and cause an unacceptable power drain. They also mask failures by other devices. In addition to the highly

Table 5.4 Various dielectrics used in TMO transistor technology [10, 18]

Insulator	E_g (eV)	Relative dielectric constant	Breakdown field (MV/cm)
SiO_2	11	3.8	6
SiN	9	7	9
Al_20_3	9.5	8	3.5–6
$BaTa_2O_5$		22	3.5
HfO_2	5.8	16	3
Ta_2O_5	4.6	24	1.5–3
TiO_2	3.7	60	0.2
Y_2O_3	5.6	12	4
ZrO_2	5	19.8	

deleterious effect of shorts, typical large-area applications consist of many devices and crossovers requiring a highly reliable dielectric. Dielectrics that have been successfully used for TMO TFTs are included in Table 5.4 [10, 18]. The dielectrics currently being used in large-area electronics, such as SiO_2 and SiN work reasonably well for TMO devices. Typically, if SiN is used, a thin SiO_2 buffer layer is used so that the SiN does not directly contact the TMO. One unresolved issue is that the presence of large amounts of H may be one of the problems with SiN in direct contact with the TMO [51]. More recently, evidence has emerged that O vacancies can be created during long-term operation of TMO transistors and result in long-term instability [52–56]. There is possible evidence that the silicon-based oxides are more reactive in creating vacancies. As a result there is interest in less reactive oxides, such as Y_2O_3, Al_2O_3, Ta_2O_5, and HfO_2 dielectrics [25, 29, 30, 36, 12]. These oxides have the advantage of having high dielectric constants as well as possibly generating fewer O-vacancy related instabilities. It is not yet clear whether the instability is actually O vacancies or rather H associated with the various dielectrics or due to the motion of metal interstitials. Hence, low H dielectrics may be necessary to solve the instability problem.

5.3.3 Contact Materials

The contact materials needed for TMO have not been completely investigated at this point. For many TMO systems, the metal−TMO contact has been sufficiently conductive to yield high-current devices. However, as shown in the section below, insertion of an intermediate layer between the metal and the TMO can result in significant decrease in the contact resistance. The metals Al, Ti, and TiW make reasonable contacts capable of making devices with more than 1 μA/(W/L) on-current per W/L. The current can be significantly increased, however, if a layer such as ITO is inserted between the TMO and the metal [26, 28]. In the case of ZTO, the ITO layer at the contact increases the on-current to 10 μA [26, 28].

5.4 Device Structures

The structures used for TMO TFTs on rigid substrates are largely the same as those used in other deposited material systems, such as a-Si. The various structures include the staggered bottom gate, collinear bottom gate, and top gate devices. Because fully versatile reproducible etching of the TMO semiconductors is still being developed, most of the early reported work has involved shadow mask structures and transistors on silicon wafers with thermal oxide. It is only recently that more fully photolithography patterned microstructures have been made.

Continuous Bottom Gate. The most prevalent structure for investigating basic material properties and the device potential of the metal oxide system is using a blanket deposited bottom gate structure (Fig. 5.3a,b). Either a layer of metal or a doped silicon wafer serves as the gate electrode. If a crystalline Si wafer is used, the dielectric is usually a thermal oxide, the source and drain electrodes are patterned on the oxidized Si wafer using either shadow masks or photolithography, and finally, the metal oxide material is deposited through a shadow mask to complete the structure. If the back contact is a continuous metal, the dielectric is a deposited dielectric and the other steps are similar to those of a silicon wafer. The shadow mask is used to define the active material to restrict current flow to a region near the contacts. Variations of this structure include the deposition of materials to improve the contact properties such as ITO or Ti. The contact material must be patterned along with the source and drain prior to deposition of metal oxide active material. Also, the contacts can be patterned first followed by deposition of the TMO as in Fig. 5.3b.

The advantages of this structure, particularly for the early phases of work with the new material systems, include the following:

(1) The structure can be made quickly with a minimum number of steps.
(2) The bulk dielectric is thermal Si oxide whose properties are well understood. Therefore any unusual results are solely attributable to the dielectric−metal oxide interface, the metal oxide bulk, or the contacts.
(3) Finally, this structure can be subjected to a full range of temperatures in order to fully investigate the potential of the material system. The continuous gate devices can be deposited using shadow masks to define both the source−drain contacts as well as the TMO channel material.

Bottom gate staggered. In later work, as the ability to etch metal oxides has improved, photolithography has been used to define staggered bottom gate devices (Fig. 5.3c). In this structure, the bottom metal is patterned followed by deposition of the dielectric, the metal oxide active layer, any contact layer, and finally the contact metal. The active region around the device is patterned followed by patterning of the source and drain electrodes and any contact layer. This procedure requires precise alignment of the patterned gate and source–drain electrodes, hence the need for photolithography. The patterning of the source–drain contacts can first be followed by deposition of the semiconductor material (Fig. 5.3d).

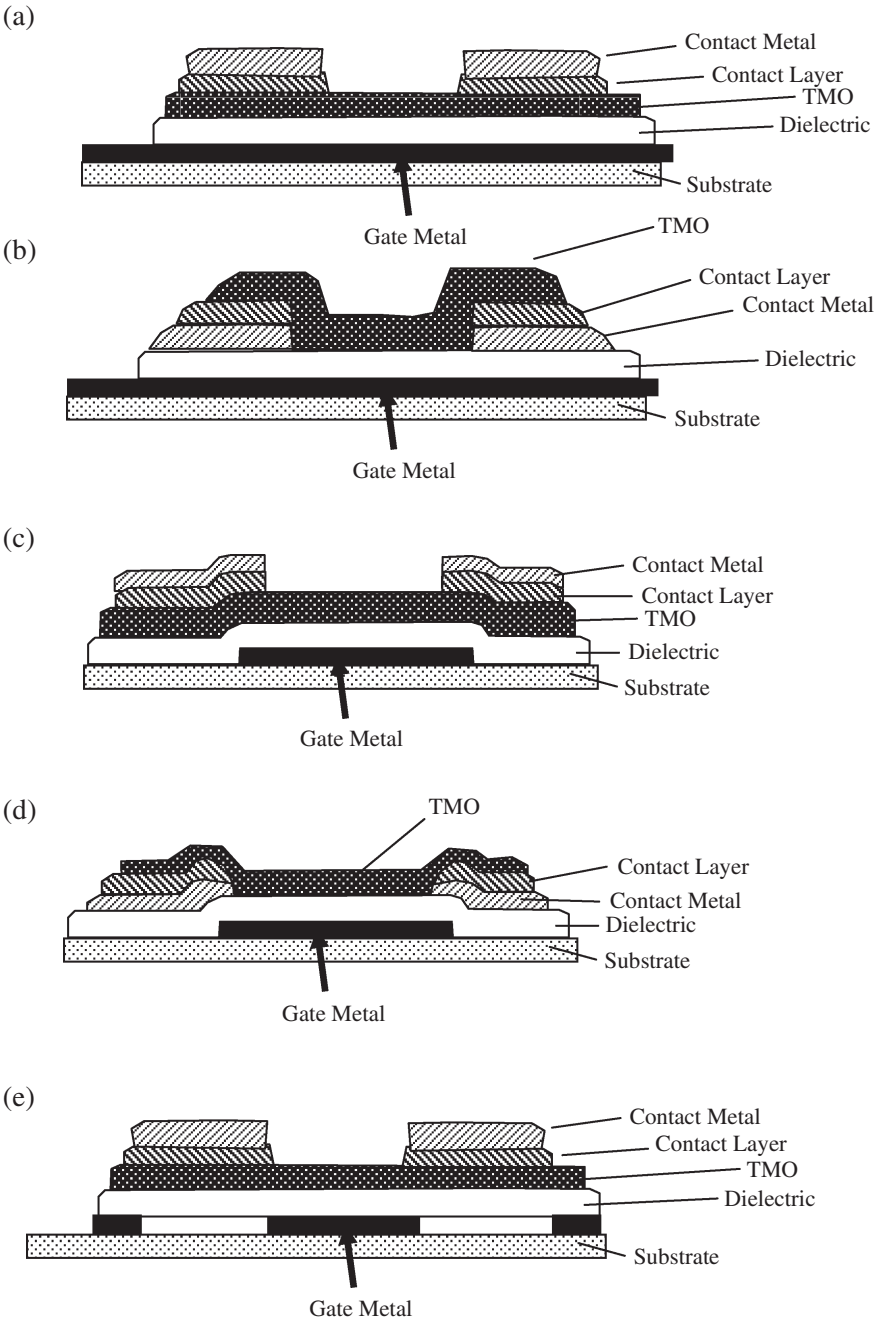

Fig. 5.3 Various transistor structures used in flexible transistors (**a**) continuous bottom gate staggered, (**b**) continuous bottom gate collinear, (**c**) bottom gate staggered, (**d**) bottom gate collinear, and (**e**) constant level transistor. Shadow mask for (**a**) and (**b**), photolithography for (**c**) and (**d**), and imprint lithography for (**a**) and (**e**)

Constant level transistor. This transistor structure is a preferred structure for SAIL defined devices [57, 58]. The material deposition is completed before any etching occurs. The layers are patterned by imprint lithography using SAIL (discussed in detail below). Devices with short channel lengths of 1 μm or less can be made on thin flexible substrates using this structure. There is no step coverage in this structure and the device can be fabricated from a complete metal–dielectric–semiconductor contact stack (Fig. 5.3e). There is also a simplified version of this device which has an unpatterned gate that is useful for transistor development work and slow applications but is unsuitable for higher speed applications (Fig. 5.3a) due to the large source–gate and source–drain overlap capacitances.

5.5 Fabrication on Flexible Substrates

One of the most difficult problems associated with flexible substrates, regardless of the materials used in the technology, is the dimensional variability of the substrate during device fabrication. The combination of large dimensional changes in flexible substrates and the strong dependence of device performance on precise source–drain alignment with respect to the gate require new approaches for fabrication. As mentioned in other chapters, some of these new methods include jetting of masking materials or electronic materials with dimensional adjustment among layers made dynamically during jetting. In this section, a new method for precise layer-to-layer alignment is presented to solve this alignment problem using a roll-to-roll compatible manufacturing technique. This fabrication method is applicable to many other flexible electronic material systems, such as low-temperature poly-Si and a-Si.

The performance of the transistors depends strongly on the source–drain electrode overlap with the gate and the size of the channel. If there is a gap between the source and the gate is 1 μm or larger, the on-current will be significantly reduced by the resistance of the unformed channel. If the pixel capacitance is small compared with the gate capacitance of the transistor, the turn-on time $t_{on} = L^2/(\mu_{FET} V_{ds})$, where L is the channel length, μ_{FET} is the field effect mobility, and V_{ds} is the drain–source voltage. Thus, a short channel greatly decreases the turn-on time of the transistor. Moreover, the on-current depends inversely on L resulting in a much larger on-current as the device size is decreased. On the other hand, a large overlap between the source–drain and the gate creates a significant feed-through capacitance that causes gate transients to be transferred to the pixel. Thus, the ability to align the source–drain contacts with respect to the gate to a level of 1–2 μm is needed to produce devices with speed and voltage transfer fidelity required by present display technologies.

The ability to control the overlap of source–drain layers with the gate to 1 μm accuracies has been quite difficult because the changes in dimensions of large-area flexible substrates in a roll-to-roll environment are quite large. Typically, plastic substrates have thermal expansion coefficients ranging from 10 to 100 ppm/°C and elastic moduli in the range of 0.5–3 GPa compared with 4–9 ppm/°C and 100 GPa

for glass. In addition, the flexible plastic substrates are about 50–100 μm thick compared with 3 mm for typical glass displays. For electronics fabricated on a 30 cm wide web, a force as small as 1 N will deform the substrate roughly 300 μm while the thermal-induced dimension changes are 30 μm/°C from one side relative to the other. In addition, as the various overlayers are patterned, the overlayer-induced strain is nonuniform. Hence, the substrate changes size with respect to the mask of the next layer. As a result, it has been virtually impossible to align successive layers to better than about 30 μm, unless the substrate held dimensionally stable by bonding to a more rigid substrate. This later approach has all the expenses and limitations of wafer and glass-based processing, negating the advantage of using low-cost substrates in the first place.

The problem of layer-to-layer alignment on flexible substrates has been solved using SAIL [57, 58]. This fabrication method uses the ability of imprint lithography to fabricate polymer masking structures with precise height control. The information for various layers is encoded within the height of the imprinted structures. Thus, a single imprint step defines all the structures needed to complete the device fabrication. Any change in the size of the substrate affects all layers and, therefore, does not alter the relative alignment of different layers.

5.5.1 Imprint Lithography

For the past 50+ years, integrated circuit fabrication has proceeded through the use of photolithography and photoresist to define the critical features of ever reduced device sizes. As mentioned before, this technology has alignment and cost problems when used with free-standing large-area flexible substrates. The comparatively new fabrication technology, imprint lithography, is a promising new approach for low-cost fabrication of submicron feature electronics on large-area flexible substrates [59–61]. Imprint lithography, or more precisely, soft lithography in the present case creates multilevel patterns that can be used as masks without expensive photolithography. As presented later, the multilevel capability of imprint lithography can solve the layer-to-layer alignment problem inherent in flexible electronics and is compatible with high-throughput batch or roll-to-roll technology. Imprint lithography is useful not only for TMO devices but also for any flexible electronic technology such as a-Si and even has applications for organic electronics if a nonorganic imprint liquid is developed.

The imprint procedure consists of a relatively small number of steps [57, 58]. First, a master is fabricated using traditional photolithography and silicon patterning steps (Fig. 5.4a). Second, a replica stamp is made from the master by coating the master with a release agent and then with polydimethylsiloxane (PDMS) polymer (Fig. 5.4b). The PDMS stamp is compliant and is a remarkably faithful inverse replica of the original master (see Fig. 5.5). This stamp is attached to a flat quartz plate if it is to be used in batch processing or can be attached to quartz roller if roll-to-roll imprint lithography is used (Fig. 5.4c). The substrate plus desired blanket

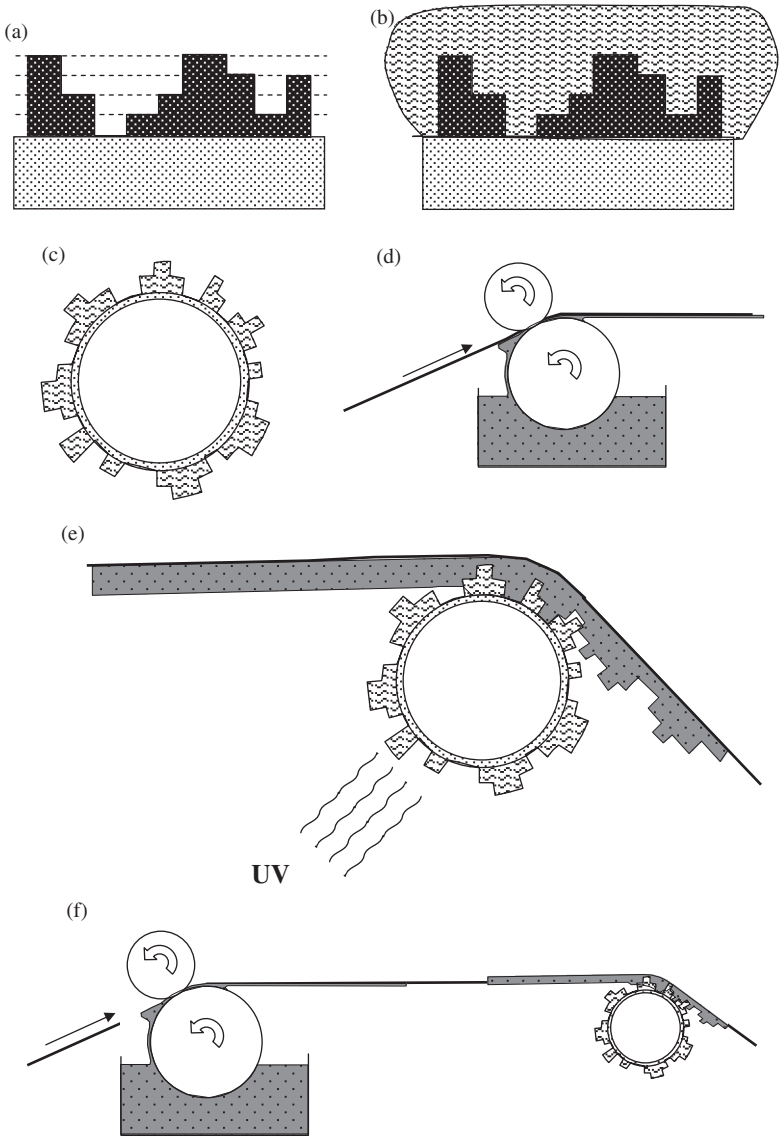

Fig. 5.4 Steps used to create imprint lithography patterns on flexible webs for SAIL fabrication of devices

deposited material is coated with a thin layer of thermal or UV curing epoxy, such as Norland UV curing epoxy (Fig. 5.4d) [62]. The epoxy layer is imprinted by the PDMS stamp and irradiated with UV or heated to polymerize the epoxy within the stamp (Fig. 5.4e,f). The polymerized epoxy replica is released from the stamp and is used as a mask for subsequent processing. An electron micrograph of a multilevel

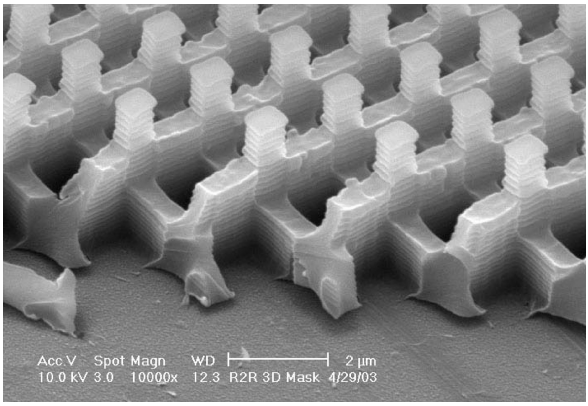

Fig. 5.5 Multilevel imprint pattern resulting from imprint lithography. The fine scallops are in the original mask arising from the passivation and etch steps of the Bosch process used to create the master

imprinted UV polymer structure is shown in Fig. 5.5. The fidelity of replication from the original master is remarkable. The scallops in the side walls are replicated from the master and arise from the passivation and etch cycles of the Bosch process used to create the high aspect ratio structures in the master. These features indicate that the process is capable of replicating 3-D features smaller than 60 nm.

Imprint lithography has a number of advantages over photolithography. It is capable of producing features as small as 60 nm at rates of centimeters per second. The PDMS stamps last over 3,000 imprints or more and each master can produce perhaps 100 or more stamps. Hence, the cost of the master is amortized over a large number of impressions while the master cost is not that much different than a single silicon wafer. So the imprint stamp costs per imprint are very low. In addition, imprint lithography equipment costs are much smaller than photolithography that requires clean rooms, vibration isolation, large complex optics, and multiple exposures per wafer. Finally, roll-to-roll fabrication facility costs scale roughly as the width of the web rather than as the area of the electronics. For large-area flexible devices, this advantage becomes increasingly important. Finally, the substrate costs are low as well as handling costs. The result of all these cost reductions lead to the expectation that the cost of large-area flexible electronics produced and imprint lithography and roll-to-roll methods can be significantly decreased.

5.5.2 Self-Aligned Imprint Lithography

The ability of imprint lithography to make multilevel layer structures enables the information of multiple mask layers to be encoded in the imprint layer thickness. Because all levels and therefore layer information is imprinted in one imprint process, subsequent changes in substrate size do not result in layer-to-layer misalignment. The SAIL process uses the multilevel imprint mask to create the desired device structures.

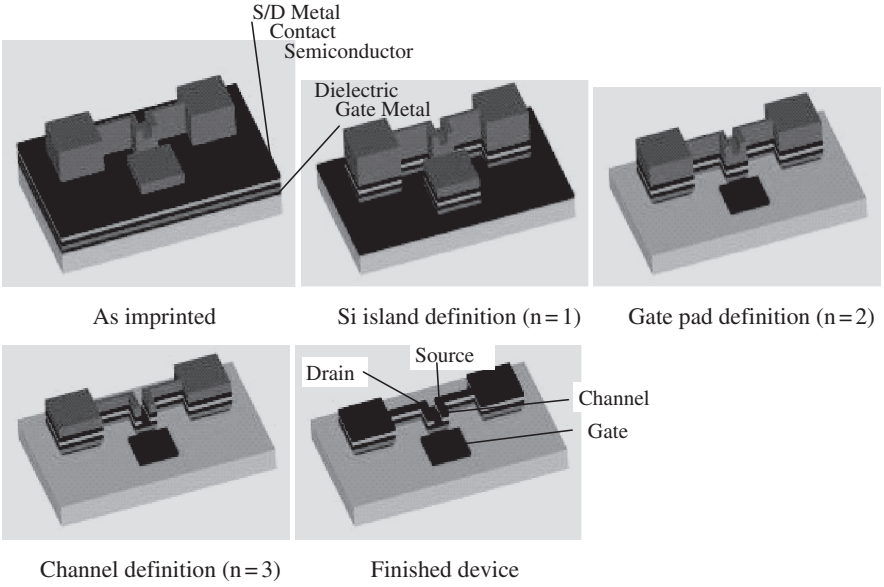

Fig. 5.6 The steps involved in SAIL fabrication of a single transistor. Between each step, the imprint mask polymer thickness is decreased by one level thickness to expose the next layer for patterning. Between n = 1 and n = 2, the gate is isolated from the bottom gate metal under the source and drain by undercut removal of the bottom metal in the narrow 'fuse' region connecting the source and drain to other pads

The SAIL process begins with a blanket deposition of a complete stack of materials needed for the device as shown in Fig. 5.6. The complete stack consists of a substrate, a gate metal, a dielectric, an active semiconductor (in this case a TMO), an optional contact material, and finally the top metal. A multilevel mask is imprinted on the device stack in order to define the subsequent features. The first etch step removes the entire stack in the region not covered by the imprinted polymer. During etching of the bottom metal, the metal is removed by undercutting the thin bridge portions of the pattern (between n = 1 and n = 2). This metal undercut isolates the source and drain regions from the gate eliminating possible shorts from the source and drain to the gate while minimizing parasitic source–gate and drain–gate capacitances. Next the imprinted polymer is etched until the next level is removed (n = 3). Then the stack layers are removed down to the gate (bottom) metal exposing the gate contact and pad. The polymer mask is then etched until the next polymer layer is eliminated exposing the channel region. The top metal and optional contact material (e.g., ITO) are etched by stopping on the active layer material using timed etching or through the use of selective etches between the contact and the active layer of the transistor. This etch step defines the channel length. Finally, the last level of the imprinted polymer is removed leaving the top metal exposed as shown in Fig. 5.7. The resulting transistor is a constant level device as

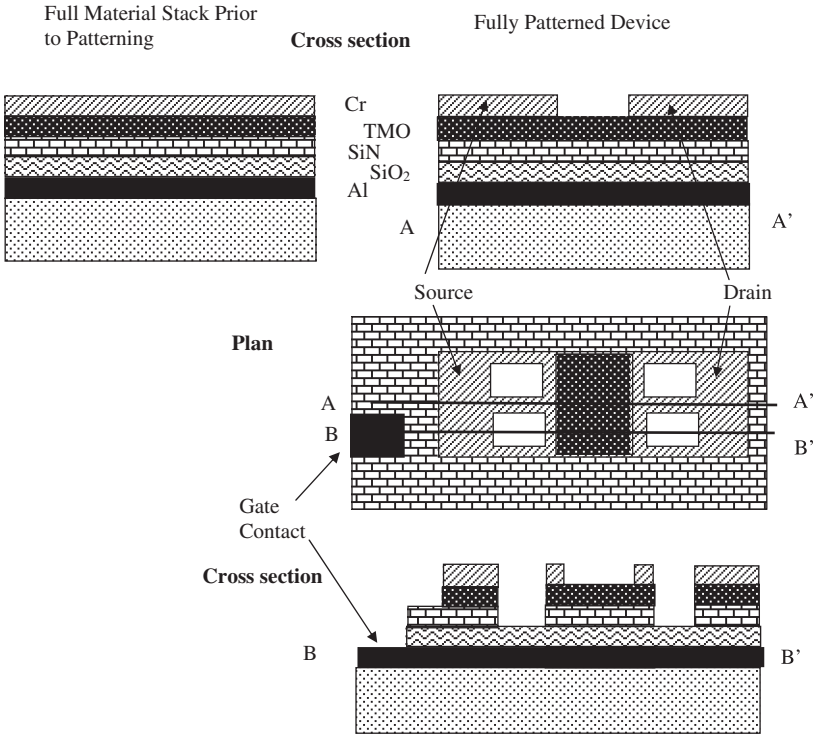

Fig. 5.7 Cross section and plan view of a single layer transistor fabricated by the simplified self-aligned imprint lithography (reefed-SAIL)

described in Fig. 5.3e. The various structures are aligned to within the accuracy of the undercut process.

There is an abbreviated form of the SAIL process, reefed-SAIL, in which the back metal is not patterned but remains as a continuous back contact (Fig. 5.4a). This eliminates one of the mask levels and several etch steps including the fuse step. This process is useful for slow devices in which the source–gate and drain–gate overlap capacitances are not important and for more rapid prototyping investigations. Cross sections and plan views of the devices produced by the abbreviated (reefed-SAIL) and full-SAIL processes are shown in Figs. 5.7 and 5.8 for a ZTO or an a-Si device with a composite dielectric.

An example of a ZTO device fabricated using reefed-SAIL is shown in Fig. 5.9. The pictured reefed-SAIL device is fabricated on a degenerate doped Si wafer as the gate and thermal oxide as the gate dielectric. These devices demonstrate the patterning precision possible with SAIL. Unlike jetting processes where there are problems of drop misplacement, splashing, and uneven drop wetting variations; the structures are sharp and well defined on a submicron scale. For this particular device, the channel region is 2 μm wide. The ability to fabricate very precise aligned and

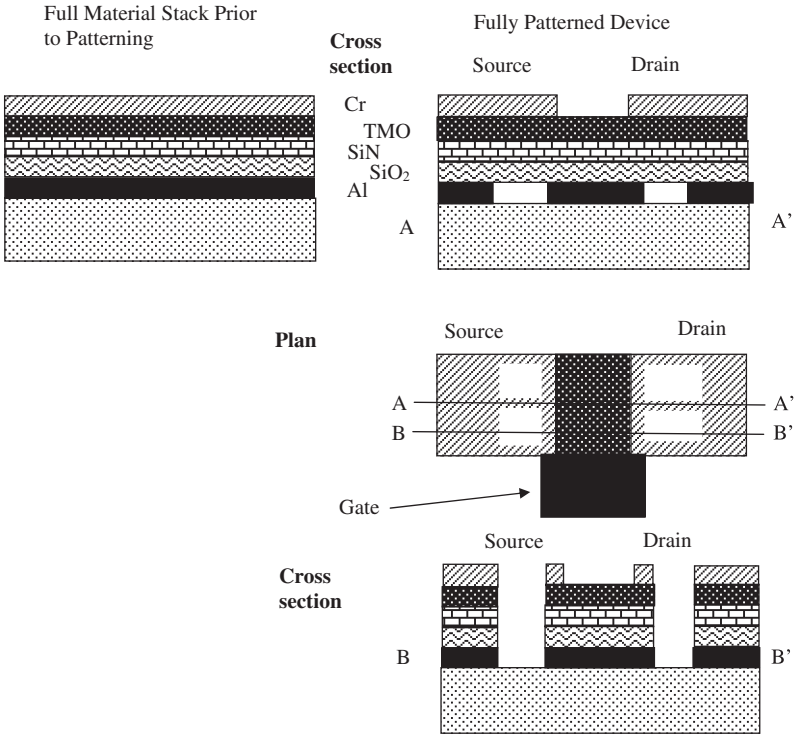

Fig. 5.8 Cross section and plan view of a single layer transistor fabricated by full self-aligned imprint lithography (full-SAIL). Note the isolation of the gate from the bottom layer metal in the source and drain

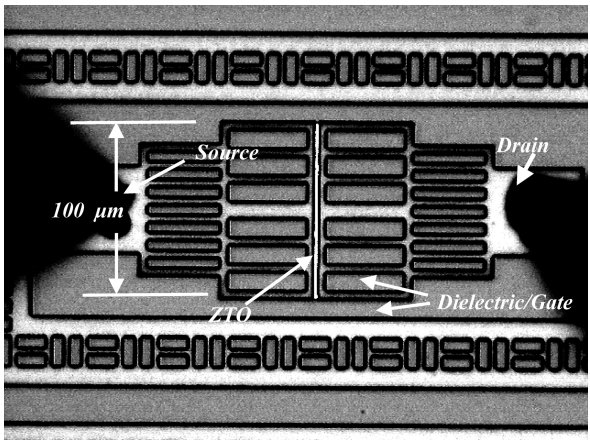

Fig. 5.9 A ZTO transistor fabricated using the reefed-SAIL method on a doped c-Si wafer as the gate electrode and thermal oxide as the gate insulator. The channel region is 2 μm wide

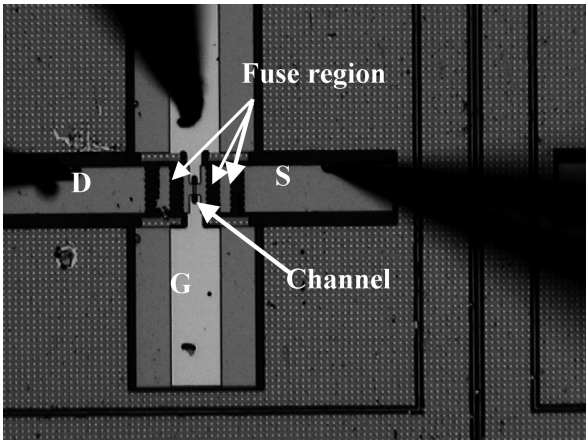

Fig. 5.10 Amorphous silicon transistor fabricated using a full-SAIL process

dimensioned devices using SAIL imprint lithography is apparent. The 0.3-μm pattern definition precision greatly exceeds that of shadow masking (roughly 20 μm on flexible substrates and roughly 15 μm for ink-jet-defined device structures). A full-SAIL a-Si device is shown in Fig. 5.10, which includes the fuse regions that are undercut by etching the bottom metal.

5.5.3 SAIL Transistor Results

While the described SAIL fabrication steps appear plausible, the fabrication and characterization of actual devices on flexible substrates indicate that the SAIL process works in practice. Because dry etching recipes for TMOs are still being developed, the reefed-SAIL and SAIL fabrication processes have been used to fabricate a-Si transistors, a mature proven technology that can be used to benchmark the transistors on flexible substrates. Basically, the results presented in this section demonstrate that imprint lithography readily produces flexible short and long channel devices whose performance matches that found for devices on rigid substrates in a-Si. By implication, imprint lithography should be able to generate comparable results for TMO devices.

Amorphous silicon devices were fabricated using SAIL and device material stacks consisting of the following layers. The substrate was 50 μm polyimide with a 100-nm stainless steel layer on the back. A 100-nm Al layer was covered by a 50-nm plasma enhanced chemical vapor deposition (PECVD) SiO_2 layer and a 200-nm PECVD SiN layer deposited at 250°C. Then a 100-nm a-Si:H layer was deposited followed by a 100-nm n+ layer and finally 100 nm of Cr comprises the top layer. The devices were imprinted and developed to produce arrays of all combinations of transistors width $W = \{10, 20, 50, 100\}$ μm and length $L = \{1, 2, 5, 10, 20, 50, 100\}$ μm. The normalized transfer characteristics, source–drain current/(W/L),

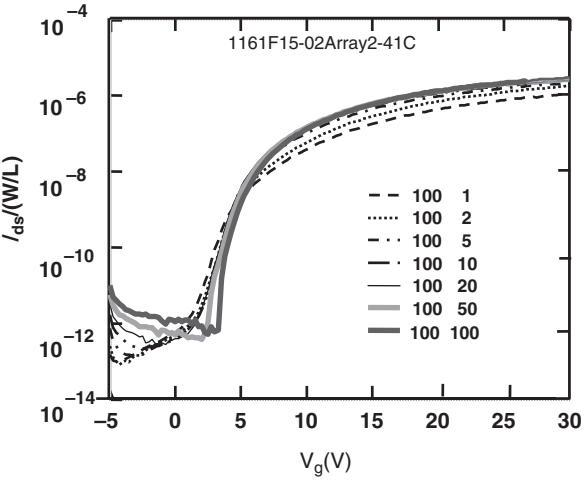

Fig. 5.11 The source–drain current $I_{ds}/(W/L)$ versus V_g for W = 100 μm and L = {1, 2, 5, 10, 20, 50, 100} μm for SAIL a-Si transistors

for $W = 100$ μm devices with various L are shown in Fig. 5.11. If the current scales with L, the curves should completely overlap. There is some broadening of the exponential slope for the shortest devices but otherwise the L scaling holds. Thus, for the $W/L = 100$ μm /1 μm devices, the on-current is 100 μA which is quite respectable for an a-Si device. Such a device could easily drive OLED pixels. The subthreshold slope is about 0.6 V/decade, the on–off ratio is about 10^5, and V_t is about 3 V. Thus, SAIL can fabricate 1 μm channel length devices in a roll-to-roll process on flexible substrates. The device uniformity is quite decent as well.

SAIL fabrication of arrays has also been undertaken using identical procedures along with the pixel electrode for the backplane of a display. Currently, arrays of 50×50 and 100×100 devices are being fabricated. As with all flexible electronics technology, the yields and susceptibility to flexing remain largely unexplored.

5.5.4 Summary of Imprint Lithography

In summary, imprint lithography can make short channel devices on flexible substrates for large area, flexible, and inexpensive applications. The SAIL process described in this section solves the layer-to-layer alignment problem for micron-scale alignment on dimensionally variable substrates. The abbreviated reefed SAIL process has been used to fabricate isolated TMO transistors, while the full-SAIL process has been used to fabricate amorphous Si arrays and transistors on flexible substrates.

5.6 Flexible TMO Device Results

The previous sections describing flexible transistor fabrication indicated that there are three main ways of fabricating TMO devices: shadow masks, photolithography, and imprint lithography. Section 5.1.2 summarized some important TMO transistor results on rigid substrates; further details can be found in Table 5.1 and the corresponding references. In this section, the performance of various flexible TMO transistors using the above-mentioned fabrication methods is described. While significant TMO work on rigid substrates has been undertaken, flexible TMO work and TMO work using imprint lithography are still in their infancy. It is expected that the TMO results on rigid substrates mentioned above represent appropriate performance benchmarks for flexible electronics because the rigid, higher temperature approaches can utilize any of the flexible technologies. Thus, the results in this section should be compared to rigid substrate results as well as alternative flexible platforms such as a-Si:H.

One of the first reports of devices fabricated on flexible substrates is by Carcia et al. [20], where a mobility of 0.4 $cm^2\ V^{-1}\ s^{-1}$, an on–off ratio of 10^4, and $V_t = 7.5$ V was achieved. The transistor consisted of a fluoropolymer dielectric, an RF sputter deposited ZnO active layer, and a polyimide substrate and was fabricated at room temperature. The results are shown in Fig. 5.12. This work was one of the first to demonstrate that TMO TFTs could produce flexible transistors with capabilities comparable to a-Si although the off-current is a bit high. Subsequent work by these researchers using a Al_2O_3 dielectric, ZnO semiconductor, e-beam evaporation on polyimide, and temperatures below 120°C produced devices with mobilities of 50 $cm^2\ V^{-1}\ s^{-1}$, on–off ratios of 10^5, and $V_t = 3.2$ V [22, 37]. However, the off-current, roughly 10^{-9} A, was too high for a pixel transistor on an LCD. Such a large leakage requires unacceptably large refresh rates and concomitant power dissipation. The mobility and on-current, however, demonstrate that high-performance flexible electronics can be made using TMO as the channel material.

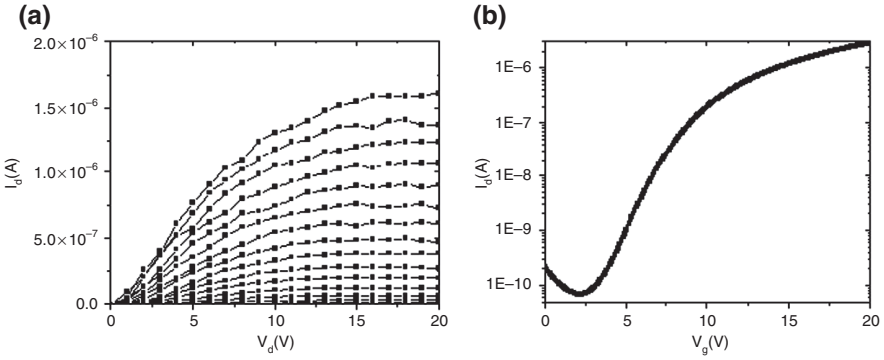

Fig. 5.12 Flexible ZnO TFT curves of (**a**) I_d versus V_d for $V_g = 0, 1, \ldots, 20$ V and (**b**) of I_d versus V_g for $V_{ds} = 20$ V. W/L = 40 μm /400 μm from [20]

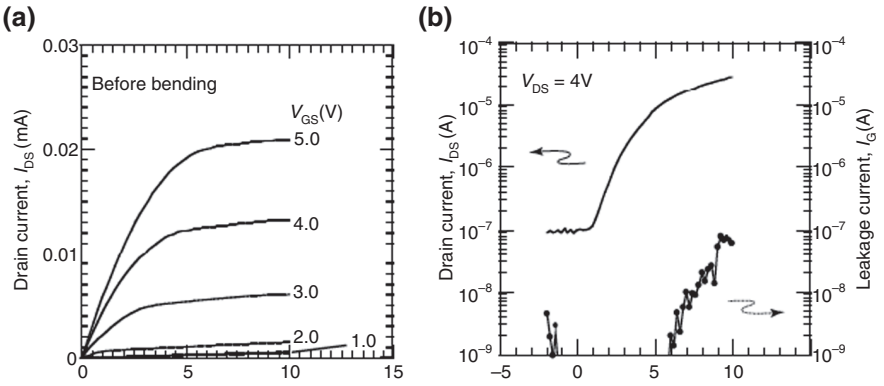

Fig. 5.13 From [29] on PET with a maximum temperature near room temperature

In [29], transistors were fabricated on PET using IGZO as the TMO and Y_2O_3 as the dielectric where the fabrication temperature was kept near room temperature (Fig. 5.13). A mobility of 8 $cm^2\ V^{-1}\ s^{-1}$ was achieved with an on–off ratio of 10^3 and an off-current of 10^{-7} A. Except for the large off-current this is a reasonable transistor. The importance of this work is that PET is clear unlike polyimide, so the devices could be used in principle as part of a backlit liquid crystal display (LCD). Also, this work represents an improvement of the transistor characteristics over the first flexible transistor work. These flexible TMO results are not as good as the results achieved on rigid substrates.

In order to further improve the performance of flexible TMO devices, the contacts must produce sufficient current. In Fig. 5.14, the output characteristics of a ZTO transistor on polyimide using shadow mask definition of ZTO on PECVD deposited SiON, 50-μm polyimide substrate, and a 250°C 10-min anneal [26]. The transistor output curves are shown for contacts consisting of Al on ZTO. The concave current

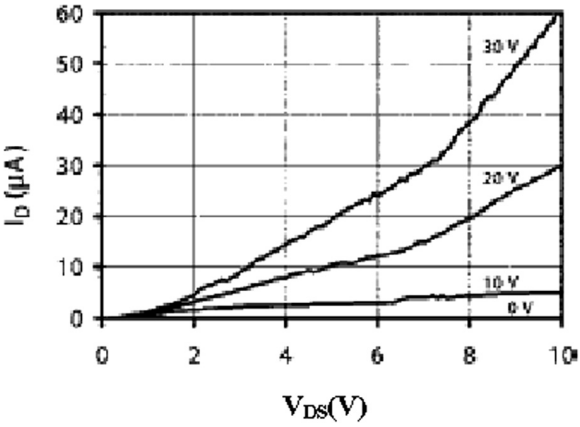

Fig. 5.14 The output characteristics for a ZTO transistor with Al contacts, SiON dielectric, and a maximum fabrication temperature of 250°C. The concave characteristics are indicative of blocking contacts and suggest that improved contacts can give rise to improved device performance [26]

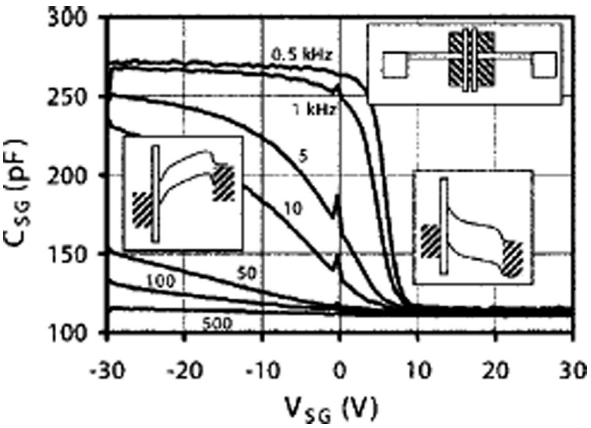

Fig. 5.15 The source–gate capacitance versus dc source-to-gate voltage bias for various frequencies for the transistor with Al source and drain contacts. The measurement frequencies are 0.5, 1, 5, 10, 50, 100, and 500 kHz. The insets indicate the device layout (*upper right*) and the band structure for negative (*left*) and positive (*right*) dc bias conditions

crowding suggests that there is a problem with the contacts. This conclusion about the contacts was further verified by two methods: capacitance and four-probe transistor measurements. In Fig. 5.15, the capacitance of a transistor structure of the source with respect to the continuous gate is shown as a function of V_{sg}. The associated band structure is depicted in the insets and as well as the device geometry. For $V_{sg} > 10$, the device is in depletion and the channel does not conduct. Hence, the capacitance is just the capacitance of the source electrode with respect to the gate regardless of the frequency. For $V_{sg} < 0$ and low frequencies, the channel is turned on so that the capacitance consists of both the source–gate capacitance, the drain–gate capacitance, and the channel–gate capacitance. Moreover, the various capacitances are only the insulator capacitances and do not include the series capacitance of semiconductor. The additional area and lack of the semiconductor series capacitance result in the roughly factor of 3 increase in the capacitance. For higher frequencies, the RC time constant from contact and channel series resistances and the capacitances is large so there is not enough time within one cycle to charge up the channel–gate and drain–gate capacitances. By observing the frequency at which $AR_{contact}C_{ins}2\pi f = 1$, where A is the source–gate contact area, $R_{contact}$ is the contact resistance, C_{ins} is the insulator capacitance, and f is the frequency, the contact resistance $R_{contact}$can be estimated. Because $C_{ins} = 15$ nF/cm^2 the area of the device is 0.03 cm^2 and $R_{contact} \approx$ 30 kΩ. This device is, therefore, not capable of passing much more than about 35 μA without a significant voltage drop across the contact.

A second means of estimating the contact resistance is to measure the voltage drop across the contact using a four-probe method (Fig. 5.16) [26, 28]. The source and drain probes drive a current through the source and drain contacts and the voltage of the two inner probes is measured using a very high impedance instrument, so no current is drawn through the probes. The potential difference between the source and the first contact yields the voltage drop across the source contact, while the voltage difference between the final voltage probe and the drain yields the voltage

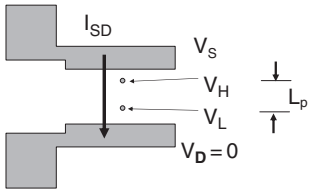

Fig. 5.16 Four-probe configuration for measuring the source and drain contact resistance. Two addition high impedance probes or electrodes are placed between the source and drain to measure the potential drop between the channel and the source and drain electrodes

drop across the drain. The potential drop between the two voltage probes yields the channel voltage drop. In particular, the channel resistance, R_{CH}, the source resistance, R_S, and the drain resistance, R_D are roughly given by

$$\begin{aligned} R_S &= (V_S - V_H)/I_{SD} \\ R_D &= V_L/I_{SD} \\ R_{CH} &= (V_H - V_L)/I_{SD} \end{aligned} \tag{1}$$

The expressions for R_S and R_D are approximate in that some channel resistances are included because the probes include at least several microns of the channel. Using these relations, the source, drain, and channel resistances can be estimated [26, 28]. For the Al and ZTO contact, this method yields approximately the same value of the contact. The four-probe method can be used to determine

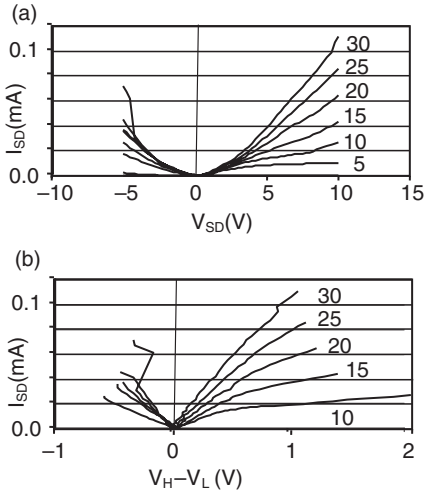

Fig. 5.17 The source–drain current in a ZTO transistor with Al contacts and no ITO layer to improve the contact resistance (**a**). The same current plotted against the voltage drop between the inner voltage sensing probes (**b**). Notice that the current crowding indicative of contact effects has been eliminated

the characteristics without contact impedance effects. In Fig. 5.17, the source–drain current through a ZTO transistor with PECVD SiON dielectric, Al contacts deposited directly on the ZTO, with $W/L = 2000\ \mu m/200\ \mu m$ is presented. The field effect mobility is about 0.2 $cm^2\ V^{-1}\ s^{-1}$ for the uncorrected curves. The normal output curves in Fig. 5.17a exhibit current crowding while plotted against the potential difference between the two electrodes eliminates the crowding (Fig. 5.17b). Notice also the difference in horizontal scales is almost a factor of 10. The mobility extracted from the contact corrected curves will, therefore, be about a factor of 10 larger and is about 1.5 $cm^2\ V^{-1}\ s^{-1}$. Thus, the contact effects dramatically alter the extracted mobility. The four-probe methods enable the true channel mobility to be extracted by eliminating the contact effects. Clearly, however, the most important point is that the contacts must be improved.

By including an ITO layer between the Al and the ZTO, the contact resistance was decreased to about 3 kΩ. In addition, if an oxide buffer layer is included between the SiON and the ZTO, the device performance is greatly improved. For this device the output and transfer characteristics are shown in Figs. 5.18 and 5.19. The incremental mobility is 14 $cm^2\ V^{-1}\ s^{-1}$(Fig. 5.20) and the on–off ratio is 10^7, and an off-current of 10^{-11} A was produced showing that the high off-current can be reduced while maintaining high on-currents. Moreover, this is a stable current and changes little with stressing. The threshold voltage is somewhat negative but this can be changed by adjusting the dielectric deposition conditions and/or injecting the appropriate charge into the dielectric to adjust the threshold voltage. The maximum incremental saturation mobility is ∼14 $cm^2\ V^{-1}\ s^{-1}$ (Fig. 5.20) [26, 28]. The threshold voltage is about −9 V (Fig. 5.21). In summary, the flexible transistor properties are nearly equivalent to a comparable rigid substrate device composed of similar materials. This bodes well for the future of flexible TMO devices.

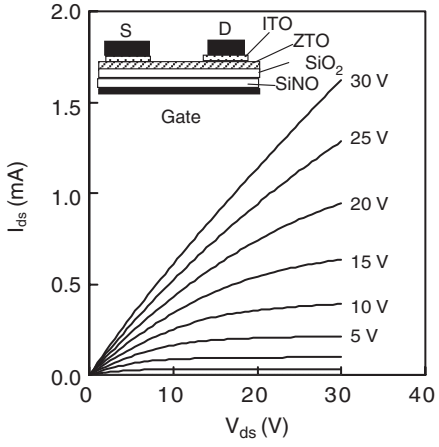

Fig. 5.18 A ZTO transistor deposited on 50 μm polyimide, PECVD SiON, ITO contact layer, Al contacts, and a SiO_2 buffer layer (W/L = 1,000 μm /100 μm)

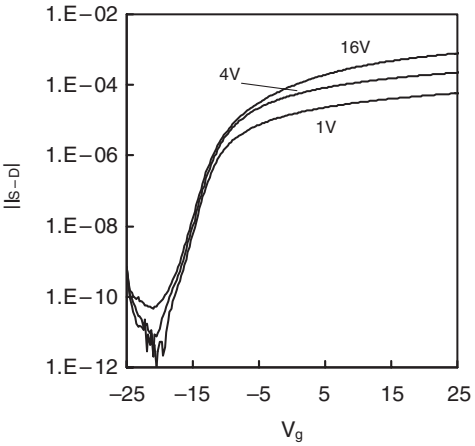

Fig. 5.19 The transfer characteristics of the device in Fig. 5.18

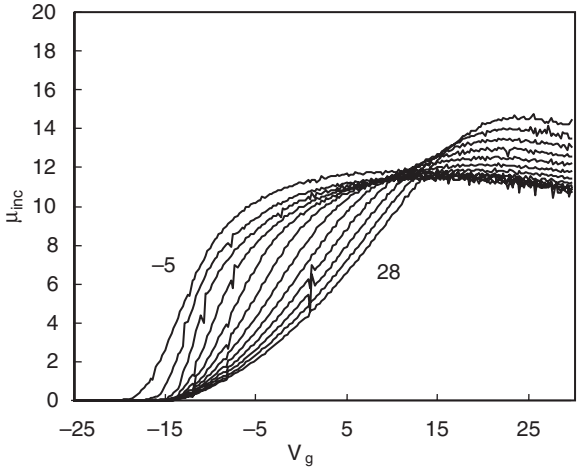

Fig. 5.20 The incremental mobility for the device in Fig. 5.18. The maximum mobility is 15 cm^2 V^{-1} s^{-1}

5.7 Future Problems and Areas of Research

In order to realize the full promise of flexible TMO electronics, there are a number of areas in which further research is desirable. These include the following:

(1) Better control of the carrier density in the TMO channel materials.
(2) Improved low-temperature dielectrics.
(3) Better etching processes for TMO materials.

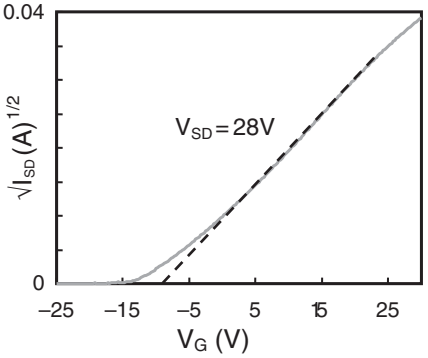

Fig. 5.21 Transfer characteristics of device in Fig. 5.18. $V_T = -9$ V

(4) Improved p-type material.
(5) Device electrical stability.
(6) Flexure and adhesion of the TMO materials on flexible substrates.
(7) Yield validation of flexible substrate fabrication methods.

Progress on these issues could greatly expand the possible areas of application for flexible TMO electronics and improve the control of the TMO material system for cost effective production.

5.7.1 Carrier Density Control

One of the areas that can be difficult to control reliably in TMO materials is the carrier density particularly within the lower temperature constraints imposed by flexible substrates. Because oxygen defects act as n-type dopants, the materials typically must be sputtered in high-oxygen partial pressure conditions. Otherwise the TMO will end up being n-type and unsuitable for an accumulation mode transistor [52–56]. Such n-type materials could in principle be used in depletion mode applications if low off-currents are not required. The high-oxygen partial pressures, however, tend to promote arcing and dielectric breakdown of the underlying gate dielectric in the sputtering environment. More research is needed in understanding the energy levels and doping effects of O vacancies in the various TMO systems particularly as a function of the transition metal cation.

The carrier density is also affected by the presence of H. There is significant evidence that H within many of the TMO materials acts as an n-type dopant [51]. In fact, exposure to an H plasma can change the conductivity of TMO by orders of magnitude [48, 49]. Hence reactive ion etching (RIE) with H-containing materials, such as CH_4 and CF_3H, can be a source of carrier density variation even though these gases are the leading candidates for dry etching TMO materials. Also

dielectrics such as PECVD a-SiN dielectrics can also introduce H into the adjacent TMO. Because of the ubiquitous prevalence of H during deposition, etching, and in neighboring materials and the rather high mobility of H in TMOs, postfabrication annealing protocols can be important to control the carrier density. Often annealing for short times above 200°C can significantly reduce the excess carrier density. Presumably this annealing causes H to move to become electrically inactive without releasing H from any dielectric such as SiN that might contain H. Postfabrication H motion could also be a source of instability in the electronic properties of the fabricated devices. Significantly more research is needed in understanding the energy levels introduced by H, the diffusion of H within TMOs, and the interchange of H with dielectrics both during deposition and postdevice fabrication.

5.7.2 Low-Temperature Dielectrics

As with all material systems used on flexible substrates, good low-temperature dielectrics are critical. The dielectrics must have low interface defects with the TMO materials at low deposition temperatures. In bottom gate devices, it is also desirable that the surface roughness of the dielectric be small in order that the field effect mobility approaches that of the underlying TMO. Most importantly, the dielectric must withstand high fields without trapping significant charge. The trapped charge will cause threshold shifts arising from continuous application of gate biases. While charge-trapping-induced threshold voltage shifts are undesirable for all flexible electronic systems, they are particularly undesirable for electronic applications such as driving OLEDs and drive electronics; the potential new application areas for TMO materials. Otherwise one must use more elaborate self-compensating circuits in such applications. Some of the dielectrics that have been used are listed in Tables 5.1 and 5.4, but there has been little investigation into their stability under voltage stress or their tendency to create interface states. Research comparing the stability of the various dielectrics may also shed light on the physical origins of the metastability.

5.7.3 Etching of TMO Materials

For batch fabrication of TMO electronics on flexible substrates, etching continues to be a somewhat difficult area. Both wet and dry etching of TMO materials have undesirable features. Besides the waste disposal issues and expensive process of wet etching, many flexible substrates such as polyimide and PET can absorb water which in turn can cause swelling. Hence, wet etching may require a moisture barrier layer to protect the substrate. The preferable dry RIE etching is also somewhat difficult for TMO materials. The two most promising etching chemistries are CH_4/H_2 and BCl_3 [50]. The BCl_3 chemistry is slow and tends to etch contact metals as well as TMO materials thereby limiting the types of process flows and structures that can

be fabricated. The CH_4/H_2 chemistry on the other hand etches the TMO material while leaving metals intact. The chief difficulty with the CH_4/H_2 chemistry is that it tends to leave carbon structures, maybe even carbon nanotubes on surfaces other than the TMO such as the walls of the chambers and source–drain contacts. In normal conditions, one uses oxygen to suppress carbon compound formation but this interferes with the etching of the oxygen in the TMO. The hydrogen concentration is adjusted to help etch surface carbon compounds but as mentioned above, excess atomic H can cause problems for the carrier density in the TMO unless the hydrogen is removed by subsequent annealing steps. The deposition of carbon compounds on the chamber walls often requires periodic mechanically cleaning as the material is remarkable resistant to usual O cleaning procedures. While existing etch protocols are satisfactory, improved etching chemistries and protocols would be quite useful for the wide scale use of TMO electronics.

5.7.4 P-type TMO

Another major area for future research is the deposition of p-type TMO material. P-type material would be highly desirable in order to create CMOS-type circuitry for drive electronics and other electronic applications. Significant effort has been made to develop p-type TMO materials [63–69]. In general, because O vacancies dope n-type TMO, it is difficult to produce p-type material. Whenever a p-type dopant atom is introduced into the growing materials, an O vacancy becomes more energetically favorable. The O vacancies compensate the material. There is promising work using Cu containing materials to help dope the material p-type [63–69]. The Cu cation has an unfilled 4d that lines up with the valence band of most TMO. Cu doping then serves as a p-type dopant. The p-type carrier densities that have been achieved are 3×10^{19} carriers cm^{-3}. Unfortunately, the features of TMOs that make the electron mobility high even for amorphous disorder, results in reduced mobility for holes. The top of the valence band is primarily directional O 2p-type orbitals that are sensitive to disorder. In sufficient quantities, the Cu constituents create a miniband at the top of the valence band that increases the hole conductivity despite the disorder induced broadening of the valence band edge. The best mobilities achieve to date are mobilities of $0.13\,cm^2/V{\cdot}s$ for nonsingle crystalline material [63–69].

5.7.5 Stability

As in the case of many material systems with disorder and low-temperature dielectrics, TMO devices exhibit metastability. The quantification and understanding of this phenomenon are just beginning. It has been known for a while that ZnO, for example, exhibits a persistent photoconductivity [52–56]. Illumination by bandgap light causes significant changes in conductivity that last for hours or more. This effect has been attributed to O chemisorption initiated by the UV light. The

effect is minimized if the transistor has a passivation layer preventing O interaction with the back surface [52–56]. Depending on the composition, annealing history, and exposure to O or H, the electrical characteristics exhibit varying degrees of instability. The instabilities can arise from changes in carrier concentrations, defects in the semiconductor, and/or charge trapping in the insulator. In general, the higher the annealing temperatures, the better the stability and the smaller the initial device-to-device variation in threshold voltages and subthreshold slopes. The presence of In also appears to increase instability. The origin and control of instabilities are of particular interest as one of the many advantages of TMO is their use in edge driver electronics and OLED drivers. The stability requirements of driver electronic devices are typically more demanding because the on-time voltage duty cycle can approach 100%, while in the typical pixel transistor, the on-time duty cycle can be made small. Significant work in this area is required.

5.7.6 Flexure and Adhesion of TMO

Common to all flexible electronic materials and fabrication methods, more work needs to be done characterizing and understanding the effects of flexure on the performance of TMO electronics. The brittle nature of TMO may suggest that flexure maybe a problem. However, the small relative area of the TMO transistor channel region, the small thickness of the TMO material, and the large compliance of the substrate suggest that flexure may not be a significant limitation for TMO electronics. Preliminary studies of devices using brittle a-Si:H as a channel material indicates that metal lines and dielectrics are more of a problem. Virtually no flexing studies on TMOs have been done.

5.7.7 Flexible Fabrication Method Yields

A final area of future study common to most all flexible material systems concerns the yield of various fabrication methods. Because the substrate dimensions are not fixed, the fabrication temperatures are low, and the fabrication methods are relatively nonstandard (not the typical photolithography), there is the all important question of yield. The initial yield of the devices, lines, and crossovers for both imprint lithography and jetting methods of fabrication must be measured and optimized. Work is just beginning to characterize the yield issues of imprint lithography. Dirt-induced defects tend to be eliminated by the imprint process while defects due to imprint stamp wear, propagate, and can result in significant yield loss. Improper stamp filling and bubble defects are less important; they cause at most the failure of one array. Yield issues regarding control and uniformity of etching masks remain unexplored. Jetting methods have problems of splashing, wetting, gaps, and nonuniform coverage issues. The yield issues associated with these flexible substrates transcend the material system and are not specific to the TMO devices.

Issues specific to SAIL that need to be measured include the following:

(1) The yield of the devices and arrays using SAIL is not yet known. There are imprint defects such as voids caused by under filling and excess imprint polymer if there is over filling.
(2) The impact of imprint wears on device yield needs to be measured in order to estimate stamp life time. Defects may form in the stamp due to particles or failure to release from the mold. These defects are then replicated.
(3) The effects of particle densities on yield and whether acceptable yield can be obtained without a clean room.
(4) Finally, the required levels of process uniformities and latitudes that affect device yield should be measured. Because SAIL is so recent, many of these issues require further work. In general, we have been encouraged by the fact that as we have moved toward roll-to-roll fabrication using SAIL, device yields, controllability, and uniformity have markedly improved over batch processing suggesting that SAIL represents a promising fabrication method for large area, inexpensive, and flexible electronics.

5.8 Summary

SAIL is a solution to the layer-to-layer alignment problem for the critical features on flexible substrates. The SAIL process can produce submicron-aligned layers and submicron-sized features, is compatible with both roll-to-roll and high-throughput manufacturing, and is inexpensive. The complex series of steps (deposition, coat with resist, expose resist, develop, etch, and resist removal) required for each layer in the standard photolithography is eliminated. The capability of the SAIL process can be used for any materials system, such as a-Si, low-temperature poly-Si, and laser recrystallized Si as well TMOs. The only materials system for which SAIL does not currently seem straightforward is organics because etch selectivity between the imprint polymer and the organic layer has not been adequately investigated. SAIL should be considered as a possible fabrication methodology in the area of flexible electronics and can enable many of the structures and devices mentioned elsewhere in this book.

The major point of this chapter is the promising possibility of TMOs for flexible electronics. These materials have demonstrated high mobilities, large on–off ratios, and reasonable threshold voltages using fabrication temperatures and procedures compatible with flexible substrates and large-throughput manufacturing methods. Transistors with mobilities as high as 30 $cm^2\ V^{-1}\ s^{-1}$, on–off ratios of 10^7, $V_t = 3$ V, off-currents of 1 pA, and on-currents in the range of 1 mA have been demonstrated. Moreover, the transistors can be completely transparent so the fill factor can be large. If the stability issue, transition metal etching and appropriate

dielectric material selection are solved, the future looks very promising for flexible TMO electronics.

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