

Contents

Preface	v
1 Introduction	1
1.1 Networks on Chips: Scalable Interconnects for SoCs	1
1.2 NoC Design Challenges	4
1.3 Book Overview	5
1.3.1 NoC Design Methods	5
1.3.2 NoC Reliability Mechanisms	7
1.4 Related Work	7
1.4.1 NoC Architectures and Design Methods	8
1.4.2 Reliability Support for NoCs	10
Part I NoC Design Methods	
2 Designing Crossbar Based Systems	15
2.1 Problem Motivation and Application Traffic Analysis	17
2.1.1 Problem Motivation	17
2.1.2 Application Traffic Analysis	19
2.2 Design Methodology	19
2.3 Exact Approach to Crossbar Synthesis	22
2.3.1 Problem Formulation	22
2.3.2 Exact Crossbar Synthesis Algorithm	24
2.4 Heuristic Approach to Crossbar Synthesis	24
2.5 Experiments and Case Studies	28
2.5.1 Experimental Platform and Power Models	28
2.5.2 Application Benchmark Analysis	29
2.5.3 Comparisons of Heuristic Engine with the Exact Engine	32
2.5.4 Window Sizing	34
2.5.5 Real-Time Streams & Effect of Binding	36
2.5.6 Overlap Threshold Setting	36
2.6 Summary	37
3 Netchip Tool Flow for NoC Design	39
3.1 Front-End Design Phase	39
3.2 Architectural Design Phase: The \times pipes NoC Library	40
3.3 Summary	42
4 Designing Standard Topologies	43
4.1 On-Chip Traffic Modeling	45
4.2 Problem Formulation	47

4.3	Mapping and Physical Planning Algorithm	50
4.4	Physical Planning	51
4.5	Experiments and Case Studies	53
4.5.1	Effect of Physical Planning	53
4.5.2	Design for QoS Guarantees	53
4.5.3	VOPD Design	54
4.5.4	Buffer Sizing and Network Optimization	54
4.6	Summary	56
5	Designing Custom Topologies	57
5.1	Objectives	57
5.1.1	Background on NoC Topology Synthesis	58
5.1.2	Background on Deadlock-Free NoC Design	59
5.2	Input Models	60
5.2.1	Area, Power Models	60
5.2.2	Traffic Models	62
5.3	Design Algorithms	62
5.4	Experiments and Case Studies	68
5.4.1	Experiments on MPSoC Benchmarks	68
5.4.2	Layout-Level Comparisons	70
5.4.3	Impact of Frequency Constraints	72
5.4.4	Handling Dynamic Effects	74
5.5	Summary	74
6	Supporting Multiple Applications	77
6.1	The Æthereal NoC Architecture	78
6.1.1	Switch/NI Architecture	79
6.1.2	Dynamic NoC Reconfiguration	79
6.2	Design Methodology	80
6.3	Use-Case Preprocessing	82
6.4	Unified Mapping–NoC Configuration	83
6.5	Simulation Results	89
6.5.1	Experimental Benchmarks	89
6.5.2	Effect of Mapping for SoC Benchmarks	90
6.5.3	Frequency-Area Trade-offs	90
6.5.4	Dynamic Configuration	92
6.5.5	Parallel Use-Cases	93
6.6	Summary	93
7	Supporting Dynamic Application Patterns	95
7.1	NoC Design Challenges for CMPs	95
7.2	Basics of the Synthesis Approach	97
7.3	Design Flow	98
7.4	Problem Formulation	99
7.5	Synthesis Algorithm	101
7.5.1	NoC Link Sizing	102

7.5.2	Timing Feasibility Check	105
7.5.3	Algorithm Run-Time	105
7.6	Experimental Results	105
7.6.1	Experiments on a Mesh Topology	106
7.6.2	Effect of Core Injection Rates	107
7.6.3	Effect of Different NoC Sizes	108
7.6.4	Effect of Link Length	110
7.6.5	Application to Torus Topology	110
7.6.6	Validating Design Flow Predictability	111
7.7	Summary	112

Part II NoC Reliability Mechanisms

8	Timing-Error Tolerant NoC Design	117
8.1	The Double Sampling Technique	118
8.2	Using Links as a Storage Medium	120
8.3	<i>T-error</i> Link Designs	123
8.3.1	Scheme 1: Low overhead <i>T-error</i> Links	123
8.3.2	Scheme 2: High-Performance <i>T-error</i> Links	126
8.4	Aggressive Switch/NI Design	128
8.4.1	Output Buffer Changes	128
8.4.2	Input Buffer Changes	129
8.5	Dynamic Configuration of the NoC	130
8.6	Experimental Results	131
8.6.1	Simulation Platform	131
8.6.2	Experiments on a Multi-Media Benchmark	131
8.6.3	Effect of Application-Level Power Management	134
8.6.4	Experiments on Other Benchmarks	134
8.6.5	Effect of NoC Configuration	138
8.6.6	Choice of Link Design Schemes	138
8.6.7	Synthesis Results	139
8.7	Summary	139
9	Analysis of NoC Error Recovery Schemes	141
9.1	Switch Architecture Design	142
9.1.1	End-to-End Error Detection	142
9.1.2	Switch-to-Switch Error Detection	143
9.1.3	Hybrid Single Error Correcting, Multiple Error Detecting Scheme	143
9.2	Energy Estimation and Models	144
9.2.1	Energy Estimation	144
9.2.2	Error Models	144
9.3	Experiments and Simulation Results	144
9.3.1	Power Consumption of Schemes for Fixed Residual Error Rates	144
9.3.2	Performance Comparison of Reliability Schemes	146

9.3.3	Power Consumption Overhead of Reliability Schemes . . .	146
9.3.4	Effect of Buffering Requirements, Traffic Patterns and Packet Size	149
9.4	Summary	151
10	Fault-Tolerant Route Generation	153
10.1	Multi-Path Routing with In-Order Delivery	155
10.2	Path Selection Algorithm	156
10.3	Multipath Traffic Splitting	160
10.4	Fault-Tolerance Support with Multipath Routing	161
10.4.1	Resilience Against Transient Errors	161
10.4.2	Resilience Against Permanent Errors	162
10.5	Simulation Results	164
10.5.1	Area, Power and Timing Overhead	164
10.5.2	Case Study: MPEG Decoder	164
10.5.3	Comparisons with Single-Path Routing	165
10.5.4	Effect of Fault-Tolerance Support	166
10.6	Summary	167
11	NoC Support for Reliable On-Chip Memories	169
11.1	Analysis of Multimedia Software	170
11.2	Baseline SoC Architecture and Extensions	172
11.2.1	SoC Template Architecture	172
11.2.2	Proposed Hardware Extensions	173
11.3	Run-Time Fault Tolerant Schemes	176
11.3.1	Permanent Error Recovery Support	177
11.3.2	Intermittent Error Recovery Support	178
11.4	Experimental Results	178
11.4.1	Performance Studies	179
11.4.2	Architectural Exploration of NoC Features	182
11.4.3	Effects of Varying Percentages of Critical Data	183
11.4.4	Synthesis Results	184
11.5	Summary	186
12	Conclusions and Future Directions	187
12.1	Putting It All Together	187
	Bibliography	191



<http://www.springer.com/978-1-4020-9756-0>

Designing Reliable and Efficient Networks on Chips

Murali, S.

2009, X, 198 p., Hardcover

ISBN: 978-1-4020-9756-0