Preface

The complexity of *Multiprocessor Systems on Chips* (*MPSoCs*) is growing rapidly with the advances in semiconductor technology. The number of processors, hardware cores, and memories on a single chip is increasing and a highly-scalable communication infrastructure is required to connect them. To effectively tackle the interconnect complexity of current and future MPSoCs, a communication-centric design approach, *Networks on Chips* (*NoCs*), has recently emerged. NoCs bring the networking principles for data transfer, such as those used in large area networks (e.g., the Internet), to the on-chip domain.

Developing NoC-based systems tailored to a particular application domain, satisfying the application performance constraints with minimum power-area overhead is a major challenge. With technology scaling, as the geometries of on-chip devices reach the physical limits of operation, another important design challenge for NoCs will be to provide dynamic (run-time) support against permanent and intermittent faults that can occur in the system.

The purpose of this book is to provide state-of-the-art methods to solve some of the most important and time-intensive problems encountered during NoC design. We present methods for topology synthesis, mapping of cores onto NoC topologies, crossbar sizing, route generation, resource reservation, achieving fault-tolerance, RTL code, and layout generation. We show how the different design methods can be integrated to make a complete tool flow for designing reliable and efficient NoCs for application-specific MPSoCs and chip multiprocessors. To have less design respins and faster time-to-market, we show how the architectural synthesis models can be integrated with back-end physical design tools and models, thereby bridging a big design gap in on-chip interconnect synthesis.

Key features of book:

- Presents in depth the state-of-the-art algorithms and optimization models for performing system-level design of NoCs
- Presents an integrated flow to design interconnect architectures that can lead to faster time-to-market and design closure
- Shows evolution of design methods from complex crossbar based buses to NoCs
- Presents static and run-time methods for achieving reliable operation of the NoC and the entire system

This book should be of interest to:

- System level architects and designers: The methods show how to improve design productivity and achieve design closure of SoCs.
- Communication architecture/interconnect designers: The methods show trade-off analysis and explorations of NoCs.

- Design automation engineers: The high-level synthesis methods and mathematical models presented in this book can be applied to solve several communication architecture issues. They are also of general interest to designers working in related fields, such as sensor, body-area, and automotive networks.

This book is based on my Ph.D. research work done at Stanford University. I am greatly indebted to my adviser Prof. Giovanni De Micheli and co-adviser Prof. Luca Benini (University of Bologna), as they were instrumental in shaping the ideas presented here. The work is a result of collaboration with many researchers. I thank all my collaborators: Dr. Federico Angiolini and Antonio Pullini of iNoCs, Prof. David Atienza (EPFL), Dr. Kees Goossens and his team (Dr. Andrei Radulescu, Martijn Coenen, Andreas Hansson) at NXP research, Prof. Davide Bertozzi (University of Ferrara), Rutuparna Tamhankar (Marvell Technology), Prof. N. VijayKrishnan, Prof. Mary Jane Irvin and Dr. Theocharis Theocharides at Pennsylvania State University, Prof. Salvatore Carta, Paolo Meloni and Prof. Luigi Raffo of University of Cagliari for their contributions to this work.

EPFL, Lausanne, Switzerland Srinivasan Murali

http://www.springer.com/978-1-4020-9756-0

Designing Reliable and Efficient Networks on Chips
Murali, S.
2009, X, 198 p., Hardcover
ISBN: 978-1-4020-9756-0