

## Chapter 2

# Dielectric Materials

### 2.1 Introduction

Copper (Cu) has higher *conductivity* and resistance to *electromigration* (EM) than aluminum (Al) and has been the choice of the semiconductor industry for inter-connecting metal in sub-100 nm devices. With rapidly *decreasing feature sizes* and more demand for circuit *speed*, low- $K$  and passivation materials have been inserted with Cu-interconnects to address the additional  $RC$  delay reduction [1–2]. Unfortunately, as the thickness of the gate oxide becomes very thin because of the scaling down of channel length, quantum mechanical *tunneling* occurs for voltages below the Si/SiO<sub>2</sub> barrier height which is approximately 3.1 eV [3–4] (Fig. 2.1).

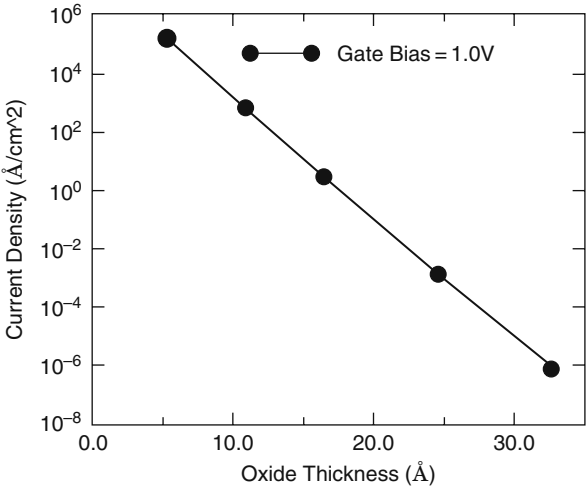
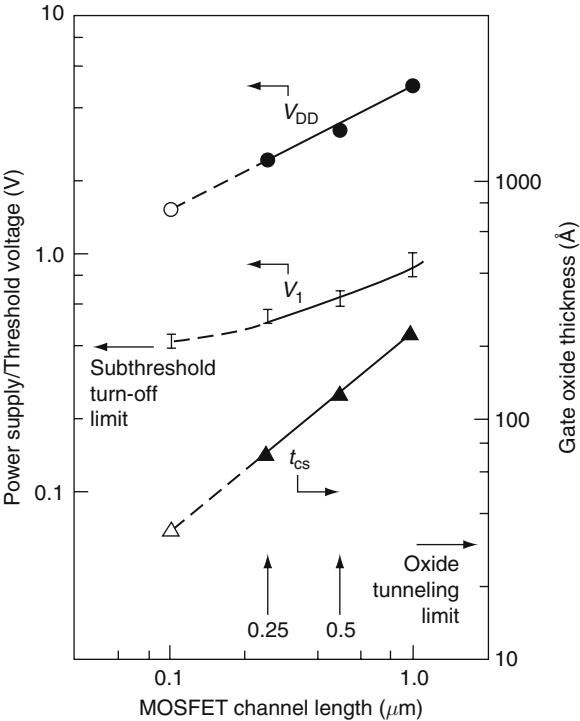
Figure 2.2 shows the simulated results of gate oxide scaling and the current density when the applied gate voltage is 1 volt. As the thickness of silicon dioxide (SiO<sub>2</sub>) as the gate material becomes very thin (less than 1.5 nm), the tunnel current increases significantly.

Therefore, the need exists for a dielectric material with high  $K$  ( $K$  is the dielectric constant of the material), which will provide the required electrical properties. Calculations based on experimental data show that the threshold voltage and transconductance fluctuations become major issues when the gate oxide thickness is scaled down to less than 1 nm. Figure 2.3 shows that the thinner the gate oxide, the greater the shift in threshold voltage. As a matter of fact, instability is more severe for static negative bias temperature (SNBT) than dynamic negative bias temperature (DNBT) [5].

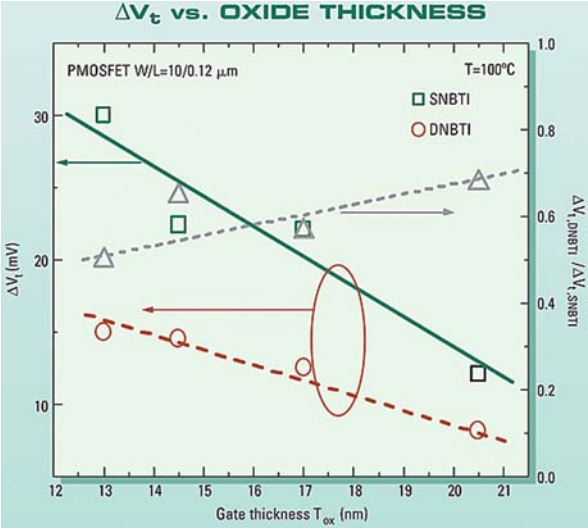
According to some experts, the NBTI is thought to be an electrochemical activity that involves the electric field, holes, Si–H bonds, and temperature. Interface traps are formed when hydrogen (H<sub>2</sub>) is released from the Si–H bond. Figure 2.4 shows some of the possible chemical activities and probable reasons for instability due to negative bias temperature (NBT). However, it is expected that using a recessed SiGe source/drain (S/D) with an elevated S/D structure will minimize the effect [6].

This chapter will be devoted to dielectric materials (low- $K$  and high- $K$ ) – the second most important material in the copper damascene process. Figure 2.5 shows the Cu-damascene architecture with low- $K$  materials into the trenches and via holes.

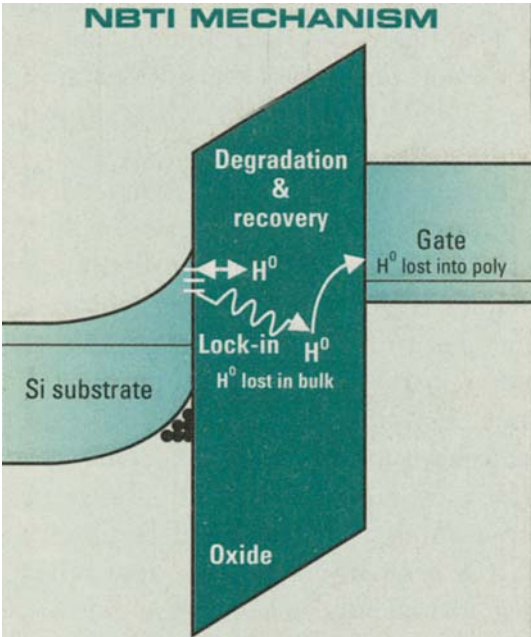
**Fig. 2.1** The effect of gate oxide on channel length and its consequences on the oxide-tunneling limit (Reprinted with permission, IBM Research [3])



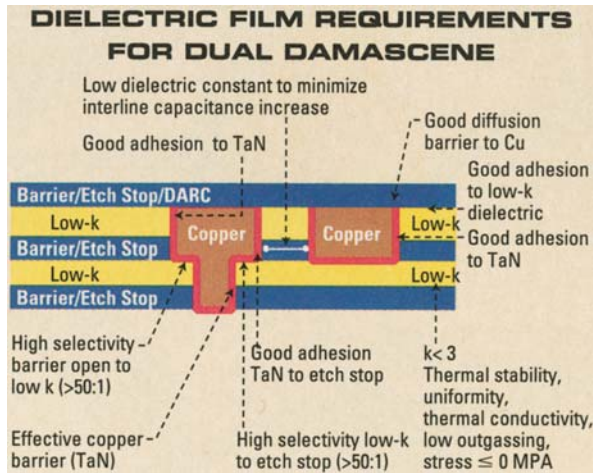
**Fig. 2.2** Simulated direct tunneling current density versus gate oxide thickness for  $V_{GB} = 1.0$  V



**Fig. 2.3** The dependency of the threshold voltage ( $V_t$ ) on the thickness of the gate (S = source, D = Drain, and NBTI = Negative bias temperature instability) (Reprinted with permission, Semiconductor International, March 2004, p. 48)



**Fig. 2.4** Breaking up of the Si-H bond, release of hydrogen ( $H_2$ ), re-passivation of the bonds, and lock-in when  $H_2$  is no longer available (Reprinted with permission, Semiconductor International, March 2004, p. 48, Courtesy, Intel Corp.)



**Fig. 2.5** The damascene architecture with low- $K$  materials in the trench and via holes (Reproduced with permission, Applied Materials)

*Dielectrics* or electrically *insulated* materials are understood as materials in which electrostatic fields could persist for a long time. The materials offer a very high resistance to the passage of electric current, and have been used as thin films in electronic circuits. In conventional silicon planar devices, deposition of resistors, capacitors, and their connections are made on stable insulating substrates like silicon dioxide ( $\text{SiO}_2$ ). Thin insulating dielectric films are used in a wide variety of components. The films are usually amorphous or near amorphous in nature and they show higher electrical resistance compared to polycrystalline or crystalline thin films. In integrated circuit (IC) dielectric materials are used as *insulating layers between conducting layers, diffusion and ion implantation masks, capping material for doped films to prevent loss of dopants, passivation layers to protect devices from impurities, moisture and scratches, sandwich material between two electrodes to form a capacitor, and gate oxide* [1–2].

The thin film dielectric materials that are most commonly used in exploratory  $RC$  ( $R$ , is resistance, and  $C$  is capacitance of a circuit) circuit applications are inorganic substances, mainly the oxides, and halides of metals and semiconductors. However, scaling down of the devices and the complexity of the integrated circuits (ICs) have stimulated the development of inorganic, organic and hybrid dielectric materials to deal with  $RC$  problems [7]. In comparing the properties of different dielectric materials it is convenient to use the capacitance density, which is defined as the capacitance per unit area, and is related to the *dielectric constant* ( $K$ ) and the dielectric thickness of the material. The other important electrical properties of a dielectric material are its breakdown voltage, and dielectric strength. The breakdown voltage of a dielectric is dependent on the thickness and dielectric strength of the dielectric material. The dielectric strength for most of the dielectric film materials that have been used in conventional ICs is between  $10^6$  and  $10^7 \text{ Vcm}^{-1}$ .

The inorganic dielectric materials that are now being used or are under investigation for future high- $K$  dielectric materials are silicon monoxide ( $\text{SiO}$ ,  $K \sim 5.0$ ), silicon dioxide ( $\text{SiO}_2$ ,  $K \sim 3.9$ ), silicon nitride ( $\text{SiO}_3\text{N}_4$ ,  $K \sim 6$ ), alkali halides (rubidium bromide,  $\text{RbBr}$ ,  $K \sim 4.7$ , lithium fluoride,  $\text{LiF}$ ,  $K \sim 9.2$ ), barium titanate ( $\text{BaTiO}_3$ ,  $K$  varies between 130 and 1000), lead titanate ( $\text{PbTiO}_3$ ,  $K$  is between 200 and 400), and metal oxides (hafnium oxide  $\text{HfO}_2$ ,  $K \sim 40$ , tantalum oxide,  $\text{TaO}_5$ ,  $K \sim 27$ , tungsten oxide,  $\text{WO}_3$ ,  $K \sim 42$ , and zirconium oxide,  $\text{ZrO}_2$ ,  $K \sim 24.7$ ).

Linear dielectric materials show a direct proportionality between the electric moment  $p$  (induced) acquired by the particle during the process of *polarization* and the intensity  $E$  of the electric field acting on the particle in question. The *polarizability* ( $\chi_e$ ) of a dielectric is defined as the electric dipole moment  $p$  per unit volume divided by the electric field ( $E$ ) and the permittivity of free space  $\epsilon_0$ . The dielectric materials having low polarizabilities are better in designing low- $K$  materials. It has been observed that materials having single C–C and C–F bonds have the lowest electronic *polarizability* ( $\approx 0.531$  and  $\approx 0.555 \text{ \AA}^3$  respectively), making fluorinated and non-fluorinated aliphatic macromolecules potential candidates for low- $K$  applications [8–9]. Conversely, materials having double and triple bonds show higher electronic polarizability because of increased mobility of  $\pi$ -electrons ( $\text{C}=\text{C} \approx 1.643$ , and  $\text{C}\equiv\text{C} \approx 2.036 \text{ \AA}^3$ ). In general, materials with low polarizability having low dielectric constants show poor adhesion property. In contrast, aromatic  $\pi$  bonding configurations have higher bonding strength. Experimental observations show that increasing the bond length, bonding orientation, as well as discontinuing the chain by inserting single bond atoms or groups of atoms into the main structure, can also lower the  $K$  value of a material.

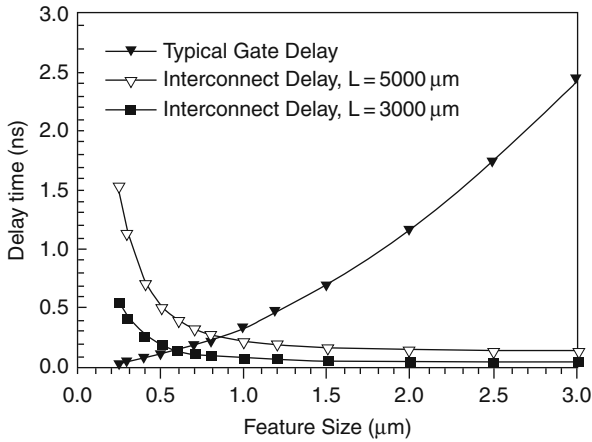
Advances in silicon ultra-large-scale integrated (ULSI) technologies have historically been made by scaling of the device dimensions. As a result, to minimize signal delay a reduced resistance,  $R$ , of the metal wiring and a reduced capacitance,  $C$ , of the encapsulating interlayer dielectric (ILD) line are required [1]. Thus the effort in the development of organic low- $K$  dielectric materials has centered around inorganic dielectric materials. These organic dielectric materials offer highly desirable electrical and mechanical properties. At the same time for future sub-100 nm devices the thickness of the gate oxide will reach a value less than 1.5 nm, which will require high- $K$  materials to lower the leakage current and tunneling. This chapter will be devoted to low- $K$  and high- $K$  dielectric materials, their characteristics, and deposition methods.

## 2.2 Interlayer Dielectric (ILD)

### 2.2.1 Introduction

Aluminum (Al) metal lines and silicon dioxide ( $\text{SiO}_2$ ) as dielectric material have been used so far in conventional integrated circuits (ICs). But as the circuit lines changed to  $0.18 \mu\text{m}$  in width from  $0.25 \mu\text{m}$ , the limiting factor in computer processor speed shifts from the transistors' gate delay to the interconnect delay caused by

the Al-interconnects and SiO<sub>2</sub> (dielectric material). As a result, the interconnect  $RC$  delay (Fig. 2.6) becomes the major factor, which limits device performance [7].



**Fig. 2.6** The effect of feature size on the gate and interconnect delay (Reprinted with permission IEEE [7])

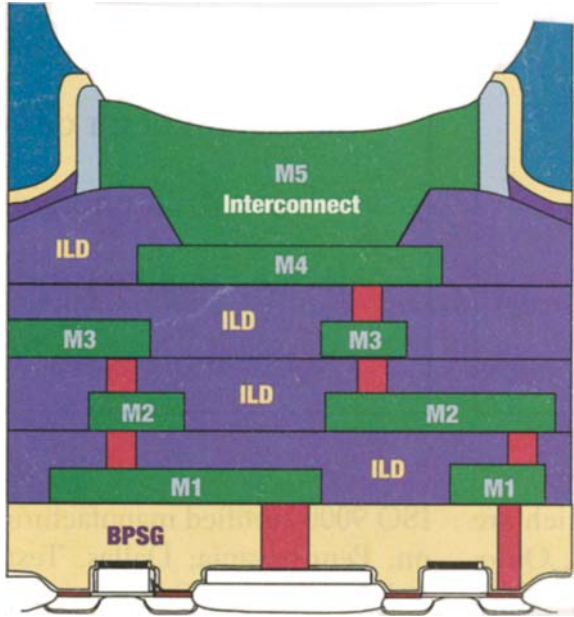
Thus the need to introduce advanced interconnect and dielectric materials becomes essential to limit the number of metal levels, die size and to reduce  $RC$  delay in *ultra-large-scale integrated (ULSI) circuits*. Figure 2.7 shows a multilayer metallization scheme with interlayer dielectric (ILD).

Technological innovation leads to the development of Cu-interconnect technology to replace Al- interconnecting lines since it will lower the line resistance ( $R$ ) and improve electromigration reliability. Further requirements of the reduction of  $RC$  delay depend on the value of the stack and inter-electrode capacitance (Fig. 2.8).

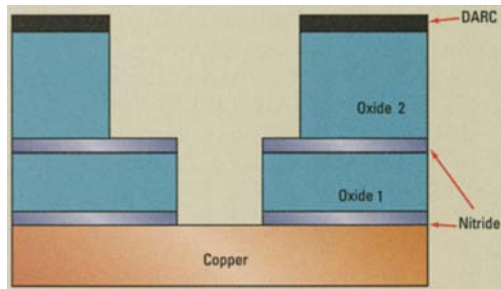
The gate oxide thickness has reached a level where SiO<sub>2</sub> will not be able to provide adequate reliability (leakage current and tunneling). Therefore, there has been a continuous search for dielectric materials that will offer proper  $K$  values (both high- $K$  and low- $K$ ), electrical and mechanical properties better than SiO<sub>2</sub>, and better deposition processes to integrate the dielectric materials in sub-100 nm devices without much difficulty [1,7, 10–11].

The *dielectric constant*,  $K$ , of a specific material has three main contributions, namely *electronic*, *ionic (distortion)*, and *orientation*. The electronic contribution comes from the contribution of the electrons under an applied field and is related to the number of bonds per unit volume. Therefore for a particular class of dielectric material the electronic contribution is directly proportional to the density of the material. The ionic contribution represents the response of the atoms to an electric field and is dependent on the types of atoms (Si, C, H, N, F) present in the material. The last one, where the contribution is due to the orientation of the molecules under an applied field, is related to the structure of the material [12–13].

**Fig. 2.7** Multilayer metallization with interlayer dielectric (ILD) (Reprinted with permission, Air Products and Chemicals, Inc., 2002)



**Fig. 2.8** A typical dual-damascene film stack of different dielectric materials including dielectric antireflecting coating (DARC)



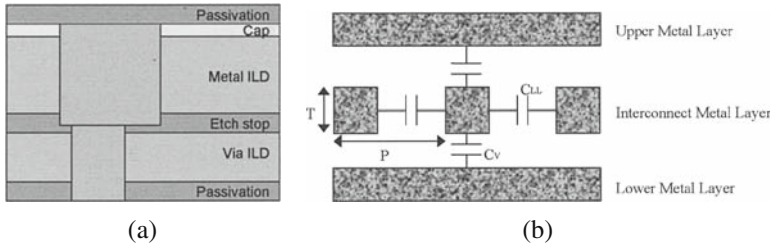
### 2.2.1.1 Low-K

There are two primary approaches to achieve low- $K$  dielectric materials. The first one is to lower the electronic contribution by the addition of fluorine (F) [14] and/or carbon (C) [15], which will provide the material with an inherently lower electronic polarizability. The second one is to lower the contribution due to the orientation and or the ionic contribution. This can be done by the introduction of a free volume in a material, which will decrease the number of polarizable groups per unit volume and will lower the atomic or dipolar contributions. Generally, the low- $K$  materials fall under three categories, namely inorganic, organic, and hybrid (organo-silicates).

Due to their hydrophobic nature and low polarizability, organic dielectric materials show lower  $K$  values than inorganic materials. However, inorganic materials retain a  $\text{SiO}_2$ -like matrix, which help them to integrate easily into the existing  $\text{SiO}_2$ -like processes. Hybrid materials, on the other hand, are typically doped with carbon (C) to take advantages of both organic and inorganic regimes. Once the base material is selected (organic/inorganic/hybrid), the next step is the integration of the material in the sub-100 nm device.

### 2.2.2 Mathematical Model

The demand for higher speed and overall performance of the ULSI circuits has prompted extensive development of *low- $K$  materials* for interlayer stacks (ILD/IMD). As the device down-sizes, the parasitic resistance and capacitance, i.e. *the RC effects*, become dominating factors for circuit performance. We can express the RC as:  $RC = 2\rho K \varepsilon_0 \{(4L^2/P^2) + L^2/T^2\}$ , where  $\rho$  is the interconnect resistivity in  $\Omega\text{-cm}$ ,  $K$  the dielectric constant of interlayer dielectric (ILD),  $\varepsilon_0$  the permittivity of free space,  $L$  the interconnect length in cm,  $P$  the interconnect pitch in cm, and  $T$  the interconnect thickness in cm (Fig. 2.9b). From the equation, we can see that by changing  $\rho$  and  $K$ , we can effectively minimize the value of RC [12].



**Fig. 2.9** (a) Schematic of ILD stack with many discrete layers (Reprinted with permission, AMD), and (b) equivalent circuit showing the effective capacitance within ILD layers (Reproduced with permission, Intel Corp.)

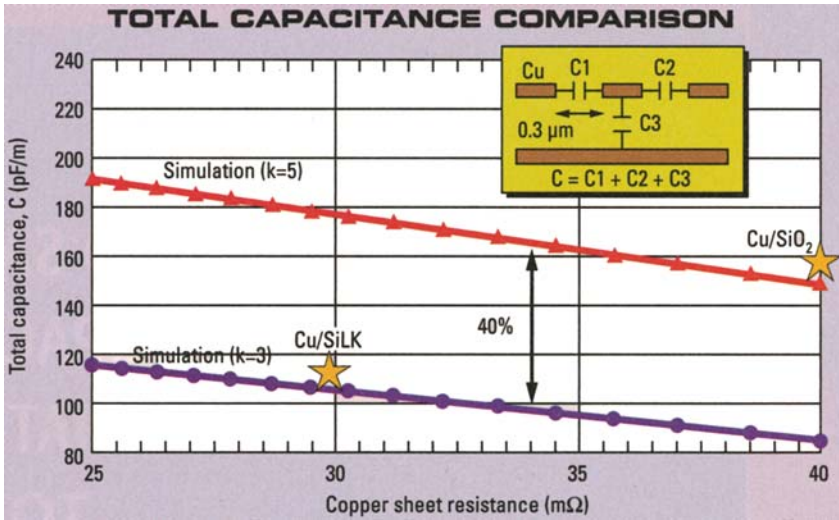
Figure 2.9a shows a schematic of an ILD stack with many discrete layers, and Fig. 2.9b represents the equivalent circuit showing the effective capacitance within ILD layers. The integrated  $K$  value of  $C_{LL}$  together with the  $K$  values of the other stacks will usually refer to the effective  $K$  value ( $K_{\text{eff}}$ ) of the full stack assuming that the films are homogeneous.

The  $K_{\text{eff}}$  value is a strong function of the thickness of the individual stack, and the materials used in the cap and passivation layers. Considering the effective resistance ( $R_{\text{eff}} = \{(2\rho L)/PT\}$ ) and the total capacitance  $C = (C_{LL} + C_V)$  we can write the total RC delay as:

$$RC = 2\rho K_{\text{eff}} \varepsilon_0 L^2 \{(4/P^2) + (1/T^2)\} \quad (2.1)$$



From the above equation it is clear that as the chip geometry drivers ( $P$  and  $T$ ) are decreased, and the interconnect length (as the device size shrinks) is increased, they will force the  $RC$  delay to increase. As a result the speed of the circuit will be affected severely. The dielectric constant ( $K$ ) of the ILD layer comes indirectly in the factor  $C$  of the  $RC$  delay and thus the selection of an ideal dielectric material with very low- $K$  will be a key to minimizing the  $RC$  effect. Figure 2.10 shows the effective capacitance effect of low- $K$  on Cu-interconnects.

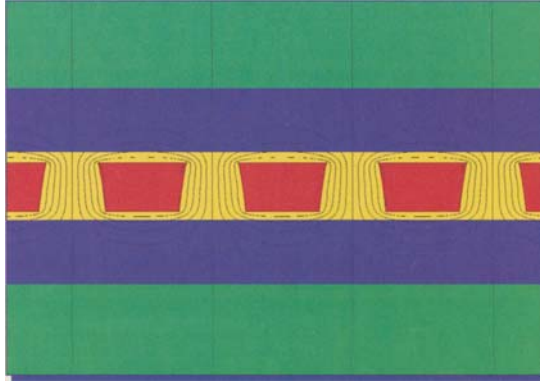


**Fig. 2.10** The effective capacitance effect of low- $K$  on Cu-interconnects (Reprinted with permission, Semiconductor International, June 2000, p. 118)

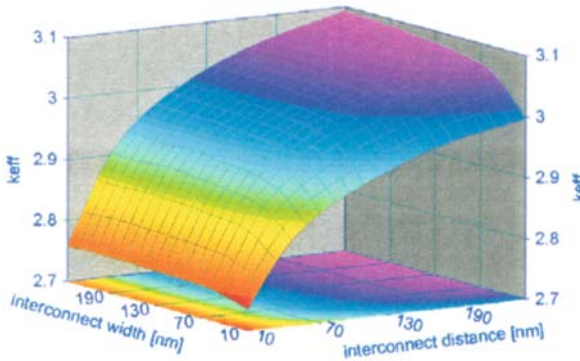
To extract  $K_{\text{eff}}$ , the capacitance between two inter-digitated combs is measured, and the dimensions of the combs (dielectric layer thickness and the metal line shape) obtained from cross-sections are entered into the model. The output of the model is matched to the measurement by varying the  $K$  value of the effective dielectric [12].

Figure 2.11 shows the results of capacitance simulations which have been used to extract the effective relative permittivities of interconnect structures by taking account of the bulk low- $K$ , the dielectric thin films below and above the metal line (such as the etch stop, hard mask, and cap).

Capacitance simulations (Fig. 2.12) take care of the thickness and the  $K$  values of the damaged side walls (from electron energy loss spectroscopy measurements), especially when the thickness of the dielectric layer reaches  $\leq 65$  nm. The predictive  $K_{\text{eff}}$  simulations show that side-wall damage can no longer be neglected in the development work when the design node is less than 65 nm.



**Fig. 2.11** The embedded metal inside the etch stop, bulk dielectric, hard mask, and cap. The combined structure gives rise to an effective dielectric (*broken lines* are equipotential lines) (Reprinted with permission Semiconductor International, July 2004, p. 87, Courtesy, SEMATECH, Austin, TX)



**Fig. 2.12** Simulated results for the effect of variation of geometrical dimensions on  $K_{\text{eff}}$  (Photo courtesy, Prof. T. Gessner, Chemnitz University of Technology)

### 2.2.3 Selection Criteria for an Ideal Low- $K$ Material

In order to increase the speed (improve  $RC$  delay) the dielectric layer should have low  $K$ , as well as reduce AC power dissipation ( $CV^2f$ , where  $C$  is the capacitance,  $V$  is the applied voltage, and  $f$  is the frequency of the applied voltage). The magnitude of the value of  $K$  is dependent upon the ability of the material to orient to the oscillations (frequencies) of an alternating electric field. As a matter of fact, the power consumed by the chip decreases as the interconnect capacitance is reduced.

The dielectric constant ( $K$ ) is a physical measure of the electric polarizability of a material and can be expressed as  $K = 1 + \chi_e$ , where  $\chi_e = M/E\epsilon_0$ ,  $\epsilon_0$  being the permittivity of free space,  $M$  the induced dipole moment per unit volume of

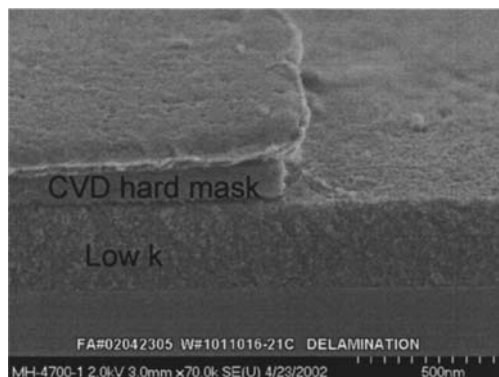
the dielectric, and  $E$  the applied field. Thus, the most obvious approach to synthesize a low- $K$  material is to choose a material with few polar chemical groups with symmetry to cancel the dipoles of chemical bonds between dissimilar atoms.

Low- $K$  dielectric materials have been targeted for better  $RC$  value to increase speed and to reduce interconnect cross-talk and bit-line capacitance for the memory chips [8]. It has been found that the devices are more susceptible to cross-talk at lower voltages and inductive coupling becomes more of an issue at higher operating frequencies.

The most important advantage of using the amorphous form of glassy silicon dioxide ( $\text{SiO}_2$ ), in conventional silicon devices, is ease of forming silicon dioxide ( $\text{SiO}_2$ ) by simple thermal oxidation [16]. But the disadvantages of  $\text{SiO}_2$  in the copper damascene process are: (a) oxygen ion vacancies from positively charged defects that might oxidize the cap layer (barrier) or copper to form ionized  $\text{Cu}^{+}/^{++}$  ions; (b) non-uniformity and voids in loose disordered networks, which can form diffusion paths for the intermediate layers; and (c) most important of all is its high dielectric constant value ( $K$  of  $\text{SiO}_2$  can vary between 3.9 and 4.9) [17].

Thus the need to introduce a low- $K$  material compatible with the copper damascene process becomes essential to reducing  $RC$  delay in ULSI circuits. The liner material (ILD) should satisfy a number of diverse specifications, including good conformality and continuity, good adhesion, and good electrical and mechanical properties. But any process change in the semiconductor industry is difficult, yet, choosing a new dielectric material has been (and continues to be) an exercise in trying to find a low- $K$  material with electrical, mechanical and thermal properties comparable to or better than  $\text{SiO}_2$ . Desired properties for these low- $K$  dielectric materials will depend on the applications and the chip architecture. Some of the fundamental requirements that a processed dielectric material should show in the sub-100 nm level devices are listed below:

- (i) dielectric constant should be below 3.0;
- (ii) good thermal stability at least at the processing temperatures of the device, and low coefficient of thermal expansion;
- (iii) good adhesion on the substrate and should be conformal after deposition;
- (iv) should have low thermal shrinkage, ability to resist cracking and compatible with chemical mechanical polishing (CMP);
- (v) should have an isotropic dielectric constant ( $K$ );
- (vi) high dielectric breakdown, low charge trapping and leakage current;
- (vii) low solubility in  $\text{H}_2\text{O}$  and low moisture absorption from the ambient;
- (viii) materials should be friendly to the environment and safe during handling;
- (ix) processing method should be simple and cost-effective;
- (x) should be chemically inert;
- (xi) should have high etch selectivity;
- (xii) good mechanical properties, i.e. the film should have enough mechanical strength to prevent cohesive failure, and interfaces *delamination* (Fig. 2.13).



**Fig. 2.13** Typical cap delamination failure (Reproduced with permission, AMD)

### 2.2.4 Search for an Ideal Low- $K$ Material

The variation in the dielectric constant is attributed to the frequency dependence of the polarization mechanisms that contribute to the dielectric constant ( $K$ ). The polarizability and  $K$  value of a dielectric material are generally results of the addition of three components (i.e. electronic + atomic + dipolar).

One approach to reduce the  $K$  value of a dielectric is to introduce carbon (C) or fluorine (F) atoms to increase the free volume of the matrix which will decrease the number of polarizable groups per unit volume. For example, in  $\text{SiO}_2$  ( $K = 3.9$ ), the introduction of C atoms to form  $\text{SiCOH}$  ( $K$  is between 2.7 and 3.3), and F atoms to form fluoro-silicate glass ( $K$  is between 3.2 and 4.0), and fluorinated polyimides ( $K$  is in between 2.5 and 2.9), reduces its  $K$  value. On the other hand, hydroxyl and carbonyl groups are polar functional groups which can attract water via hydrogen bonding and thus drastically increase the dielectric constant ( $K$  of water  $\sim 78.5$ ). Thus to formulate a low- $K$  material polar functionality containing elements like oxygen or nitrogen should be avoided.

The other approach that has been successfully implemented to reduce the  $K$  value is by introducing an air gap ( $K$  of air is 1) or pores. The addition of pores in a dielectric material is particularly challenging because the percentage of pores needed for low- $K$  dielectric materials is not an absolute number that can be applied across the film. Thus the overall dielectric constant of a material can be varied from that of a dense material down to the value of air ( $K = 1$ ) [18]. However, the porosity of a foam (static mixture) depends upon many factors, e.g. pore diameter, distribution of microstructure, and thickness of the pores (Fig. 2.16).

Based on this rationale, porous silica, referred to as silica xerogel, is synthesized by hydrolysis and condensation of tetra-ethylorthosilicate (TEOS). A great variety of formulas have been suggested for calculation of dielectric constant ( $K$ ) of these static mixtures (doped and porous dielectric materials) [19]. It is easy to calculate

the effective permittivity  $\varepsilon^*$  of a static mixture as:

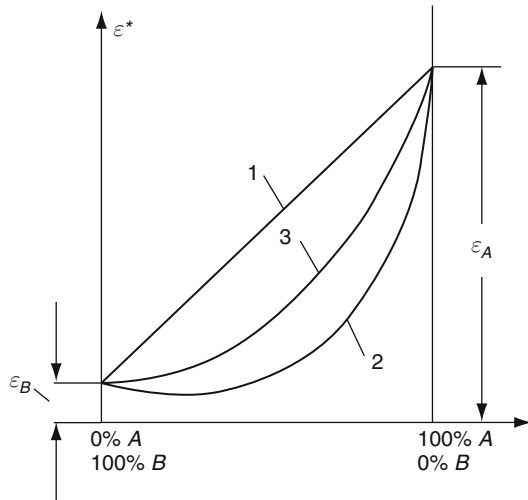
$$\varepsilon^* = \sum_{i=1}^{i=m} y_i \varepsilon_i \text{ (homogeneous connected in series)}$$

and

$$\varepsilon^* = \sum_{i=1}^{i=m} (y_i / \varepsilon_i) \text{ (homogeneous connected in parallel).}$$

where  $y_i$  is the volume content of the components,  $\varepsilon_i$  is the permittivity of the components, and  $m$  is the number of the components. Figure 2.14 shows the effective permittivity of two components A and B versus their volume content in the mixture.  $\varepsilon_A$  and  $\varepsilon_B$  are the permittivities of material A and B, respectively. 1, 2, and 3 refer to parallel connection, series connection, and statistic distribution of the mixture, respectively. Our low- $K$  dielectric materials (either doped or with pores) can be visualized as the static mixture of two materials.

**Fig. 2.14** The relative permittivity  $\varepsilon^*$  of a mixture of two components A and B mixed together vs. their volume content in the mixture (Reprinted with permission, MIR Publishers Moscow)



There are several formulas that have been developed for the calculation of permittivity of statistic mixtures. Among these, wide recognition has been given to the formula developed by Lichtenecker and Rother, which is known as the *logarithmic law of mixing*. The law can be mathematically expressed as:

$$\log \varepsilon^* = \sum_{i=1}^{i=m} y_i \log \varepsilon_i \quad (2.2)$$

For porous polymers with a vast number of small pores (porous low- $K$ ) the modified Lichtenecker–Rother equation fits very well and can be represented mathematically as:

$$\log \varepsilon^* = (D^*/D) \log \varepsilon \quad (2.3)$$

where

$\varepsilon^*$  = Permittivity of the foamed material = (mixture/matrix)

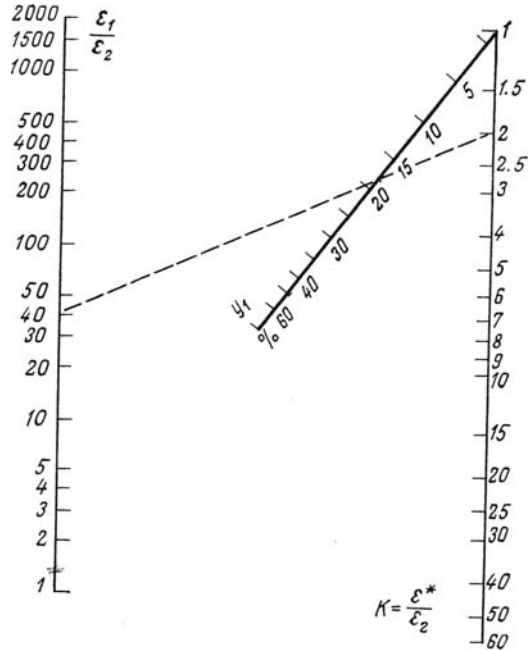
$\varepsilon$  = Permittivity of the solid material

$D^*$  = Volume mass of foamed material (mixture/matrix)

$D$  = Density of the solid material

Figure 2.15 illustrates a nomogram convenient for practical calculations plotted on the basis of Equation (2.2). The ratio  $\varepsilon_1/\varepsilon_2$  of permittivities of the components is plotted on the left vertical axis (assuming  $\varepsilon_1 > \varepsilon_2$ ). The volume content of the first component in the mixture, i.e.  $y_1$  (in percentage) is plotted on the inclined scale. The dotted line exemplifies the plot for the solution of a particular problem with a given ratio of  $\varepsilon_1/\varepsilon_2$  and the value of  $K$ .

**Fig. 2.15** Nomogram for calculations of dielectric constant of a mixture following Lichtenecker–Rother equation (Reprinted with permission, MIR Publishers Moscow)



After drilling through all these models a dielectric with permittivity  $\varepsilon_1$  incorporating uniformly distributed (by volume) spherical inclusion of a material with permittivity  $\varepsilon_2$  (volume concentration of inclusions  $y$ ) can be written as [19]:

$$\varepsilon^* = \{\varepsilon_1(2\varepsilon_1 + \varepsilon_2 + 2y(\varepsilon_2 - \varepsilon_1))/2\varepsilon_1 + \varepsilon_2 - y\varepsilon_2 - \varepsilon_1\} \quad (2.4)$$

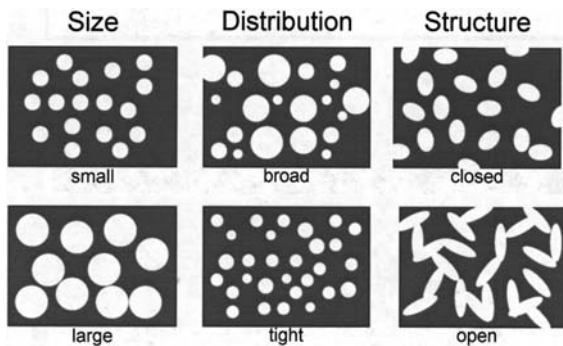
Equation (2.4) can be applied to calculate the effective dielectric constant ( $K_{\text{eff}}$ ) of the foam matrix (silesquioxane MSQ with pores).  $K_s$ ,  $K_p$ , and  $K_{\text{eff}}$  are the dielectric constants of the bulk MSQ, the pores, and the mixture (foam), and  $y$  is percentage porosity. We can set up a mathematical equation to calculate the effective dielectric constant of the porous MSQ. The equation can be written as:

$$K_{\text{eff}} = K_s \{ (1 + 2C) / (1 - C) \} \quad (2.5)$$

where  $C = y \{ (K_p - K_s) / (K_p + 2K_s) \}$ . Several investigators have calculated the effective dielectric constants ( $K_{\text{eff}}$ ) of porous dielectric materials applying different empirical formulas and have reported from time to time [20–23].

Figure 2.16 shows different sizes, distribution and structure of pores inside a low- $K$  porous dielectric material. The porous dielectric materials can be (a) a constitutive porous dielectric or (b) a subtractive porous dielectric [24]. In a constitutive porous dielectric, the material is deposited either by various sol-gel reactions – usually a combination of hydrolysis and condensation processes – or by controlling the  $S/V$  ratio, where  $S$  represents the internal surface area of the reactor and  $V$  represents the reactor volume. Constitutive dielectric materials can also be obtained by doping silica with carbon or fluorine. On the other hand, subtractive porosity is introduced either by sol-gel processes or through the use of sacrificial nanoparticles, called *porogens*, that are desorbed during film cure.

**Fig. 2.16** Different sizes, distribution and structure of pores inside a low- $K$  porous dielectric material (Reprinted with permission, AMD)



Commonly, the pores bearing low- $K$  materials like xerogel and aerogel films have relatively broad pores, whereas pores in the porogen additive dielectric depend on the size of the chosen *sacrificial nano-particles* [25]. Care must taken in the time of introducing pores so that a monotonic increase in connectivity should not degrade the film properties.

Silica based dielectric materials can be non-porous or porous. Porosity in these materials can be either constitutive with pore size of 1 nm or subtractive where the pore size can reach as high as 10 nm.

### 2.2.4.1 Problems with Porous Films

One of the key problems with porous dielectric materials is the diffusion of metallic precursors through the pores and subsequent degradation of its electrical properties. Besides, thermal conductivity of silica based porous low- $K$  materials is strongly dependent upon the porosity. As a matter of fact, with increasing porosity a strong decrease in thermal conductivity is observed (down to 0.3 W/m K at 50% porosity) [26–28]. The number of pores, pore size, and the distribution of the pores in the foam also affect the mechanical properties of the porous dielectric materials. For example, 45–50% porosity with subtractive techniques show an elastic modulus of around 2 Gpa or less. Besides, electrical properties and the adhesion of the porous dielectric materials are seen to decrease with percentage increase of porosity.

Swelling of low- $K$  porous materials in the presence of liquids results in delamination. The degree of swelling during adsorption depends on the overall rigidity of the film skeleton. Further, the effect of different etch chemistries, e.g. non-polymerizing  $\text{CF}_4/\text{O}_2/\text{Ar}$  (hard mask etch) versus polymerizing  $\text{C}_4\text{F}_8/\text{Ar}/\text{N}_2$  (low- $K$  etch), demonstrated undercut versus delay in the onset of damage. During reactive ion etching, porous low- $K$  dielectric materials forms  $\text{CF}_4$  compounds that decompose into volatile products, CO and  $\text{CO}_2$ . The depletion of carbon from these carbon containing compounds from the surface of the low- $K$  leaves behind several dangling silicon bonds that ultimately change the physical, mechanical and electrical properties of the low- $K$  dielectric materials.

Experimental data show that for  $\leq 65$  nm devices, the  $K$  value of the dielectric should be  $\leq 2.2$  which is primarily produced by introducing pores within the dielectric materials. Figure 2.14 shows different sizes, distribution, and structure of the pores in a porous film. One of the methods of introducing pores in dielectric films is by heating porogen. Unfortunately, the heating process leaves behind pores along with some carbon residue, which is conductive and dramatically reduces the breakdown voltage of the dielectric material. However, UV curing with the correct energy has been successful in minimizing carbon deposition compared to heating by electron beam or simple heating.

Once the pores are created, beam-positron annihilation lifetime spectroscopy (PALS) and transmission electron spectroscopy (TES) are used to study the void volumes and pore structures in the porous films [29–30]. The critical thickness of the porous films required in maintaining the continuity of the film is determined from the histograms of the peak height profile obtained from atomic force microscopy (AFM) [31–32].

Sometimes the pores can be interconnected (elongated, that is  $\sim 7$  nm or longer in pore size) and can form a large open area within the dielectric film (Fig. 2.14). PALS measurements can detect them. The presence of moisture or oxygen inside these open areas can contaminate the barrier layer and can form oxide. It is not unlikely for the trapped oxygen to leak to the copper layer to form  $\text{Cu}^{+}/^{++}$  ions and to migrate into the silicon layer.

The degradation in mechanical and thermal properties of the porous dielectric material compared to the dense virgin material has become a reliability issue.



Moreover, if the pores are not *sealed* properly they can absorb moisture and can react with fluorine-containing material to form hydrofluoric acid (HF), which is detrimental to the ILD stack and to the associated layers. The atomic layer deposition (ALD) method has been reported to be successful in sealing the pores of the porous low- $K$  material with silica [33–34].

#### 2.2.4.2 Pore Sealing

The methods of pore sealing are dependent on the nature of the pore structures (mesoporous, microporous with micro- and meso-connections), morphology and chemical nature of the surface bearing the pores. In order to avoid the problems encountered with porous dielectric films, the pores are not generally sealed until the value of  $K$  reaches below 2.5 or the film porosity reaches more than 30%. The most common method practiced for pore sealing is plasma ashing followed by either physical vapor deposition (PVD) or plasma enhanced chemical vapor deposition (PECVD). However, care must be taken to ensure that the penetration of the sealing material should not act as a barrier but will give a good surface fitting to the copper.

Needless to say, deposition of a pore sealant in the pores should be compatible with the low- $K$  dielectric with minimum thickness. Sealants like silicon oxycarbide, SiC:H, parylene, and benzocyclobutane (BCB) have been used so far and the results of their compatibility with low- $K$  dielectric materials have been reported from time to time [35–39].

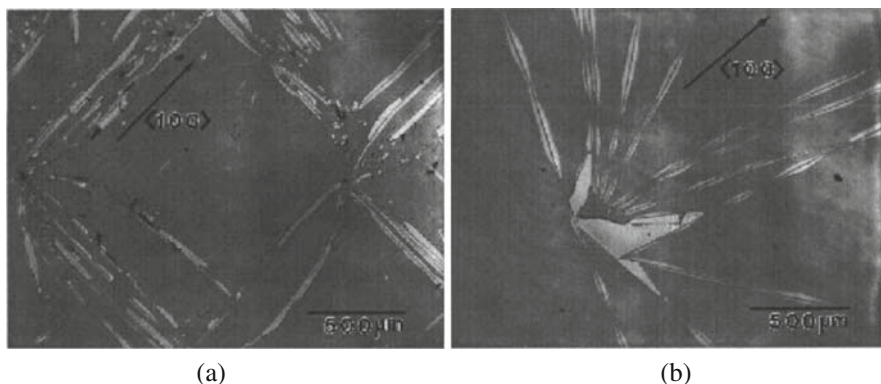
### 2.2.5 Achievement

#### 2.2.5.1 Porous Silicon Dioxide (SiO<sub>2</sub>) (the Xerogel)

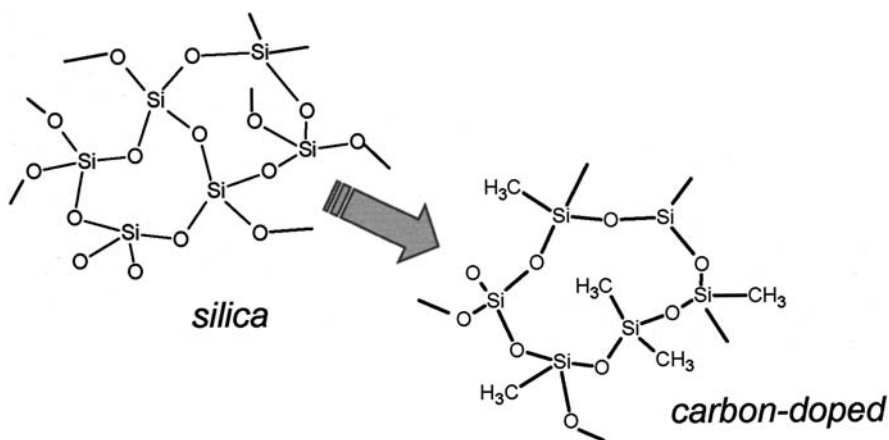
In order to lower the effective dielectric constant ( $K_{\text{eff}}$ ) of SiO<sub>2</sub>, pores are introduced inside the SiO<sub>2</sub> matrix. The porous silica is termed *xerogel*, and is prepared by hydrolysis and condensation of either tetra-ethyl-orthosilicate (TEOS) or its derivatives [33]. Depending on the porosity and the processing technologies the  $K$  value of a porous *xerogel* can vary from 1.3 to 2.5. A highly porous xerogel is called *aerogel* [11, 40]. Final porosity during spinning can be controlled by using solvents, such as ethylene glycol (EG) or dimethylsulfoxide [41]. The drawback with the porous xerogel film is that it shows cracking patterns (Fig. 2.17) when the film is thin (<1  $\mu\text{m}$ ) [42–43]. Experimental observations further show that all interfaces having energies below 5 J/m<sup>2</sup> lead to either film delamination or cracking and become a reliability threat during packaging and testing [44].

#### 2.2.5.2 Carbon Doped Oxide

The synthesis of a nanopore carbon doped oxide (CDO) is reported with atomic composition of Si : C : O : H as 20.5 : 14.5 : 31 : 34. The porosity of the film is detected as  $\sim 20\%$  with pore size of 1–4 nm. A 200 nm commercial CDO film



**Fig. 2.17** (a) Xerogel cracking on a  $\langle 100 \rangle$  Si-wafer, and (b) cracking on a  $\langle 111 \rangle$  silicon wafer (Photo courtesy, Prof. K.N. Tu, UCLA, CA)



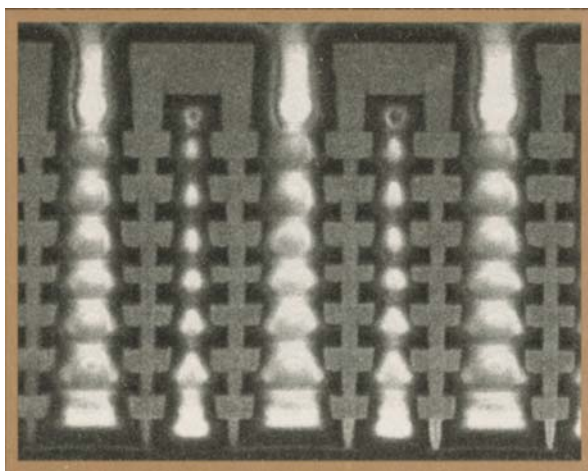
**Fig. 2.18** The structure of silica and carbon doped silica (Reprinted with permission, Prof. R.H. Dauskardt et al., Stanford University, CA)

(Orion) deposited by PECVD shows a  $K$  value less than 2.2, with excellent thermal stability up to 600 °C and a leakage current of 1 nA/cm<sup>2</sup> at 2.5 MV/cm. Figure 2.18 shows the structural change of silica when it is doped with carbon.

### 2.2.5.3 Black Diamond

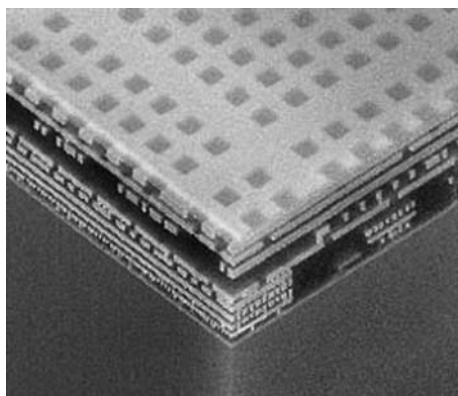
**Black Diamond (BD)** is a low-density silicon dioxide-like material formed generally by chemical vapor deposition (CVD). The precursors used include silicon-containing compound, typically an organosilane ( $\text{RSiH}_4$ ) and an oxidizer. The density and the  $K$  value (2.5–2.7) of the material can be controlled by appropriate choice of  $R$  (network terminating group). The CVD processed film is isotropic

and amorphous in nature. The measured leakage current and breakdown field of the film have been reported as  $\sim 5 \times 10^{-9} \text{ A/cm}^2$  at 1 V and  $>2.5 \text{ MV/cm}$ , respectively. An eight-level Cu/black diamond integrated architecture is shown in Fig. 2.19, and Fig. 2.20 shows a nine-level metal with black diamond dielectric layer which has been fabricated by following the 130 nm process technology.



**Fig. 2.19** Eight-level Cu/black diamond integration (Reprinted with permission, Applied Materials)

**Fig. 2.20** AMD's 130 nm process, which uses nine levels of metal, black diamond low- $K$  dielectric and BLOK dielectric barrier film (Photo courtesy Applied materials)



#### 2.2.5.4 Bezocyclobutene (BCB) Based Polymer

In the late 1980s bicyclo (4,2,0) octa-1,3,5,-triene or 1,2-dihydrobenzocyclobutene, a low- $K$  polymer, was formulated based on benzocyclobutene (BCB). Later on, a new formulation of BCB was reported as B-staged BCB which is a partially

cross-linked 1,3,-divenyl-1,1,3,3 tetramethyldisiloxane-bisbenzocyclobutene (DVS-bis-BCB), a monomer in mesitylene solvent [33]. Figure 2.21a shows the structure of BCB and Fig. 2.21b represents DVS-bis-BCB.

**Fig. 2.21** Chemical structure of (a) BCB and (b) DVS-bis-BCB

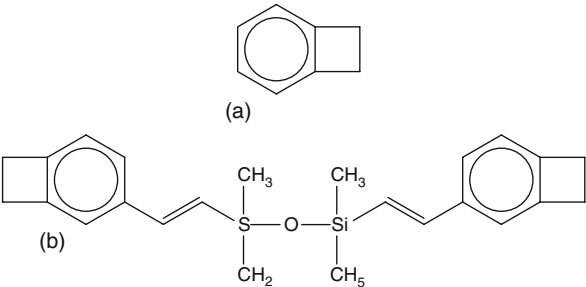


Table 2.1 shows some of the physical characteristics of bezocyclobutane (BCB). The dielectric *K* can be reduced further by the addition of fluorine (F). However, fluorine (F) readily attacks tantalum based barriers, leading to volatile TaF<sub>2</sub> formation and ultimately loss of adhesion in the interface layer. The disadvantage of using this material is its higher moisture intake, which makes the film vulnerable to cracking.

**Table 2.1** Characteristics of BCB dielectric film

Material	Dielectric constant (K)	Dielectric strength (V/cm)	Volume resistivity (Ω-cm)	CTE (ppm/ °C)	Thermal conductivity W/mK
BCB	2.49–2.65	3 × 10 <sup>6</sup>	1 × 10 <sup>19</sup>	52	0.29

[31,33,40, 43]

**2.2.5.5 Aromatic (Hydrocarbon) Thermosetting Polymer (ATP)**

Aromatic (hydrocarbon) thermosetting low-*K* polymer is receiving much attention for back-end-of-line (BEOL) applications in sub-100 nm node technology for its low moisture uptake and high fracture roughness [45]. The commercial product of ATP is *SiLK*– a cross-linked poly-aromatic matrix. It largely eliminates the nuclear polarizability component and shows high bond strength and excellent thermal resistance [46–47]. It is expected that this commercial product will serve the purpose of an ILD material in both Cu-damascene and Al-W systems. The polymer has an isotropic *K* value and some commercial houses are using this low-*K* dielectric material in a two-level Cu damascene process [44]. Figure 2.22 shows the structure of *SiLK*.

Figure 2.23 shows a scanning electron micrograph of the 130 nm Cu-damascene process architecture with *SiLK* as ILD [48].

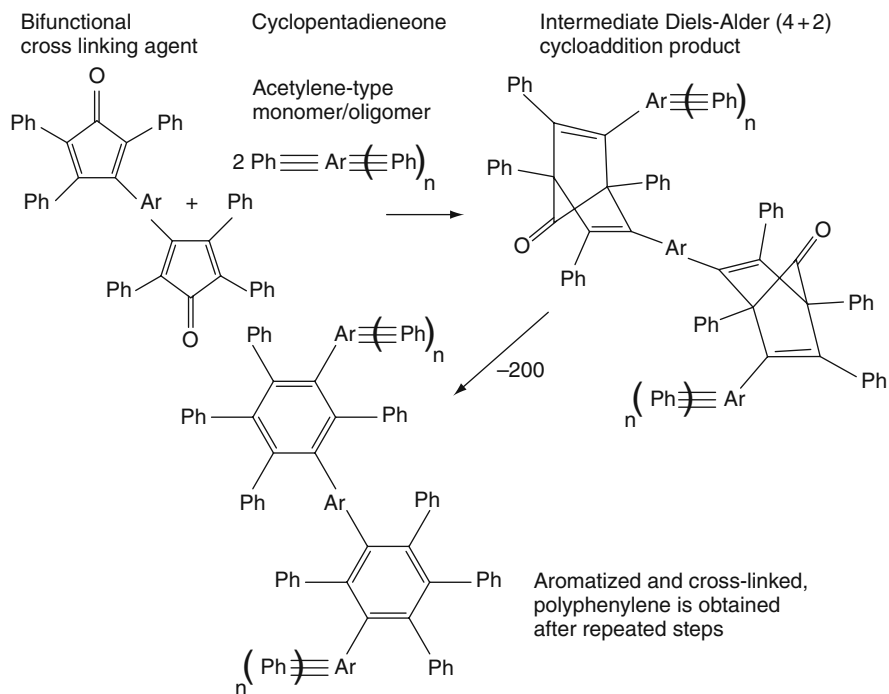


Fig. 2.22 Structure and synthesis of SiLK

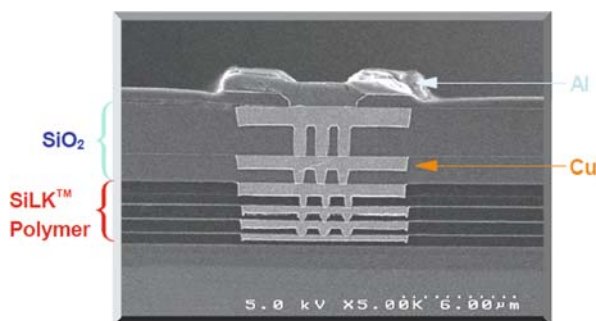


Fig. 2.23 Scanning electron micrograph of IBM's 130 nm Cu-damascene process with SiLK polymer (Reproduced with permission, IBM Research)

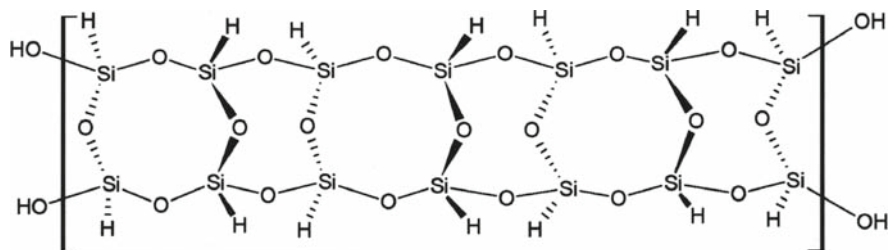
### 2.2.5.6 Hydrogen Silesquioxanes (HSQ, $\text{HSiO}_{1.5}$ )

The chemical formula for HSQ can be written as  $(\text{R Si}(\text{OH})_x\text{O}_{(3-x)/2})_n$  where R is hydrogen or a methyl group,  $n$  is an integer whose value is greater than 8, and the value of  $x$  is between 0 and 2. The reactive mixture is composed of chlorosilane ( $\text{RSiCl}_3$ ) and a polar organic solvent containing water or hydrogen. The solvent

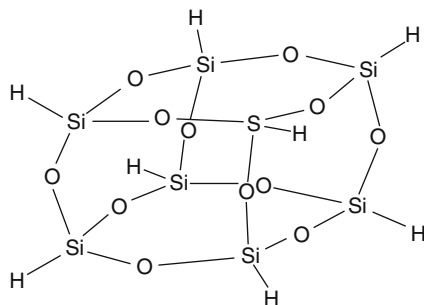
must be able to form hydrogen bonds with residual silanol ( $\text{Si-OH}$ ) groups [49]. Ethyl acetate or methyl isobutyl ketone is the possible solvent which has been used in the experiment [50]. The dielectric constant ( $K$ ) of HSQ is 2.9 [51], which can be further reduced either by introducing bonds with lower polarizability or by pores [52–53]. The nano-pore material forms an extra-low- $K$  (XLK) material with reduced density.

*FoX* (flowable oxide), a commercial product of HSQ, condenses at elevated temperatures and forms a ladder network. During annealing care must be taken so that there is no exchange of hydrogen and/or oxygen atoms from moisture, which could raise the  $K$ -value of the material due to the presence of silanol ( $\text{Si-OH}$ ) groups. In methyl silsesquioxanes ( $\text{MSQ}$ ,  $\text{RSiO}_{1.5}$ , where,  $R$  stands for  $\text{CH}_3$ ) this problem has been avoided by the substitution of the liable H atoms by hydrophobic organic  $R$  groups (Fig. 2.26). However, when an organic material is integrated into an inorganic resin matrix, they can segregate at the surface to lower their free energy, possibly leading to adhesion problems [48].

The synthesized HSQ can form two basic structures, namely a ladder structure (Fig. 2.24) and a cage structure (Fig. 2.25) and the film can be deposited by the spin-on-deposition (SOD) technique. The main drawback with HSQ is its thermal instability [54–57].



**Fig. 2.24** Ladder structure of hydrogen silsesquioxane (HSQ)



**Fig. 2.25** Another form of hydrogen silsesquioxane (HSQ) which resembles a cage structure

### 2.2.5.7 Methyl Silsesquioxane (MSQ)

Methyl silsesquioxane (MSQ,  $\text{CH}_3\text{SiO}_{1.5}$ ) is synthesized by the hydrolysis of methyl triethoxy silane [58–59]. Commercially available MSQ has a  $K$  value of  $\sim 2.7$ . Due to the presence of hydrophobic organic H atoms in MSQ, the hybrid polymer is protected from environmental oxygen to form any silanol groups that might increase its  $K$  value. Cross-linking (curing) takes place in MSQ through reactions of the alkoxy silyl groups on the oligomers. The main difference between HSQ and MSQ is that MSQ is more stable at high temperatures ( $400^\circ\text{C}$  and above) [49]. Figure 2.26 shows the ladder structure of MSQ.

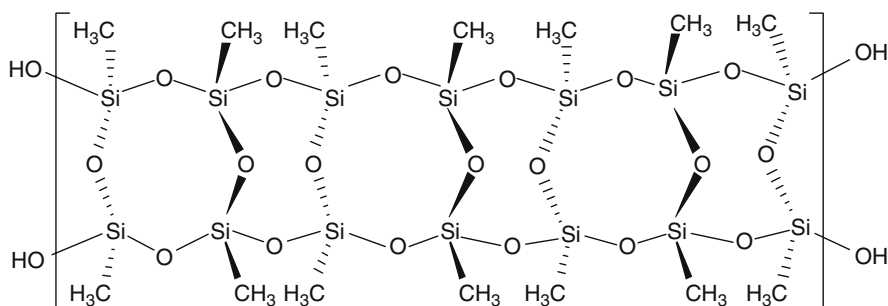


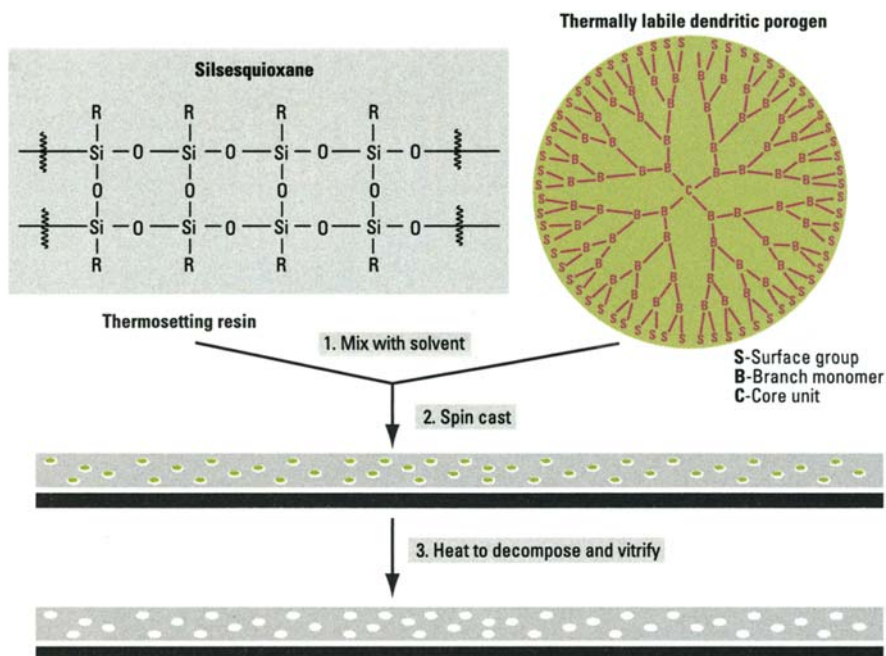
Fig. 2.26 Methyl silsesquioxane (MSQ) ladder structure

### Processing of Low-K MSQ

*Case I:* By varying the percentage of *porogen* (organic polymer) from 1 to 30% in MSQ the porosity and the pore size inside the hybrid polymer can be changed from 12 to 34% and from 10 to 15%. As a result, the dielectric constant of the foam is found to change from 3.5 to 2.5 (Fig. 2.26). However, the wall density is found to be independent of the porogen content [60].

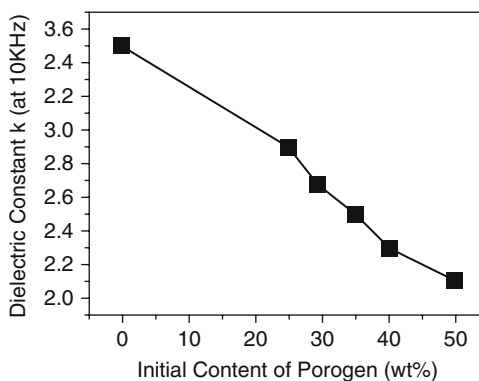
The inorganic–organic matrix gives rise to a hybrid system, which offers versatility and extendibility of the host matrix since the matrix material remains constant and only the loading of porogen varies [61]. Figure 2.27 shows the process sequence of blending thermosetting resin with dendritic polymer (porogen) and subsequent spin coating of the hybrid foam over a substrate. However, the main drawback of this hybrid matrix is that at elevated temperatures porogen decomposes and subsequently diffuses as a volatile product. Figure 2.28 shows the effect of porogen blending on the  $K$  (dielectric constant) value of the matrix.

*Case II:* Another way to change the  $K$  value of MSQ is to introduce an air gap by using a family of polynorbness [62–63]. It has been reported that the addition of 20% derivatives of norbornene (NB) polymer containing triethoxy silyl groups produces  $\sim 70$  nm pores in MSQ and it reduces the  $K$  value of the foam from 2.7 to 2.3. The voids created in this method exhibit a closed pore structure, which is advantageous from the standpoint of moisture intake. In addition to that, NB changes the number of pores but not their sizes.



**Fig. 2.27** The hybrid mix of inorganic silsesquioxane with organic porogen polymer solubilized in a common solvent (Reprinted with permission, IBM Research, [61])

**Fig. 2.28** The initial porogen content (wt%) in MSQ versus change in  $K$  value of MSQ (Reprinted with permission, R.H. Dauskardt, Stanford University, CA)

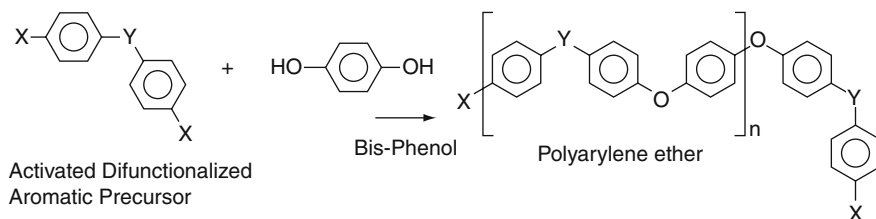


### 2.2.5.8 Poly (Arylene Ethers) (PAE)

Poly-arylene ethers (PAE) are synthesized by reducing bisphenol with activated defunctionalized aromatic precursor. The PAE family is a non-fluorinated polymer and shows a  $K$  value of  $\sim 2.8$ . The elimination of fluorine from the PAE has shown better results in the areas of low out-gassing after cure, thermal stability, low moisture uptake, good solvent resistance, and adhesion over the substrate [64]. The



commercial products of the PAE family are FLARE and VELOX [65]. FLARE is a bridged PAE with a dielectric constant of 2.5 and has shown thermal stability up to 400 °C [66]. Figure 2.29 shows the structure of a PAE family.



**Fig. 2.29** The structure of poly-arylene ether low- $K$  polymer

### 2.2.5.9 Parylene

Parylene is a common generic name for a unique series of polymers based on paraxylene. The thermoplastic polymer family is available in three trade names as: parylene N, parylene C, and parylene D [67]. The synthesis of the material is performed in a vacuum by pyrolysis of di-p-xylene (dimmer). The temperature during synthesis is very critical because it changes the morphology of the film from a homogeneous (non-porous) structure to a heterogeneous (porous) structure [68]. When fluorinated, parylene-N shows lower  $K$  (2.65–2.1) values but the adhesion of the co-polymer is impaired [70]. Experimental observations show that the CVD process produces films with better conformality and good gap filling compared to spin-on deposition (SOD) [69].

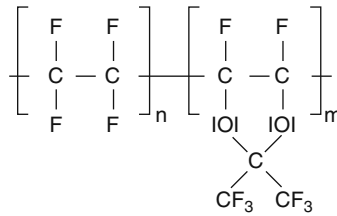
### 2.2.5.10 Teflon AF

This is a copolymer of tetrafluoroethylene and 2,2, -bis trifluoromethyl-4, 5-difluoro-1,3-dioxole [71], having optical and mechanical properties similar to other amorphous polymers including strength. The  $K$  value of the material is between 1.89 and 1.93, and it shows very good thermal and chemical stability at elevated temperatures [72].

The Teflon AF polymers are distinct from other fluoropolymers in that they are soluble in selected solvents, with high gas permeability, compressibility, creep resistance, and low thermal conductivity. The index of refraction of these polymers is between 1.29 and 1.34. Figure 2.30 shows the structure of the AF copolymer of Teflon and perfluoro-2,2-dimethyl-1,3-dioxole.

### 2.2.5.11 Diamond-Like Carbon (DLC)

DLC film shows high electrical resistivity and dielectric constant which can range from  $10^2$  to  $10^{16} \Omega\text{-cm}$  and 2.7–3.8, respectively, depending on the deposition conditions [73–74]. However, when doped with nitrogen, the film shows lower  $K$



**Fig. 2.30** The structure of Teflon AF<sup>®</sup>

(2.4–2.8) values and internal stress. A film of DLC can be deposited by the PECVD method using hydrocarbon as a precursor [75]. Besides the PECVD method, deposition of DLC has been reported by microwave plasmas [76], dc discharge, and ECR (electron cyclotron resonance) methods. DLC is an amorphous, metastable material and is grouped into four categories according to whether the material contains hydrogen or not [77].

### 2.2.6 Impact of Low-*K* ILD Materials on the Cu-Damascene Process

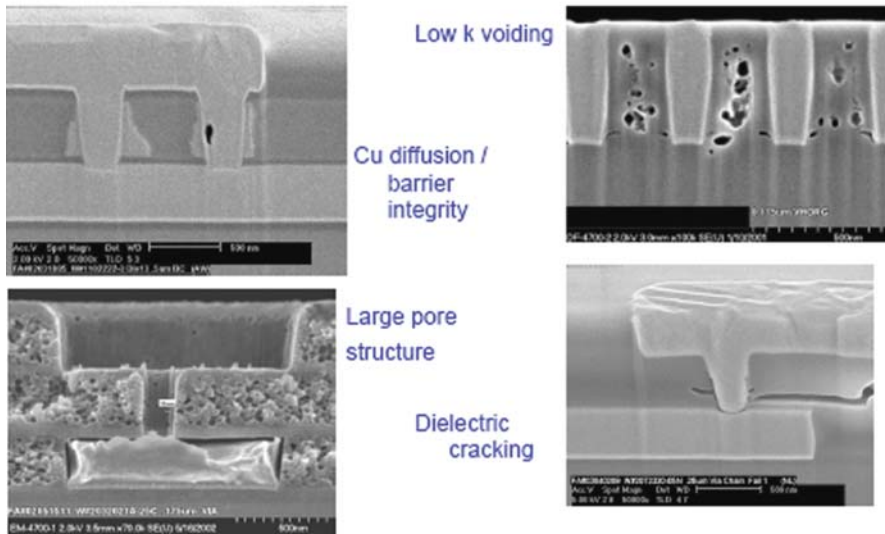
The choice of dielectric material has significant impacts on both lifetime and packaging reliability. Dual laid Cu-interconnect with low-*K* ILD has been introduced to address the *RC* delay reduction. However, porous low-*K* dielectric materials are generally less dense than SiO<sub>2</sub>. As a result, integration of low-*K* materials in a Cu-damascene architecture has become a challenge (Fig. 2.31).

The pores in the dielectric medium are supposed to be spheroid and the porous dielectric medium can be considered as a random composite medium. In order to address the reliability issues of the porous dielectric, the dielectric layer is sandwiched between passivation layers and/or the pores are filled with some different material. Thus the total *K* value of the dielectric has to be calculated from the effective *K* value (*K*<sub>eff</sub>) of the composite [78]. One way to determine the *K*<sub>eff</sub> value is to apply the effective medium theory developed by Bruggeman, which is presented mathematically as [79–80]:

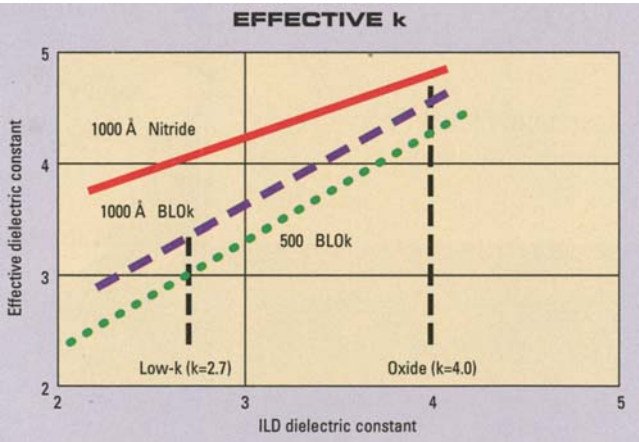
$$f_1 \{ (K_1 + K_{\text{eff}}) / (K_1 + 2K_{\text{eff}}) \} + f_2 \{ (K_2 - K_{\text{eff}}) / (K_2 + 2K_{\text{eff}}) \} = 0 \quad (2.6)$$

where *f*<sub>1</sub> and *f*<sub>2</sub> represent the fraction of the two dielectric materials having *K*<sub>1</sub> and *K*<sub>2</sub> values. The value of *K*<sub>eff</sub>, due to mixing of two dielectric materials, can be determined by substituting the values of *f*<sub>1</sub>, *f*<sub>2</sub>, *K*<sub>1</sub>, and *K*<sub>2</sub> in the above equation. Bruggeman's model helps us to choose a barrier layer and an etch stop for a particular ILD material. From Fig. 2.32, we can see how the change of barrier layer from silicon nitride based material to silicon carbide based material significantly influences the *K*<sub>eff</sub> value even before the low-*K* ILD is introduced.

# Low-k – Integration Challenges



**Fig. 2.31** Different challenges related to low-*K* integration in integrated circuits (ICs) (Courtesy, Peter J. Wolf)



**Fig. 2.32** The SiC based dielectric barrier impacts the effective *K* value much less dramatically than the traditional nitride film (Courtesy, Applied Materials)

The number of pores in a dielectric medium not only controls the *K* value but it also controls the mechanical strength and thermal conductivity of a dielectric film that ultimately controls the cracking, and delamination properties of the film [10]. The mechanical strength of a low-*K* dielectric material is important for

chemical mechanical polishing (CMP) operations, where the dielectric strength impedes  $\text{Cu}^{++/+}$  diffusion at higher electric fields (approximately 1 MV/cm or above) [81–82].

To integrate the low- $K$  dielectric material in Cu-interconnect structures it is helpful to sandwich them between capping stacks. The capping materials should also have low  $K$ , and should be compatible with photolithography processes [70]. Amorphous silicon carbide (SiC) [69] has low relative permittivity, good adherence properties on the substrate, high modulus and hardness [68], is chemically inert and moisture resistant [71–72], and has shown promising results as a capping material. Besides SiC, amorphous SiC:H has also been used as a cap layer and anti-reflecting coating (ARC) but dry etching of the material is hard. However, recent result shows that  $\text{Ar}/\text{CF}_4/\text{N}_2/\text{O}_2$  chemistry is able to dry-etch  $\alpha$ -SiC: H [75].

Fluorinated oxide shares many integration similarities with undoped plasma oxides and is being extensively developed as the next generation ILD material with  $K \sim 3.5$ . Fluorinating a dielectric is a common method of reducing  $K$  provided that the fluorine atoms are incorporated correctly. The external electric field cannot perturb the fluorine atom, because of its high electronegativity. Thus it is not possible to polarize it easily. But fluorine being a highly reactive element, excessive fluorination might corrode the metal and the dielectric.

Organic polymers, especially the polyimides, have good mechanical strength, thermal stability, and show high chemical resistance but their  $K$  values are typically more than 3.0. Moreover, they absorb moisture and show significant anisotropy in the dielectric constant. These shortcomings have stimulated the chemical industry to develop different families of low- $K$  dielectric materials that are tailored to ILD integration. These include polyarylene ethers, derivatives of cyclobutane, polynobornenes, amorphous Teflon<sup>®</sup>, phase separated inorganic–organic hybrids, parylene-N, parylene-F, polynaphthalene, and polytetrafluoroethylene [83].

Table 2.2 shows some of the promising materials for low- $K$  application in Cu-interconnects and their suitable deposition methods.

**Table 2.2** Low- $K$  dielectric materials

Materials	Dielectric constant	Deposition process
Silicon dioxide ( $\text{SiO}_2$ )	3.8–3.9	PECVD
Carbon doped $\text{SiO}_2$	2.2–2.7	PECVD
Bezocyclobutane (BCB)	2.49–2.65	Spin-on
HSSQ	2.9	Spin-on
MSSQ	2.7	Spin-on
Polyarelene (PAE)	2.8	Spin-on
Parylene-N	2.8	CVD
Parylene-F	2.3–2.5	CVD
Teflon AF	1.89–1.93	Spin-on
Diamond like carbon (DLC)	2.7–3.4	PECVD
Fluorinated DLC	2.4–2.8	PECVD
Aromatic thermosets (SiLK)	2.6–2.8	Spin-on

### 2.2.7 Deposition Techniques

Deposition methods for different materials frequently used in Cu-damascene processes have been presented in a separate chapter. In order to keep the flow of the damascene architecture, a brief outline of the low- $K$  deposition system is presented here. The chapters in the book have been arranged in sequence with the damascene process flow.

#### 2.2.7.1 Flow chart for Damascene Architecture

- (a) deposition of dielectric material;
- (b) pattern generation (to create trenches);
- (c) deposition of barrier layer;
- (d) Cu-seed layer;
- (e) electro-chemical deposition (ECD) of Cu;
- (f) planarization; and
- (g) via holes if necessary.

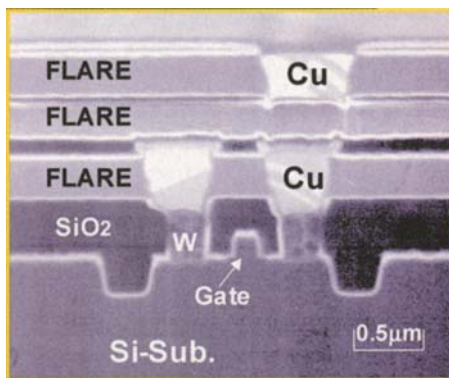
The deposition techniques used for the deposition of dielectric films include low-pressure processes such as physical vapor deposition (PVD), sputtering, plasma deposition, and chemical vapor deposition (CVD). The processes operating at atmospheric pressure may include thermal oxidation, conventional CVD, anodization, electrophoretic deposition, spin-on/spray-on technologies, screen printing and miscellaneous deposition processes, e.g. roller coating, offset printing, etc. [69–72]. Use of CVD processes offers an evolutionary approach for inter-metal low- $K$  dielectric materials (IMD) with transition from plasma enhanced CVD (PECVD)  $\text{SiO}_2$  to so-called organosilicate glass (OSG). However, the high plasma energy of PECVD is detrimental to the deposition of inorganic materials, especially the materials containing fluorinated amorphous carbon (FLAC).

Spin-on deposition (SOD), on the other hand, is very much like photoresist (PR) deposition, but the baking temperature of the SOD dielectrics is higher (400 °C and above) relative to the post-baking temperature of PR (130–140 °C). Many factors affect SOD processing, including track system cost, material cost (amount of material needed to coat), and track system throughput. Thus the process becomes very lengthy and expensive. Moreover, curing and pore generation at the same time are very difficult to achieve with SOD systems especially if the curing is done on a hot plate.

On the other hand, organic spin-on materials and inorganic CVD materials can be complementary, making hybrid integration a viable and attractive option. By eliminating process steps and allowing chip makers to use some of their current CVD equipment, the hybrid approach will allow the manufacturer to extend their knowledge in tackling the sub-100 nm node copper damascene process. It is most likely that organosilicate glass (OSG) will be the candidate for CVD technology while aromatic thermoset resin (ATR) could possibly be patterned with inorganic dielectric materials.

Thus there are two main strategies suitable for depositing low- $K$  materials: (a) SOD and (b) CVD. For both SOD and CVD processes there are methods and materials that are unique combinations for a particular system. However, SOD is considered to be the most widely used method. CVD films, on the other hand, have given the biggest accomplishment in sub-100 nm processes. CVD grown OSG has the capability of producing film with  $K < 2.5$  which is not possible to grow with other methods. Although the CVD process has been the mainstream deposition process for silicon based inorganic dielectric materials, there are some shortcomings in vapor deposition methods when the dielectric material is a polymer. Therefore, one can say that the degree of molecular control one can exercise with the SOD process is not possible with a CVD system. Figure 2.33 shows a commercial low- $K$  material (FLARE) which has been integrated in a Cu-damascene architecture.

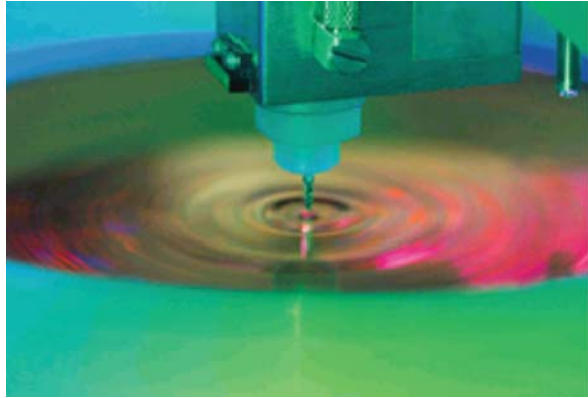
**Fig. 2.33** Scanning electron micrograph (SEM) of FLARE integrated into the damascene structure (Courtesy of Honeywell Corp.)



However, there are controversies about SOD low- $K$  materials and CVD carbon doped oxides. As a matter of fact, some of the spin-on organic varieties include polyarylene ethers, derivatives of cyclobutane, phase separated inorganic–organic hybrids, amorphous Teflon, xerogels, and polynorbornenes. On the other hand, the CVD alternative of organic polymers covers parylene-N and F, polytetrafluoroethylene (Teflon), and polynaphthalene. But when the mismatch of the coefficient of thermal expansion (CTE) between two adjacent materials is an issue, the use of low- $K$  SOD materials will be a matter of much concern. Moreover, delamination of SOD films at the point where interconnect via holes are attached to copper wire has been a troubling episode. Considering all of these facts, we can say that instead of using SOD or CVD alone, use of both in the 65 nm node technology might be a viable alternative.

Figure 2.34 shows a picture of a SOD coating system. Depending on the SOD material, the coat track design and processing requirements will differ. Generally, SOD track platforms are developed around resist tracks and are designed to continually remove evolved gases from the spin cup and hot plate areas.

**Fig. 2.34** The spin coating process (SOD) for dielectric materials used in the copper damascene process (Courtesy of Tokyo Electron Limited)



## 2.3 High-K Dielectric Materials

### 2.3.1 Introduction

The semiconductor industry is feverishly ferreting after a dielectric material for a gate which will provide a very high- $K$ , low leakage current and a low *equivalent oxide thickness* (EOT) compared to silicon dioxide ( $\text{SiO}_2$ ) [84–85]. The search is spurred by the urgency of minimizing power consumption, particularly in battery-driven high-performance sub-100 nm devices [86–87]. As the thickness of silicon dioxide ( $\text{SiO}_2$ ) approaches  $<1.5$  nm, the leakage current becomes  $>1$  A/cm<sup>2</sup> and the tunnel current is seen to increase significantly. Therefore, it is expected that the future high- $K$  materials for sub-100 nm node technology should provide excellent electrical characteristics such as dielectric constant ( $K$ )  $>30$ , interface density  $<1 \times 10^{11}$ /cm<sup>2</sup>-eV, tunneling current  $<10$  mA/cm<sup>2</sup>, and negligible hysteresis [88–90]. An important issue preventing the implementation of high- $K$  gate material is charge trapping in pre-existing traps inside the dielectric material, which affects the threshold voltage.

Scaling the thickness of the gate dielectric has long been recognized as one of the keys to scaling devices [91]. But when the oxide is made thinner, and the substrate doping is increased, the electric field applied to the oxide/silicon interface causes a significant quantization of the carriers perpendicular to the interface [92].

The International Technology Road Map for Semiconductors (ITRS) projected that for 45 nm node technology, the equivalent oxide thickness (EOT) should be  $<1.0$  nm. The EOT scaling is very much dependent on high- $K$  gate stacks, that include multilayer structures of  $\text{SiO}_2$  interfaces with silicon (Si) substrates, including deposited high- $K$  dielectrics. For efficient operation of the device, the interfacial layer created during surface preparation should have minimum interfacial charge to maximize channel mobility [93]. In addition to that, the high- $K$  dielectric layer deposited by oxidants (ozone,  $\text{O}_3$ ) during the CVD or PVD process should have

sufficient barrier height, minimum charge-traps [94], and reduced tunneling leakage and the metal gate electrodes should be electrically and thermally stable with controllable work function [95].

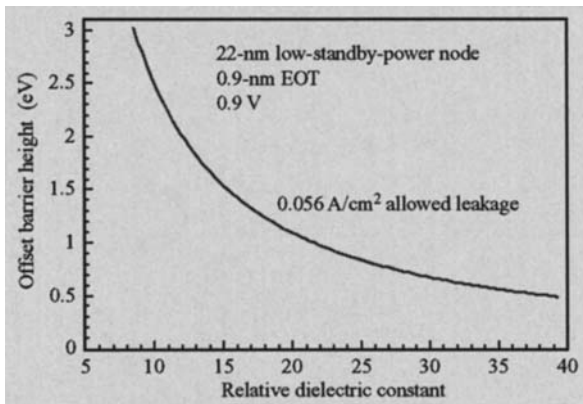
During device fabrication with high- $K$ , etching of Si wafer is generally done with hydrofluoric acid (HF) followed by an ammonium hydroxide ( $\text{NH}_4\text{OH}$ ) surface treatment. The operation reduces EOT but degrades mobility due to surface nitridation. On the other hand, chemical oxidation by ozone ( $\text{O}_3$ ) is seen to increase mobility at the expense of EOT. However, compared to chemical oxide, *in situ* steam generated interfaces exhibited better overall electrical performances.

Recently, oxides of the transition metals ( $\text{TaO}_2$  and  $\text{TiO}_2$ ) [96]  $\text{Al}_2\text{O}_3$  [97],  $\text{ZrO}_2$ , [98–99],  $\text{HfO}_2$ , [100–101], ferroelectric materials ( $\text{Pb}(\text{Zr,Ti})\text{O}_3$ ,  $(\text{Ba,Sr})\text{TiO}_3$ ) [102–104], and metal silicates ( $\text{ZrSi}_x\text{O}_y$ ,  $\text{HfSi}_x\text{O}_y$ ) [105–107] are showing promise for high- $K$  gate materials in sub-100 nm node technology.

### 2.3.2 Impact on Scaling and Requirements

The gate dielectric has not been scaled as rapidly as feature size. It is expected that by the end of 2015, the equivalent oxide thickness ( $\text{EOT} = (t_1 (\text{bottom}) - t_2 (\text{top})) (K_1/K_2)$ ) will be a few ångströms to minimize short channel effects and maximize device drive current. To meet all the stringent requirements of a sub-100 nm device, the gate dielectric must be physically thick, and it must have reasonably large band offsets to silicon (Si), so that it can minimize direct tunneling [88, 107–108].

On the basis of the requirement of ITRS [109] for a high- $K$  dielectric material, a relation between the required  $K$  corresponding to the offset barrier of the material has been established and is shown in Fig. 2.35. However, the tradeoff between offset barrier height and  $K$  should meet the leakage current specification of a 22 nm device at low-stand-by power mode [88].



**Fig. 2.35** The relation between relative dielectric constant of an insulator with its barrier height (Reproduced with permission, IBM Research, [88])



**Table 2.3** Comparative analysis of band offsets and dielectric constants ( $K$ ) of different dielectric materials

Insulator	Bandgap (eV)	Relative dielectric constant	Conduction band offset (eV)
SiO <sub>2</sub>	9	3.9	3.15
Si <sub>3</sub> N <sub>4</sub>	5.3	7.9	2.4
Al <sub>2</sub> O <sub>3</sub>	8.8	9.5–12	2.8
ZrSiO <sub>4</sub>	~6	10–12	1.5
ZrSiO <sub>4</sub>	4.5		0.7 (interfacial layer)
HfSiO <sub>4</sub>	~6	~10	1.5
ZrO <sub>2</sub>	5.7–5.8	12–16	1.4–1.5
HfO <sub>2</sub>	4.5–6	16–30	1.5
La <sub>2</sub> O <sub>3</sub>	~6	20.8	1.5
Ta <sub>2</sub> O <sub>5</sub>	4.4	25	2.3
TiO <sub>2</sub>	3.05	80–170	~0

Reprinted with permission IBM Research and Dev. [88]

Table 2.3 shows the comparative analysis of band offsets and dielectric constants of different promising high- $K$  materials [110–112]. From the table we can see that the conduction band offset decreases with increasing dielectric constant ( $K$ ). The  $K$ , however, is related to the phase of the material and the first principles density functional approach confirms that the cubic phase has the highest  $K$  value [113]. However, the electronic density of states and the band gap do not have a profound effect on the electronic dielectric constant [114]. Thus it seems that novel structural modifications of a dielectric material might possibly provide a route to enhance the  $K$  value [115]. Above all, high- $K$  gate dielectric materials should preserve high device channel mobility, low interfacial charge scattering centers, and should not degrade the interfacial roughness [116]. Furthermore, the conduction mechanism inside the dielectric should be electronic and not ionic because of the reliability issue.

### 2.3.3 Search for a Suitable High-K Dielectric Material

#### 2.3.3.1 Nitrides and Oxynitrides

It is true that a single molecular layer of SiO<sub>2</sub>, which contributes about 0.3 nm to the overall EOT, will not be able to meet all the requirements of a 65 nm device. Therefore, an alternative high- $K$  dielectric material suitable for the sub-100 nm Cu-damascene process has to be identified.

It seems that oxynitrides and combinations of oxide and nitride of metals and semiconductors [117–118] including nano-crystalline alloys will serve as potential candidates as gate dielectric materials for advanced Si devices [119–120]. These materials have moderate to high  $K$  and can be optimized to a thickness of 1 nm to reduce the leakage current by about two orders of magnitude [121–122], which is not possible to achieve with SiO<sub>2</sub>. However, it is very difficult to fabricate a

reproducible gate material at the nanometer scale, which will be able to withstand the passage of a current density on the order of  $10^5 \text{ A/cm}^2$  (which means about  $10^{11} \text{ C/cm}^2$  of charge over a ten-year life time) [111].

Amorphous silicon nitride ( $\text{Si}_3\text{N}_4$ ) [123–124] is another potential candidate for a gate material. It can be deposited by any one of the following processes, such as: rf sputtering using an *a-Si* target with nitrogen discharge or by the reaction of  $\text{SiH}_4$  and  $\text{NH}_3$  in the presence of nitrogen ( $\text{N}_2$ ) or with plasma enhanced cold wall systems.  $\text{Si}_3\text{N}_4$  has a high dielectric constant (6–9 versus  $\sim 4.2$  for CVD  $\text{SiO}_2$ ), making it less attractive for inter-level insulation.

Oxynitride films of silicon ( $\text{SiO}_x\text{N}_y$  ( $\text{H}_z$ )), which has attracted attention as a gate material, have physical and chemical properties that are intermediate between silicon dioxide and silicon nitride [125]. The material can be deposited in the same way as  $\text{Si}_3\text{N}_4$  with additional introduction of nitric oxide (NO) and ammonia ( $\text{NH}_3$ ) gas. Properties of the material can be tailored for improved thermal stability, low stress, and crack resistance. However, the etch rate of the glassy mixture in buffered HF is about 35 times higher than  $\text{Si}_3\text{N}_4$  films [126–127].

### 2.3.3.2 Tantalum Oxide ( $\text{Ta}_2\text{O}_5$ ) and Titanium Oxide ( $\text{TiO}_2$ )

In recent years many investigators have renewed their interest in  $\text{Ta}_2\text{O}_5$  and  $\text{TiO}_2$  because these materials have high dielectric constant ( $K$ ). Unfortunately, for a large number of high- $K$  materials, the band gap is inversely proportional to  $K$ . To reduce leakage current tunneling, while maintaining the same gate capacitance, the material should have a large band gap and barrier height between the electrode and the conduction band of the dielectric [128–129].

$\text{Ta}_2\text{O}_5$  is the most thoroughly studied dielectric, used in thin film capacitors and as a gate dielectric [130–135]. Recently, atomic layer deposition (ALD) of  $\text{Ta}_2\text{O}_5$  using  $\text{TaI}_5$  and  $\text{O}_2$  precursors is gaining importance as high- $K$  material in dynamic memory circuits [136]. However, the oxides of Ta and Ti are thermally unstable when it is deposited over silicon, and an additional passivation layer raised concern about the scalability of EOT and process complexity [137].

### 2.3.3.3 Hafnium Oxide ( $\text{HfO}_2$ )

CVD and ALD deposited oxides ( $\text{HfO}_2$ ), silicates ( $\text{HfSiO}_x$  and  $\text{HfSiON}$ ) and aluminates of hafnium (Hf) show higher  $K$  and lower leakage current than  $\text{SiO}_2$  at the same EOT. The materials also offer a higher limiting offset barrier (0.5 eV) [138–139] besides being stable thermodynamically and electrically over silicon (Si) at high temperatures [140–144]. At the same time silicon dioxide and oxynitride, the traditional gate dielectric materials in field effect transistors (FETs), are rapidly approaching their ultimate thickness. Thus, the compounds of hafnium are under investigation.

Besides  $\text{HfCl}_4$  and  $\text{H}_2\text{O}$ , Hf amides and Hf alkoxides are used as precursors to deposit  $\text{HfO}_2$  during ALD [145]. On the other hand, in reactive dc magnetron sputtering [150], and CVD (MOCVD), Hf ( $\text{NO}_3$ )<sub>4</sub> is used to deposit  $\text{HfO}_2$  films

[146–149]. However, when the temperature exceeds 700 °C, Hf (NO<sub>3</sub>)<sub>4</sub> shows high oxygen diffusion, besides hysteresis, and crystallization. Moreover, the channel mobility of Hf (NO<sub>3</sub>)<sub>4</sub> is inferior to the Si/SiO<sub>2</sub> interface [151].

#### 2.3.3.4 Zirconium Oxide (ZrO<sub>2</sub>)

Zirconium oxide (ZrO<sub>2</sub>) has attracted much attention as a high-*K* material because of its high temperature stability and high mechanical strength [152]. Thin films of ZrO<sub>2</sub> can be prepared by many methods like sol-gel, spin coating, ALD, reactive sputtering, MOCVD, E-beam evaporation, pulse laser ablation, and rapid thermal CVD [153–155].

Unfortunately, oxides of hafnium (HfO<sub>2</sub>) and zirconium (ZrO<sub>2</sub>) tend to crystallize much more rapidly than SiO<sub>2</sub>, which makes the interface surface rough. So the key issue will be to form amorphous oxides of the metal initially, which might transform into the crystalline state during thermal cycling. One current avenue of investigation is to incorporate silicon (Si), Al, or N<sub>2</sub> into the random network structure [115]. Indeed, adopting the above theory, zircon (ZrSiO<sub>4</sub>), a compound of ZrO<sub>2</sub> and SiO<sub>2</sub>, has shown better interface behavior with silicon (due to its dangling bonds) and has provided more symmetric band alignment with much higher conduction band offsets compared to ZrO<sub>2</sub> (2.10 eV compared to 0.64–1.2 eV of ZrO<sub>2</sub>).

#### 2.3.3.5 Lanthanum Aluminate (LaAlO<sub>3</sub>)

Aluminate of lanthanum (La) is a promising material for a gate oxide. The localized d state in La oxide, as well as the energy relative to the silicon (Si) conduction band, play important roles in determining the magnitude of the direct tunneling current [156–157]. Molecular beam deposited 10 Å film shows a *K* value ~24 with an optical band gap of 5.6 eV. The band offsets between LaAlO<sub>3</sub> and Si is 2.1 eV for electrons and 1.9 eV for holes [158].

#### 2.3.3.6 Titanate Compounds of Barium (BaTiO<sub>3</sub>), Barium Strontium (BaSrTiO<sub>3</sub>), and Lead (PbTiO<sub>3</sub>)

The *K* values of BaTiO<sub>3</sub>, BaSrTiO<sub>3</sub>, and PbTiO<sub>3</sub> are 1000, 1500 and 200–400, respectively [159]. Ferroelectric materials are ceramics and have nonlinear dielectric properties that show hysteresis under the action of an alternating voltage. Another interesting phenomenon observed with these dielectric materials is regions of spontaneous polarization, which is not caused by any external electric field. As a result, displacement of the titanium and oxygen layers results on a slightly distorted shape of the cell, and a special type of phase transition takes place when the temperature passes through the Curie point [149]. It is expected that these ceramics can be potential candidates for high-*K* materials, provided the conduction band offsets are comparable to alumina (Al<sub>2</sub>O<sub>3</sub>) (Table 2.3).

These titanate compounds can be deposited by direct and flash evaporation and CVD methods (by reacting metal lead (Pb) with ethyl titanate, Ti (C<sub>2</sub>H<sub>5</sub>O)<sub>4</sub>).

Reactive sputtering from a lead titanium cathode in an argon–oxygen atmosphere can also be applied to fabricate thin films of titanium compounds.

The search for high- $K$  materials to replace  $\text{SiO}_2$  is still an ongoing process. There are several primary concerns about these high- $K$  materials such as:

- (a) *Threshold voltage pinning*: Gate stacks fabricated by polysilicon,  $\text{HfO}_2$  and  $\text{ZrO}_2$  show relatively high threshold voltage levels due to defects at the gate electrode/gate electrode interface. This reduces drive current and impairs device performance.
- (b) *Phonon scattering*: Higher  $K$  dielectric materials show polarization effect and higher optical phonon vibration, that affect electron mobility and the performance of the device.

### 2.3.4 Deposition Technology for High- $K$ Materials

Oxides of metals that are potential candidates for gate dielectrics can be deposited by reactive sputtering by introducing the second element (oxygen) in gaseous form. In order to increase the deposition rate, the second element can be introduced along with argon gas. However, other methods, such as atomic layer deposition (ALD) [160–163] and chemical vapor deposition (CVD) [164], can be applied to deposit the high- $K$  materials with proper precursors. Physical vapor deposition (ionized physical vapor deposition (IPVD), a special type of sputtering system, for example) [165] and electron beam (EB) deposition methods [166] can also be used to deposit high- $K$  gate materials. Details of the deposition methods have been presented in a separate chapter.

### 2.3.5 Summary

Scaling of device dimensions has historically made advances in silicon ULSI technology. As a result of this scaling, both the vertical and horizontal dimensions have been reduced to a point where silicon dioxide as a dielectric material cannot satisfy the requirements. The many benefits driving manufacturers to use low- $K$  dielectric materials include increased device speed, reduced power, required heat dissipation, and reduced interline talk. However, the transition to low  $K$  has been delayed primarily because of challenges in their integration, including etching and stripping problems associated with the carbon content materials. At the same time, porous low- $K$  materials are susceptible to absorbing moisture during planarization (CMP). The moisture inside the pores may react with fluorinated dielectric materials and can produce hydrofluoric acid, which is very corrosive. The moisture may also cause ionization of copper and may drive the ionized  $\text{Cu}^{+}/^{++}$  to silicon. Thus to reduce  $RC$  effects and to increase the speed of sub-100 nm devices the price is very high.

Low- $K$  materials in general exhibit weak polarization when subjected to an external electric field. There are several guidelines in formulating these materials; the

most obvious one is the choice of a non-polar dielectric system. In these materials polarity is weak because of symmetrical polar chemical groups that cancel the dipoles of chemical bonds between dissimilar atoms.

In the case of high- $K$  materials, scaling the thickness of the gate dielectric has long been recognized as one of the keys to scaling devices. It is expected that for sub100 nm devices (CMOS) the gate oxide will be less than 2 nm. Thus it appears that  $\text{SiO}_2$  will be unsuitable as a gate insulator in the sub-100 nm device. The vertical scaling requirements for gate stacks and for shallow extension junctions require 1 nm equivalent oxide thickness (EOT) to deal with leakage current tunneling. Some metal oxides, like  $\text{HfO}_2$ ,  $\text{ZrO}_2$  and their silicates, have been identified as promising materials that are supposed to work with 1 nm EOT. However, integration of high- $K$  materials will be a challenging task because of the chemical bonding (ionic) and are likely to exhibit both ionic conduction and high charge levels.

The limited chemical and thermal stability are the two most important criteria associated with alternative high- $K$  dielectrics and alternative gate electrode materials. In spite of the advantages of the polysilicon gate, the present process flow to integrate the future advanced gate stack employing these high- $K$  materials is still questionable. Thus new integration schemes and device structures may be required to form source/drain junctions of MOS and all high temperature processes are to be done before the formation of the gate stack. At the same time, the chemical mechanical polishing (CMP) process used to planarize the surface has several advantages and challenges. The challenges include identifications of suitable materials for sacrificial gate stack and spacers and development of the consumables. Although several high- $K$  materials and processes have been investigated, it still appears that the major concern is the cost.

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