

Preface

The frontiers of knowledge are advancing at an ever-increasing rate. Today's discoveries will tomorrow be part of the toolbox of every researcher. By analogy, the process of advancing the line of settlements, and cultivating and civilizing new territory, takes place in stages, and the semiconductor industry, which has brought a revolution in modern civilization, is a vivid example. The intellectual foment that marked its beginnings has changed the way we view the physical world forever. Since the creation of the integrated circuit in 1960 there has been a continuous reduction in the size of circuits and thus the feature size of devices.

Following Moore's famous prediction, the number of devices manufactured on a single chip has exceeded the expectation of very large-scale integrated (VLSI) circuits. As a result, new materials are being introduced to meet the challenge of 21st century IC technology. The increasing device count accompanied by a shrinking minimum feature size, which was expected to be smaller than $1\text{ }\mu\text{m}$ before 1990, has reached $0.1\text{ }\mu\text{m}$ at the beginning of the 21st century. Progress in the development of new materials is marching in tandem and with much the same speed as circuit density (number of devices per unit square area).

The entire field of VLSI circuits depends upon circuit design, layout of electronic circuitry, process development, and synthesis of new materials. As a result, traditional materials (e.g. copper) are sometimes renewed in a fashion necessary to accommodate them to modern technology. Mankind has known about copper and its processing for different uses since the prehistoric age. Now, at the beginning of the 21st century, the use of copper has opened a new era in the IC manufacturing industry.

The 1990s were the decade in which copper as an interconnecting material came to the forefront and gained much attention from microelectronics engineers and scientists. The metallic conductivity and resistance to electromigration of bulk copper (Cu) are better than aluminum (Al). But as the feature size of the Cu-lines forming interconnects is scaled, the resistivity of the lines is seen to increase. At the same time, the electromigration and stress induced voids due to increased current density become reliability issues. Innovative ideas like the use of a cobalt-tungsten cap layer and alloying of copper have worked well, but both come with an increased RC product line.

The use of Cu-interconnect has introduced the additional burden of integration of the barrier layer in Cu-damascene architecture. The barrier layer affects the resistance of the Cu-lines too. The PVD-Cu/PVD-Ta interface is “magical” and the use of precursors in the ALD/CVD (Atomic Layer Deposition/Chemical Vapor Deposition) system has raised several questions, although the advantages of ALD in comparison to the PVD system in producing perfect step coverage with very thin layers is clear.

In the field of low- K , time-dependent dielectric breakdown (TDDB) and inter-layer dielectrics (ILDs), reliability is becoming more important. As the dimensions shrink, the stress gradients increase because the same amount of stress is confined within a reduced geometry. Moreover, these low- K materials are softer than SiO_2 and susceptible to failure.

There are many challenges and difficulties with copper interconnect but not without any gain. Most of the challenges are overcome partially by using advanced instrumentation and photolithography materials. Photolithography has come a long way from 365 nm exposure technology to 157 nm exposure technology. Use of advanced laser systems with lower radiation wavelengths, additional hardware, and enhancement techniques, have all contributed to these improvements.

In 1997 IBM and Motorola introduced new approaches to Cu-interconnecting technology and in September 1997 IBM demonstrated their complementary metal oxide semiconductor (CMOS) device with six layers of copper lines. At the end of the decade, copper damascene processes were introduced and the century-old chemical mechanical polishing (CMP) procedure was renewed to integrate copper in deep sub-micron level circuitry.

This book was developed from a series of lecture notes prepared for graduate students of different universities. The notes are based on the research and publications of countless scientists and engineers engaged in this field. I express my sincerest thanks and gratitude for their indirect help.

Copper Interconnect Technology is the first book on the subject to treat materials, technology, and applications comprehensively, and is a product of my 25 years of research and teaching experience in different universities and research organizations. It is written for professionals as well as graduate students, and belongs on the bookshelf of workers in several microelectronics disciplines.

The chapters of the book are arranged sequentially following the sequence of the damascene process. In Chapter 1 basic properties of the materials used in copper interconnect are presented. Chapter 2 deals with the low- and high- K dielectric materials (dealing with the physical, chemical, and structural properties) that are of potential interest for scaled-down, high-speed devices. The diffusion of Cu in silicon is well known, so Chapter 3 is devoted to the search for new barrier materials and metal complexes to minimize diffusion of Cu from Cu interconnects. Some of the promising barrier materials, their physical and chemical properties, and the interpretation of binary and ternary phase diagrams, are also discussed.

Chapter 4 addresses different resist materials (DUV and EUV) and lithography techniques that are being used or are in the development stage. Pattern generation

technologies together with different etching systems applied in the modern IC industry are also considered.

As the state of the art of modern integrated circuit technology has changed from the subtractive aluminum metallization process to via and trench filling additive Cu, the deposition technology has also evolved. Chapter 5 covers different deposition technologies that are frequently used in the modern Cu-damascene process. Chapter 6 deals with the damascene procedure and the chemical mechanical planarization (CMP) process.

Cu-interconnect replaced Al-interconnect because of its higher bulk-conductivity and electromigration resistance. But as the feature size of the conducting lines is shrinking, the thin metal lines can no longer retain the bulk properties of the metal. In Chapter 7 the conductivity and electromigration properties of Cu-interconnecting lines are discussed. Chapter 8 deals with the routing design of the Cu-interconnects together with the reliability issues of the scaled Cu-lines forming interconnects.

Watertown, Massachusetts

Tapan K. Gupta



<http://www.springer.com/978-1-4419-0075-3>

Copper Interconnect Technology

Gupta, T.

2009, XIX, 423 p., Hardcover

ISBN: 978-1-4419-0075-3