

Contents

1	Introduction	1
1.1	Trends and Challenges	2
1.2	Physical Limits and Search for New Materials	5
1.3	Challenges	6
1.4	Choice of Materials	7
1.4.1	Why Copper (Cu) Interconnects?	7
1.5	New Technologies	15
1.5.1	Multilayer Metal Architecture	15
1.5.2	Substrate Engineering	16
1.6	An Alternate Technology for Interconnects	19
1.7	Materials Used in Modern Integrated Circuits	21
1.7.1	Properties of Copper	23
1.7.2	Grain Size	24
1.7.3	Melting Temperature	25
1.8	Barrier Layer	27
1.9	Low-K Dielectric Materials	28
1.10	Polymers	30
1.11	Semiconductors	33
1.11.1	Silicon (Si)	33
1.12	Challenges and Accomplishments	35
1.12.1	Challenges	35
1.12.2	Accomplishments	35
1.13	Technologies of the 21st Century, and the Plan to Meet the Challenges	38
1.14	Ultra-Shallow Junction (USJ)	40
1.15	Circuit Design and Architecture Improvements	41
1.16	Performance and Leakage in Low Standby Power (LSTP) Systems	42
1.17	Introduction of New Materials and Integration Processes	43
1.17.1	Nano-Materials	44
1.17.2	Superconductors	45
1.17.3	Integration Processes	47
1.18	Summary	53
	References	55

2	Dielectric Materials	67
2.1	Introduction	67
2.2	Interlayer Dielectric (ILD)	71
2.2.1	Introduction	71
2.2.2	Mathematical Model	74
2.2.3	Selection Criteria for an Ideal Low-K Material	76
2.2.4	Search for an Ideal Low-K Material	78
2.2.5	Achievement	83
2.2.6	Impact of Low-K ILD Materials on the Cu-Damascene Process	92
2.2.7	Deposition Techniques	95
2.3	High-K Dielectric Materials	97
2.3.1	Introduction	97
2.3.2	Impact on Scaling and Requirements	98
2.3.3	Search for a Suitable High-K Dielectric Material	99
2.3.4	Deposition Technology for High-K Materials	102
2.3.5	Summary	102
	References	103
3	Diffusion and Barrier Layers	111
3.1	Diffusion	111
3.1.1	Introduction	111
3.1.2	Transitional Effects	113
3.1.3	Mathematical Modeling of Diffusion in Cu-Interconnects	114
3.1.4	Grain Boundary (GB) Diffusion	118
3.1.5	Vacancy Diffusion	120
3.1.6	Drift Diffusion	121
3.1.7	Interdiffusion	122
3.1.8	Diffusion of Copper and Its Consequences	122
3.1.9	Precipitation	124
3.2	Barrier Layer for Cu-Interconnects	125
3.2.1	Theory	125
3.2.2	Ideal Barrier Layer	126
3.2.3	Barrier Layer Architecture	126
3.2.4	Interlayer Reactions	128
3.2.5	Influence of the Barrier Layer Properties on the Reliability of Cu-Interconnects	132
3.2.6	Low-K Dielectric-Barrier Layer	135
3.2.7	Reaction Rates	135
3.2.8	Influence of the Barrier Layer on the Electrical Conductivity of Cu-Lines	139
3.2.9	Influence of Barrier Layer Thermal Conductivity on Cu-Line	141
3.2.10	Classification of Barrier Layer	144

3.2.11	Properties of Different Barrier Layer Materials	145
3.2.12	Cap-Layer, Its Properties and Functions	148
3.3	Summary	150
	References	151
4	Pattern Generation	161
4.1	Photolithography	161
4.1.1	Introduction	161
4.1.2	Resolution Limits of Optical Lithography	164
4.1.3	Deep Ultraviolet (DUV) Lithography	168
4.1.4	Reticles	173
4.1.5	Enhancement Techniques for Resolution	175
4.1.6	157 nm Lithography	179
4.1.7	Chemically Amplified Resist (CA)	183
4.1.8	Extreme Ultraviolet (EUV) Lithography	185
4.1.9	e-Beam Lithography (EBL)	189
4.1.10	Electron-Beam Resist	192
4.1.11	e-Beam Reticle	195
4.1.12	Step and Flash Imprint Lithography (SFIL)	195
4.2	Etching and Cleaning of Damascene Structures	197
4.2.1	Etching	197
4.2.2	Cleaning	210
4.3	Summary	214
	References	216
5	Deposition Technologies of Materials for Cu-Interconnects	223
5.1	Introduction	223
5.2	Emerging Technologies	224
5.2.1	Cu-Damascene Process	224
5.2.2	Barrier Layer Requirements	225
5.3	Deposition Requirements	225
5.4	Thin Film Growth and Theory of Nucleation	226
5.4.1	Nucleation Theory	227
5.5	Instrumentation	230
5.5.1	Physical Vapor Deposition	230
5.5.2	Sputtering	231
5.5.3	Ionized Physical Vapor Deposition (IPVD)	234
5.6	Chemical Vapor Deposition (CVD)	236
5.6.1	Plasma Enhanced CVD (PECVD) System	236
5.6.2	Metal-Organic Vapor Deposition (MOCVD)	238
5.7	Low Temperature Thermal CVD (LTTCVD) System	240
5.8	Atomic Layer Deposition (ALD)	241
5.9	Plating	243
5.9.1	History of Electroplating and Printed Circuit Boards (PCBs)	243

5.9.2	DC Bath Chemistry	244
5.9.3	Electroplating of Copper Inside Damascene Architecture ...	245
5.10	Process Chemistry for Superconformal Electrodeposition of Copper	247
5.11	Electrochemical Mechanical Deposition (ECMD)	248
5.12	Influence of the Seed Layer on Electroplating	249
5.13	Electroless Deposition of Copper	250
5.14	Stress in Cu-Interconnects	251
5.15	Summary	253
	References	254
6	The Copper Damascene Process and Chemical Mechanical Polishing ..	267
6.1	The Copper Damascene Process	267
6.1.1	Introduction	267
6.1.2	Conventional Metallization Technology	270
6.1.3	Cu-Damascene Metallization Technology	271
6.1.4	General Objectives and Challenges	276
6.2	Chemical Mechanical Polishing (CMP) and Planarization	278
6.2.1	Introduction	278
6.2.2	Chemical Mechanical Polishing (CMP) Technology	279
6.2.3	Copper Dishing Model	285
6.2.4	Slurry Chemistry	286
6.2.5	Particle Size Inside the Slurry	287
6.2.6	Relative Velocity of the Pad and Wafer	289
6.2.7	Pad Pressure	289
6.2.8	Pad-Elasticity	289
6.2.9	Pad Conditioning	289
6.2.10	Shallow Trench Isolation (STI)	290
6.2.11	Abrasive Free Polishing	291
6.2.12	End-Point Detection	291
6.2.13	Dry In Dry Out	292
6.2.14	Multi-Step Processing	293
6.2.15	Post-CMP Cleaning	293
6.2.16	CMP Pattern Density Issues	295
6.3	Summary	296
	References	296
7	Conduction and Electromigration	301
7.1	Conduction	301
7.1.1	Introduction	301
7.1.2	Conduction Mechanism and Restrictions	303
7.1.3	Effect of Grain Boundary (GB) Resistance on the Conductivity of Cu-Interconnects	311
7.1.4	Effect of Grain Size and Morphology of the Substrate	311

7.1.5	Morphology of the Cu-Film and Its Influence on the Conduction (Electrical) Mechanism of Cu-Interconnects . . .	312
7.1.6	Effect of Film Thickness on the Conductivity of Cu-Interconnects	317
7.1.7	Diffusion Related Impacts on the Conductivity of a Cu-Line	318
7.1.8	Cu-Line Stress and Its Consequences	319
7.1.9	Conduction of Heat Through Cu-Interconnects	321
7.1.10	Thermal Cycling (Annealing) Related Phenomena	322
7.2	Electromigration (EM)	324
7.2.1	Electromigration (EM)	324
7.2.2	Mechanism of Electromigration (EM) and Its Effects	325
7.2.3	Void Formation	329
7.2.4	Analytical Model on Stress Related EM	330
7.2.5	Effect of Microstructure of the Film on Mass Migration	333
7.2.6	Effect of Solute on Electromigration	335
7.2.7	Melting Temperature of a Metal and Its Effect on Grain Growth	335
7.2.8	Effect of Temperature on EM	336
7.2.9	Current Density and Its Effect on EM	336
7.3	Summary	336
	References	337
8	Routing and Reliability	347
8.1	Routing	347
8.1.1	Introduction	347
8.1.2	Methods of Improving Interconnect Routings	349
8.1.3	Interconnect Routing Design	351
8.1.4	Challenges with High Density Routing	359
8.1.5	Cascaded Driver	361
8.1.6	Transmission Line Coupling	361
8.1.7	Clocking of High-Speed System	361
8.2	Reliability	362
8.2.1	Introduction	362
8.2.2	Reliability Issues Related to Cu-Interconnects	365
8.2.3	Measurements	388
8.3	Summary	393
	References	394
	Glossary (Copper Interconnects)	405
	Index	415



<http://www.springer.com/978-1-4419-0075-3>

Copper Interconnect Technology

Gupta, T.

2009, XIX, 423 p., Hardcover

ISBN: 978-1-4419-0075-3