errata for
Introduction to Embedded System Design Using Field Programmable Gate Arrays

Page 25
The Verilog code for Fig. 2.8a should read:

```
module shiftregb (input x, clock, rst, output reg z);

reg a,b,c;

always @ ( posedge clock)
        if (rst)
            begin
                    a = 0;
                    b = 0;
                    c = 0;
                    z = 0;
            end
        else
            begin
                    a = x;
                    b = a;
                    c = b;
                    z = c;
        end

endmodule
```

a

Page 50
The legend for Fig. 2.39 should read:

Fig. 2.39. Simulink®-based HDL simulation environment using Xilinx System Generator™

Page 128
The legend for Fig. 6.16 should read:

Fig. 6.16. a Power bridge with six switching devices to generate space vector voltages mentioned in table 6.4; **b** switching sequence to minimize switching losses for dwell times Ta, Tb and T0

Page 133
The legend for Fig. 6.21 should read:

Fig. 6.21. FPGA-based PMSM motor drive controller

Page 148 (Paragraph 1)
The last sentence of position determination section should read:

A code similar to that given in Fig. 2.16 is used to count the number of pulses coming from an incremental type position encoder.

http://www.springer.com/978-1-84882-015-9

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2009, XVII, 154 p., Hardcover
ISBN: 978-1-84882-015-9