Preface

The revolutionary impact of the discovery of transistor action by John Bardeen and Walter Brattain of Bell Labs in December 1947 was not anticipated. Similarly, the importance of William Shockley's invention at Bell Labs in January 1948 of the junction transistor (which was not experimentally demonstrated until 1950, although proof-of-concept using a non-colinear configuration was shown in 1949) was not recognized immediately. The transistor's potential was only recognized after it became evident during the 1950s that the transistor – with its much lower power dissipation – could be used to do significantly more than simply mimic vacuum tube electronics in solid-state. It was the invention of the Integrated Circuit (IC) by Jack Kilby of Texas Instruments in 1958 (germanium in the mesa configuration) and, independently, by Bob Noyce of Fairchild in 1959 (silicon in the planar configuration, built upon Jean Hoerni's research at Fairchild in late 1957), that initiated the microelectronics revolution. Even then, however, the implications were barely perceived.

The bipolar IC entered into high-volume production in the mid-to-late 1960s, followed by the MOSFET IC in the early 1970s. Patrick Haggerty's vision at Texas Instruments in the early 1960s of the pervasiveness of the silicon microelectronics revolution, based on the concept of the "learning curve" (i.e., the concomitant reduction in the cost of fabrication with the increased volume of production) and market elasticity, was one of immeasurable significance to the fledging IC industry. Concurrently, Gordon Moore at Fairchild Semiconductor in 1965 made a remarkably prescient assessment of memory component growth, based initially on bipolar and then on MOS memory density trends: A semi-log graph of the number of memory bits in an IC versus the date of initial production was a straight line, representing almost a doubling each year. Moore's observation (updated at Intel in 1975 to about 18 months per doubling and subsequently re-affirmed in 1995) showed that a viable market was indeed practical, and gave impetus to the industry. His analysis became enshrined as Moore's law and set the cadence for technology advancement, e.g., as laid out in the *International Technology Roadmap for Semiconductors* (ITRS). These

business-oriented considerations, moreover, combined with Bob Dennard's invention of the one-transistor/one-capacitor dynamic random access memory cell (DRAM) at IBM in 1968 and the related transistor scaling methodologies introduced by Dennard and colleagues at IBM in 1972, established the paradigm for the progression of IC fabrication technology (from a minimum feature size of about 10 μm in the early 1970s, to sub-35 nm in the present era) that has facilitated the explosive growth and application of the MOSFET IC (and subsequently the CMOS IC) during the past 35 years.

The myriad of new electronic products and the creation of new market segments was not (and perhaps could not be) foreseen by the researchers involved. Indeed, Robert Lucky noted in *Engineering Tomorrow* (edited by J. Fouke, T.E. Bell, and D. Dooling, IEEE Press, 2000) that "there is no *a priori* way to determine what will tip a market. It's a fundamental instance of chaos in group dynamics. And that makes it fundamentally difficult to predict future societal behaviors in the adoption of technologies." More than luck is involved; nevertheless, the next application is often a surprise.

And here we are, on the brink of the 50th anniversary of the invention of the IC, in the nano-technology era, wherein critical dimensions on an IC chip, such as the physical channel length, is less than 35 nm. Will silicon continue to be the pre-eminent active semiconductor material, and will Moore's law continue unabated, albeit in a broader economic venue? Indeed, are we wiser now in comprehending that fundamental research, per se, inevitably will lead to new material and device configurations as well as new market opportunities, barely (if at all) perceived at the present time? The research agenda is yet our best opportunity to spawn new innovations to sustain industry expansion to the next major set(s) of global applications.

In that regard, this monograph addresses these questions by reflecting upon the scientific and technological breakthroughs that enabled the microelectronics era, providing a firm foundation for ensuing research, and offering a glimpse of what is to come in the nano-technology era. Accordingly, a review and assessment of topics fundamental to silicon materials and MOSFET device structures is presented, to identify potential nano-technology research directions and possible nano-technology applications.

The monograph is divided into three sections, similar to the format of the Spring 2005 issue of *INTERFACE* (published by *The Electrochemical Society*) from which this book has its genesis. The first section reviews aspects of the historical foundations of our industry. The second section proceeds to examine the silicon material and device structures that are the foundation for state-of-the art IC technology. The third section then presents perspectives of future directions for the nano-technology era. Interestingly, the authors do not anticipate that the current silicon materials/IC industry infrastructure will simply dissolve. The global captains of industry, in-point-of-fact, would not allow this. Rather, the initial new applications in the nano-technology era may indeed come about via integration and merging of new materials with (leading edge) IC structures, forging new applications that may be presently envisioned, even as the IC industry drives towards the sub 10 nm physical MOSFET channel

length. It is the anticipation of what comes next, however, that will require our most creative perceptions and, most probably, will produce the greatest surprise(s).

Historical Background

Silicon, and more recently, related group-IV material systems such as silicon-germanium, have been utilized (with silicon) for IC fabrication over the past ∼45 years or so. While silicon and group-IV material systems are anticipated to continue to be utilized in future IC products, the group III–V materials may also concurrently be adopted in order to achieve continued improvement in the device active channel characteristics and related IC performance. Robert Cahn presents an historical perspective of silicon and the silicon revolution in an enchanting introduction titled *Silicon: Child and Progenitor of Revolution*. The phenomenal growth of the IC industry is discussed in a decidedly upbeat fashion by Dan Hutcheson in *The Economic Implications of Moore's Law*. Perhaps Gordon Moore described it best when he recently noted that "... you are once again reminded that this is no longer just an industry, but an economic and cultural phenomenon, a crucial force at the heart of the modern world." Moore further noted that "no exponential is forever; but 'forever' can be delayed." Indeed, we will depend on a new generation of research personnel to maintain and, perhaps, extend Moore's law into the nano-technology world and the next group of big applications.

State-of-the-Art

The characterization, annihilation, and selective utilization of defects to achieve superior IC performance, yield, and reliability is a cornerstone of the IC industry. Because many of the phenomena discussed are structure-sensitive, the "process-structure-property" approach is used to describe the characteristics of modern electronic/opto-electronic ICs which utilize III-V compounds in conjunction with silicon (and germanium again). Specifically, the fabrication process determines the material structure, which in turn determines the subsequent material properties and, therefore, the IC characteristics. Jim Chelikowsky notes that "computers built with silicon can be used to solve for the electronic properties of silicon itself." Chelikowsky reviews these computational approaches from first principles in *Using Silicon to Understand Silicon*. Stefan Estreicher continues this first-principles study of point defects in silicon in *Theory of Defects in Si: Past, Present and Challenges*. These theoretical considerations, in combination with microscopic experiments, have led to an understanding of silicon that is incomparable to that of any other material studied in the technological era. The selective utilization of defects, as grown in the silicon crystal as well as process-induced during device/IC fabrication, and their mutual interactions, has achieved superior IC performance. Andrei Istratov, Tonio Buonassisi, and Eicke Weber pursue several aspects of these phenomena and, in particular, indicate the viability of such an approach for the rapidly expanding defect-engineered silicon photovoltaics initiative (with quantities of silicon usage fast approaching that of the IC industry) in *Structural, Elemental, and Chemical Complex*

Defects in Silicon and Their Impact on Silicon Devices. Materials science and engineering will continue to be critical but it appears that the art and science wherein properties of materials may be dictated not as much by what atoms the materials consist of (taking some liberty here) but rather how they are arranged together will be the *sine qua non* of opto-electronic devices and circuits in the nano-era.

The theme of defects and their control may be further extended by realizing that the surface itself may be considered a giant defect, as noted by H.C. Gatos of M.I.T. and others in the 1960s. The characterization and control of the silicon surface is a fundamental requirement for stable device and IC characteristics. Martin Frank and Yves Chabal present our current understanding of surfaces and interfaces as well as their unique position in silicon micro-electronics, in *Surface and Interface Chemistry for Gate Stacks on Silicon*.

This section concludes with two device-focused articles. Patricia Mooney presents a summary of current trends in silicon-based nano-electronics – in particular the enhancement of carrier mobilities – in *Enhanced Carrier Mobility for Improved CMOS Performance*. The use of variously configured, sequential compositions and combinations of strained silicon-germanium (utilizing carbon as appropriate) to produce strain at the silicon channel surface for various MOSFET configurations permits electron and hole mobilities higher than predicted by the universal mobility curves. Further materials opportunities are noted, wherein an NMOS [PMOS] transistor exhibits optimal electron [hole] mobility for the (100) [(110)] silicon wafer orientation (in the ⟨110⟩ direction for both surfaces). Methods of fabricating substrates to enhance both NMOS and PMOS performance are described as a hybrid orientation technology (HOT), and a simplified hybrid orientation technology (SHOT). Finally, Tsu-Jae King Liu and Leland Chang discuss a host of silicon-based advanced transistor structures and associated materials, based on the conventional "top-down" IC fabrication methodology in *Transistor Scaling to the Limit*. They note that these efforts are expected to extend the ITRS to a physical channel length in the single-digits, consistent with IC leakage current, power-supply voltage, and power-delay product specifications.

Future Directions

The final section of this monograph covers several evolving opportunities for future nano-technology. Ted Kamins discusses the alternative "bottom-up" approach for device fabrication in the nano-world in *Beyond CMOS Electronics: Self-Assembled Nanostructures*. Here we see the concept of "self-assembly," introduced by way of an example in the fabrication of in-plane nanowires (5 nm in diameter by several hundred nm in length) for connections between active circuit components to enhance IC performance. Indeed, we are still basically using silicon and its myriad fabrication process technologies in conjunction with the self-assembly concept.

Mircea R. Stan, Garrett S. Rose, and Matthew M. Ziegler then discuss *Hybrid CMOS / Molecular Integrated Circuits*. The authors look to further the pervasiveness of silicon technology by "piggy-backing" the nano-technology world onto the ever-shrinking IC devices on a chip. In these initial nano-technology applications,

the authors suggest that the (nano) molecular assembled structure will be electrically connected to the upper surface of a programmable logic array (PLA), based on majority-carrier logic, with appropriate wiring schemas. It is anticipated that a nano-technology single-electron transistor can be operated in conjunction with a CMOS logic IC at room temperature (an extremely important requirement), thereby enhancing the performance of advanced logic CMOS devices beyond what they could achieve on their own.

Delving further into the nano-world, Andre DeHon notes that at the current stage of the micro/nano-electronics revolution, we no longer have the orders of magnitude difference between the size of the IC and the constituent atoms, which previously allowed the crafting of large collections of atoms into "perfect" devices. Accordingly, Andre notes that circuit designers and architects now need to take some of the responsibility for dealing with truly atomic-scale imperfections and uncertainty in *Sublithographic Architecture: Shifting the Responsibility for Perfection*. Finally, David P. DiVincenzo discusses *Quantum Computing*. Besides the potential realization of fabricating qubits (quantum bits) in Josephson junction circuits and ion traps, the author discusses the role of semiconductor quantum dots. He notes that III–V heterostructures might indeed facilitate the fabrication of a quantum computer. Interestingly, the scientific literature is also discussing the utilization of an isolated silicon double quantum dot as a qubit. The author notes at the end of his article: "It may be hoped that in ten years the details of this chapter will be thoroughly obsolete, and completely new and unanticipated effects will have been seen and controlled in such a way that it makes the path to a quantum computer clear. We will see." Indeed, we shall see more clearly as we enter the nano-technology era to identify the next big technologies that can be wrought from the nano-world for the betterment of humankind.

Finally, we are fortunate to have four additional brief contributions to the monograph rounding out this perspective of *Into The Nano Era: Moore's Law Beyond Planar Silicon CMOS*. Fred Seitz leads off with a brief introductory comment, *Silicon and Electronics*, about the evolution of electronics over the past 75 years. This is followed by Nick Holonyak's reflections on *Silicon and The III–V's: Semiconductor Electronics (Electron, Hole, and Photon) Forever*. We conclude with two afterwords by the Nobel Prize awardees Herb Kroemer and Horst Stormer. Herb Kroemer's contribution is titled *Nano-Whatever: Do We Really Know Where We Are Heading?*, reprinted from Phys. Stat. Sol. (a) **202**, No. 6, 957–964 (2005). Horst Stormer's afterword is titled *Silicon Forever! Really?*, from the 2006 issue of Solid-State Electronics, **50**, No. 4, 516–519 (2006). Clearly, we will all have benefited by these colleagues sharing their perspectives with us as we enter the nano-technology era.

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Henderson, NV, April 2008 *Howard R. Huff*

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