
Contents

Foreword: Silicon and Electronics vii

**Foreword: Silicon and the III–V’s: Semiconductor Electronics
(Electron, Hole, and Photon) Forever** ix

Preface xiii

List of Contributorsxxvii

Part I Historical Background

1 Silicon: Child and Progenitor of Revolution

R.W. Cahn[†] 3

 References 9

2 The Economic Implications of Moore’s Law

G.D. Hutcheson 11

 2.1 Introduction 11

 2.2 Moore’s Law: A Description 12

 2.3 The History of Moore’s Law 12

 2.4 The Microeconomics of Moore’s Law 23

 2.5 The Macroeconomics of Moore’s Law 30

 2.6 Moore’s Law Meets Moore’s Wall: What Is Likely to Happen 32

 2.7 Conclusion 35

 Appendix A 36

 References 38

[†] Deceased.

Part II State-of-the-Art

3 Using Silicon to Understand Silicon

<i>J.R. Chelikowsky</i>	41
3.1 Introduction	41
3.2 The Electronic Structure Problem	42
3.2.1 The Empirical Pseudopotential Method	42
3.2.2 Ab Initio Pseudopotentials and the Electronic Structure Problem	47
3.3 New Algorithms for the Nanoscale: Silicon Leads the Way	50
3.4 Optical Properties of Silicon Quantum Dots	52
3.5 Doping Silicon Nanocrystals	55
3.6 The Future	58
References	58

4 Theory of Defects in Si: Past, Present, and Challenges

<i>S.K. Estreicher</i>	61
4.1 Introduction	61
4.2 From Empirical to First-Principles	63
4.3 First-Principles Theory	66
4.4 First-Principles Theory at Non-zero Temperatures	70
4.5 Discussion	73
References	74

5 Structural, Elemental, and Chemical Complex Defects in Silicon and Their Impact on Silicon Devices

<i>A.A. Istratov, T. Buonassisi, E.R. Weber</i>	79
5.1 Introduction	79
5.2 Defect Interactions in Single-Crystalline Silicon	80
5.3 Precipitation Behavior, Chemical State, and Interaction of Copper with Extended Defects in Single-Crystalline and Multicrystalline Silicon	84
5.4 Precipitation Behavior, Chemical State, and Interaction of Iron with Extended Defects in Silicon	91
5.5 Pathways for Metal Contamination in Solar Cells	96
5.6 Effect of Thermal Treatments on Metal Distributions and on Device Performance	99
5.7 Discussion: Chemical States of Metals in mc-Si	101
5.8 Discussion: Interactions between Metals and Structural Defects	104
5.9 Discussion: Engineering of Metal-Related Nanodefects by Altering the Distributions and Chemical States of Metals in mc-Si	106
5.10 Summary and Conclusions	108
References	109

6 Surface and Interface Chemistry for Gate Stacks on Silicon

<i>M.M. Frank, Y.J. Chabal</i>	113
6.1 Introduction: The Silicon/Silicon Oxide Interface at the Heart of Electronics	113
6.2 Current Practices and Understanding of Silicon Cleaning	115
6.2.1 Introduction	115
6.2.2 Silicon Cleans Leading to Oxidized Silicon Surfaces	116
6.2.3 Si Cleans Leading to Hydrogen-Terminated Silicon Surfaces .	124
6.2.4 Microscopic Origin of Silicon Oxidation	136
6.2.5 Initial Oxidation of Hydrogen-Terminated Silicon.....	137
6.3 High-Permittivity (“High- <i>k</i> ”) Gate Stacks	147
6.3.1 Introduction	147
6.3.2 Silicon Surface Preparation and High- <i>k</i> Growth: The Impact of Thin Oxide Films on Nucleation and Performance	148
6.3.3 Post-Treatment of the High- <i>k</i> Layer: Nitridation	156
6.3.4 The pFET Threshold Voltage Issue: Oxygen Vacancies	157
6.3.5 Threshold Voltage Control: Oxygen and Metal Ions	158
6.4 Conclusion	161
References	161

7 Enhanced Carrier Mobility for Improved CMOS Performance

<i>P.M. Mooney</i>	169
7.1 Introduction	169
7.2 Enhanced Carrier Mobility in Si under Biaxial Tensile Strain.....	169
7.2.1 Devices	170
7.2.2 Strain-Relaxed SiGe Buffer Layers	171
7.2.3 SGOI and SSOI Substrates	175
7.2.4 Defect-Free (Elastic) Strain Relaxation	178
7.3 Enhanced Hole Mobility via Biaxial Compressive Strain	181
7.4 Other Methods to Increase Carrier Mobility for Si CMOS Applications	183
7.4.1 Hybrid Crystal Orientation	183
7.4.2 Uniaxial Strain	184
7.5 Summary	185
References	186

8 Transistor Scaling to the Limit

<i>T.-J.K. Liu, L. Chang</i>	191
8.1 Introduction	191
8.2 Planar Bulk MOSFET Scaling	193
8.3 Thin-Body Transistor Structures	196
8.3.1 Ultra-Thin Body (UTB) MOSFET	197
8.3.2 Double-Gate (DG) MOSFET	199
8.3.3 Tri-Gate (TG) MOSFET	205
8.3.4 Back-Gated (BG) MOSFET	205
8.4 Fundamental Scaling Limit and Ultimate MOSFET Structure	207

8.5	Advanced Gate-Stack Materials	209
8.5.1	High- k Gate Dielectrics	209
8.5.2	Metallic Gate Electrode Materials	210
8.6	Performance Enhancement Approaches	213
8.6.1	Enhancement of Carrier Mobilities	213
8.6.2	Reduction of Parasitic Components	215
8.6.3	Alternative Switching Devices	216
8.7	Summary	216
	References	217

Part III Future Directions

9 Beyond CMOS Electronics: Self-Assembled Nanostructures

<i>T.I. Kamins</i>	227
9.1 Introduction	227
9.1.1 Conventional “Top-Down” Fabrication	227
9.1.2 “Bottom-Up” Fabrication	228
9.2 Strain-Induced Nanostructures	229
9.3 Metal-Catalyzed Nanowires	235
9.3.1 Catalyst Nanoparticles	235
9.3.2 Nanowire Growth	238
9.3.3 Germanium and Compound-Semiconductor Nanowires	241
9.3.4 Doping Nanowires	243
9.3.5 Connecting Nanowires	244
9.3.6 Comparison of Semiconducting Nanowires and Carbon Nanotubes	250
9.4 Potential Applications of Metal-Catalyzed Nanowires	251
9.4.1 Field-Effect Transistors	251
9.4.2 Field-Effect Sensors	252
9.4.3 Interconnections	252
9.5 Summary	253
References	254

10 Hybrid CMOS/Molecular Integrated Circuits

<i>M.R. Stan, G.S. Rose, M.M. Ziegler</i>	257
10.1 Introduction	257
10.1.1 Top-Down Fabrication vs. Bottom-Up Assembly	257
10.1.2 Typical Molecular Device Characteristics	258
10.2 MolMOS: Integrating CMOS and Nanoelectronics	259
10.2.1 The CMOS/Nano Interface	260
10.2.2 CMOS/Nano Co-design	262
10.3 The Crossbar Array for Molecular Electronics	264
10.3.1 Molecular Memory Structures	265
10.3.2 Programmable Logic via the Crossbar Array	267

10.3.3	Signal Restoration at the Nanoscale: The Goto Pair	268
10.3.4	Hysteresis and NDR based Devices in Programmable Logic	270
10.4	MolMOS Architecture	272
10.4.1	The CMOS Interface & I/O Considerations	272
10.4.2	Augmenting the PMLA with CMOS	272
10.4.3	Array Access for Programmability	273
10.4.4	A More Complete Picture of the Overall Architecture	274
10.5	Circuit Simulation of MolMOS System	276
10.5.1	Device Modeling for Circuit Simulation	276
10.5.2	Functional Verification of a Stand-Alone Nanoscale PMLA	276
10.6	Conclusions and Future Directions	278
	References	279

11 Sublithographic Architecture: Shifting the Responsibility for Perfection

A. DeHon	281
11.1 Revising the Model	281
11.2 Bottom-Up Feature Definition	282
11.3 Regular Architectures	283
11.4 Statistical Effects Above the Device Level	283
11.4.1 Defect and Variation Tolerance	283
11.4.2 Differentiation	284
11.5 NanoPLA Architecture	285
11.6 Defect Tolerance	288
11.6.1 Wire Sparing	288
11.6.2 Crosspoint Defects	290
11.6.3 Variations	291
11.6.4 Roundup	291
11.7 Testing and Configuration	292
11.8 New Abstraction Hierarchy	293
11.8.1 Lessons from Data Storage	293
11.8.2 Abstraction Hierarchy for Computation	293
11.9 Conclusions	295
References	295

12 Quantum Computing

<i>D.P. DiVincenzo</i>	297
12.1 What Is Quantum Computing?	297
12.2 History	298
12.3 Fundamentals	299
12.4 Quantum Algorithms	301
12.5 Realizing a Quantum Computer	303
12.6 Physical Implementations	306
12.6.1 Josephson Junction Circuits	306
12.6.2 Semiconductor Quantum Dots	308

12.6.3 Ion Traps	311
12.6.4 Outlook	312
References	312

Part IV Afterwords

13 Nano-Whatever: Do We Really Know Where We Are Heading?

Phys. Stat. Sol. (a) 202(6), 957–964 (2005)

<i>H. Kroemer</i>	317
13.1 Introduction: “Nano-Talk = Giga-Hype?”	317
13.2 From Physics and Technology to New Applications	317
13.2.1 Kroemer’s Lemma of New Technology	317
13.2.2 Three Examples	318
13.2.3 Lessons	319
13.3 Roots of Nano-Technology	320
13.4 Back to the Future: Beyond a Single Degree of Quantization	320
13.4.1 Quantum Wires	320
13.4.2 Quantum Dots	321
13.5 More Challenges	322
13.5.1 Lithography Alternatives for the Nanoscale	322
13.5.2 “Loose” Nanoparticles	322
13.6 “Other” Quantization Effects	323
13.6.1 Charge Quantization and Coulomb Blockade	323
13.6.2 Magnetic Flux Quantization	323
13.6.3 Spintronics	324
13.7 Meta-Materials	324
13.8 Research vs. Applications Re-visited	325
13.9 Conclusion	326
References	326

14 Silicon Forever! Really?

Solid-State Electr. 50(4), 516–519 (2006)

<i>H.L. Stormer</i>	327
14.1 Motivation	327
14.2.1 The End of Scaling	327
14.2.2 The “Beginning” of Architecture	328
14.2.3 Silicon Stands Tall	329
14.2.4 The Silicon Wart	330
14.2.5 Beyond Lithography	331
14.3 Conclusion	332
14.4 Acknowledgements and Disclaimer	333
14.5 Citations	333

Index	335
--------------------	-----

Into The Nano Era

Moore's Law Beyond Planar Silicon CMOS

Huff, H. (Ed.)

2009, XXVIII, 348 p. 136 illus., Hardcover

ISBN: 978-3-540-74558-7