

Chapter 2

Devices for Low Power Electronics

The introduction of the concept of integrated circuits in 1958 by Jack Kilby and Robert Noyce enabled the electronics industry to achieve a phenomenal growth over the past several decades. The dimensions of semiconductor devices have been continuously shrinking to meet the needed requirements of high speed and low power as demanded by the circuit designers. Moore's law has been a well-established rule of thumb for scaling device dimensions. Minimum feature sizes of MOSFET devices have shrunk considerably since 1970, thereby increasing the number of transistors in a single integrated circuit as illustrated in Figure 2.1.

The minimum features of an integrated circuit and its devices have been scaled down by a factor of 0.7 per technology node every 3 years since 1975 [2]. The rapid scaling of transistors has resulted in increased functionality per single chip, improvement in processing speed and memory capacity, and decrease in cost and power consumption per function.

Figure 2.2 shows the evolution of Intel microprocessor computing power in million instructions per second (MIPS) [3]. The downsides of the increased computing power and increased number of transistors per chip are the increased internal capacitances, higher number of switching events, and higher power dissipation per chip. The power dissipation of a CMOS circuit can be expressed as [4],

$$P = f_{\text{clk}} a C_{\text{tot}} V_{\text{DD}}^2 + V_{\text{DD}} I_{\text{SC}} + V_{\text{DD}} I_{\text{leakage}} \quad (2.1)$$

where f_{clk} is the clock frequency, a is the average switching activity, C_{tot} is the total capacitance, I_{SC} is the short circuit current between the rail-to-rail supply voltage, V_{DD} is the supply voltage, and I_{leakage} is the leakage current. The dynamic power is proportional to the square of the supply voltage, and the power dissipation due to the short circuit current is directly proportional to the supply voltage. In addition, the leakage current has an exponential dependence on the supply voltage. Thus, supply voltage scaling is an effective strategy for low-power circuit design. However, scaling of the supply voltage is associated with the scaling of the threshold voltage. Since the subthreshold current of a deep submicron MOS transistor depends exponentially on the threshold voltage, the leakage current increases drastically for threshold voltage below 300 mV, which effectively

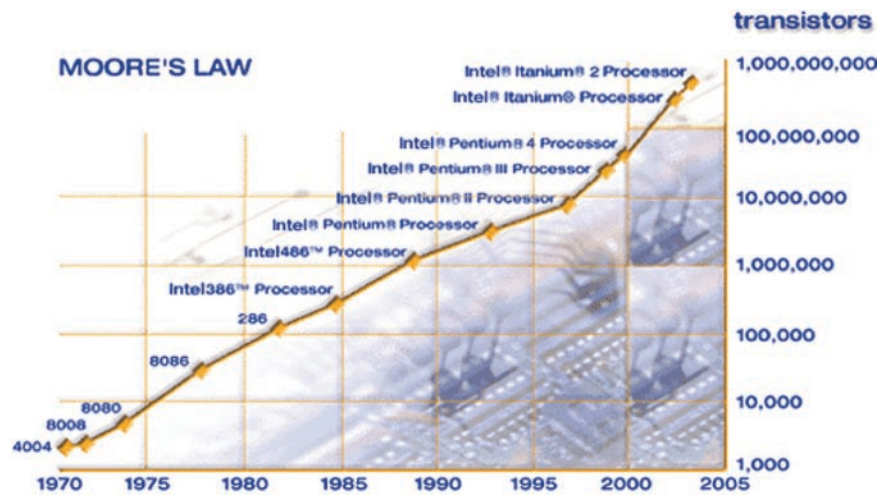


Fig. 2.1 Exponential increases in the number of transistors integrated into Intel processors and other leading platform ingredients validating Moore’s law [1]

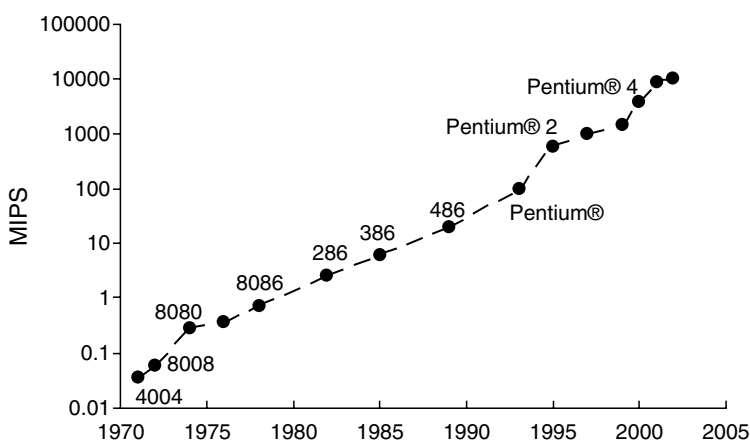


Fig. 2.2 Evolution of performance of Intel Microprocessors [3]

diminishes the benefit of device scaling. Thus, in addition to the choice of a high-end CMOS technology node, a circuit designer also needs to develop strategy for low-power circuit design techniques.

This chapter addresses silicon technology, device scaling, and future trends in device technology for low-power circuit applications, whereas various low-power circuit design techniques will be discussed in subsequent chapters.

2.1 Device Scaling

The evolution of CMOS fabrication technology MOSFETs is miniaturized to account for increased speed and circuit complexity as required by CMOS VLSI technology. The 2008 International Technology Roadmap for Semiconductors (ITRS) lists the principal categories of improvement trends in semiconductor industry as shown in Table 2.1. These trends reflect the ability of the semiconductor industry to continuously decrease the minimum feature sizes of the MOS transistors following Moore’s law. But it is the rapidly decreasing cost-per-function that has led to the realization of highly complex circuits, which are the building blocks of computers, cellular phones, and others consumer and industrial electronics. Figure 2.3 shows the 2007 ITRS product technology trend (updated in 2008), which depicts

Table 2.1 Improvement trends for ICs enabled by feature scaling

Trend	Example
Integration level	Components/chip, Moore’s Law
Cost	Cost per function
Speed	Microprocessor throughput
Power	Laptop or cell phone battery life
Compactness	Small-and light-weight products
Functionality	Nonvolatile memory, imager

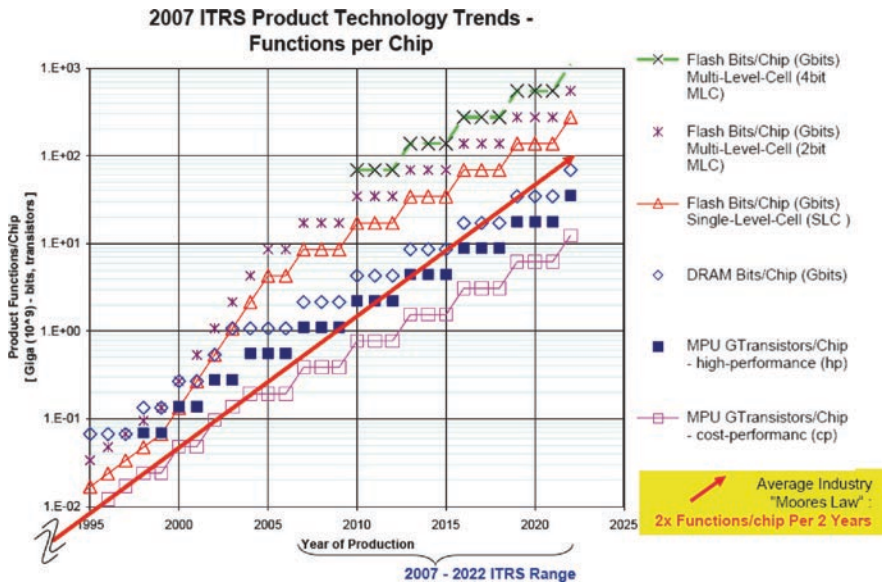


Fig. 2.3 2008 ITRS updated product function size trends showing functions per chip

Table 2.2 Technology nodes and intermediate year minimum feature sizes in nm Per 2007 ITRS

Year of production	2007	2008	2009	2010	2011	2012	2013	2014	2015
MPU physical gate length (nm)	25	23	20	18	16	14	13	11	10

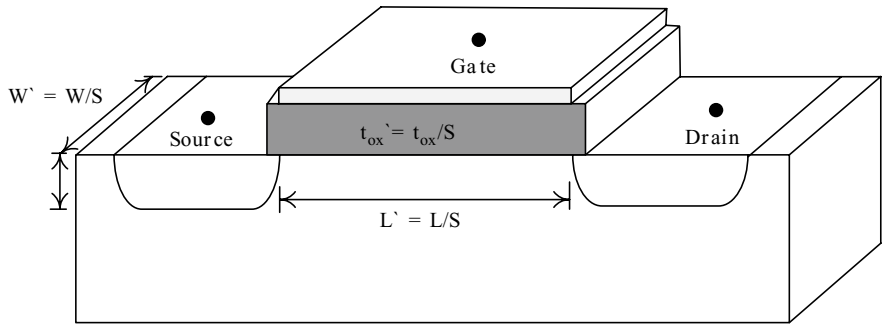


Fig. 2.4 Scaling of a MOSFET by the scaling parameter $S > 1$

the need for increasing number of transistors per chip. Table 2.2 summarizes technology nodes and intermediate year minimum feature sizes in nanometers according to 2007 ITRS.

The term *scaling* is referred to as the reduction of the dimensions of MOSFETs in an integrated circuit. With the reduction of the device dimensions, the operational characteristics of the device change. There are two basic types of scaling strategies: constant field and constant voltage scaling. Figure 2.4 illustrates the reduction of the key dimensions of a MOSFET wherein all the dimensions are scaled down by the same scaling factor, S .

2.1.1 Constant Field Scaling

This scaling strategy, also known as *full scaling*, preserves the same internal electric fields while all dimensions are scaled down by a factor of S . In order to achieve this, all potentials must be scaled down by the same scaling factor. The doping densities are increased by a factor of S to accommodate the relationship between the charge densities and electric field as dictated by Poisson’s equation. The net result of the scaling is that the oxide capacitance is increased by the factor S , while the drain current and power dissipation are reduced by the factor S and S^2 , respectively.

Constant field scaling yields a net reduction in the power-delay product of a single transistor. However, it requires a reduction in the power supply voltage with the reduction in the minimum feature sizes, which is not practical for most cases.

2.1.2 Constant Voltage Scaling

Constant voltage scaling is generally preferred over the full scaling since it provides voltage compatibility with older circuit technologies. It is particularly suitable for the high end CMOS processes with multiple power supply voltages. In constant voltage scaling method, all MOSFET dimensions are reduced by a factor of S , while the power supply and all the terminal voltages are kept unchanged. However, in order to preserve the charge–field relation, the doping densities need to be increased by a factor of S^2 . The net result of the scaling is that the oxide capacitance is increased by the factor S , while the drain current and power dissipation are both reduced by the factor S .

The disadvantage of constant voltage scaling is that the electric field increases as the minimum feature length is reduced. The power density increases by a factor of S^3 , while in full scaling case, it remains virtually unchanged. The large increase in current and power densities may lead to velocity saturation, electromigration, hot carrier degradation, mobility degradation, increased leakage currents, and lower breakdown voltages. Table 2.3 compares the constant field and constant voltage scaling of MOSFET device parameters.

As the device dimensions are reduced, various physical limitations, such as internal electric field, become very prominent which restricts further scaling. Although constant electric field scaling is more practical, the idea of reducing voltage in proportion to reduced dimensions has not been popular due to the substantial increase in electric field. A generalized scaling law has been reported where the electric field patterns within a scaled device are still preserved, but the intensity of the electric field can be changed everywhere within the device by a multiplicative factor ϵ [5]. One common technique for reducing power is to reduce the supply voltage. However, in CMOS circuits, lower supply voltage results in inferior performance. Scaling the threshold voltage can limit this performance loss somewhat. But scaling the threshold voltage of the devices down along with the applied voltage increases the standby leakage current, which limits how far it is practical to scale the power supply voltage.

Table 2.3 Comparison of the effect of scaling on MOSFET device parameters

Parameter	Symbol	Constant field scaling	Constant voltage scaling
Gate length	L	L/S	L/S
Gate width	W	L/S	L/S
Electric field	E	E	ES
Oxide thickness	t_{ox}	t_{ox}/S	t_{ox}/S
Substrate doping	N_a (or N_d)	$N_a S$	$N_a S^2$
Oxide capacitance	C_{ox}	$C_{ox} S$	$C_{ox} S$
Drain current	I_D	I_D/S	
Power dissipation	P	P/S^2	
Power density	P/area	P/area	$P/\text{area} \times S^3$

2.2 Silicon-on-Insulator CMOS

Moore's law has been the primary driving factor for over the last 40 years for the enhancement of device performances by continuously scaling down the feature sizes of the devices. The relentless drive for improved performance with simultaneous reduction of cost has resulted in the scaling of circuit elements to smaller dimensions [6].

With the maturation of silicon technology, bulk-Si devices have emerged as the active element for very large-scale integration (VLSI) circuits. However, a number of fundamental limits, such as decreasing carrier mobility due to impurity scattering and increasing gate tunneling current as the junction becomes shallower, have slowed down the growth of performance of the bulk-Si devices. These trends make conventional scaling less feasible. Since scaling of the power supply voltage degrades performance, the operating voltage tends to be set higher than that needed by a scaled down device in order to achieve the desired speed performance [7].

In bulk-Si technology, multiple transistors are isolated from each other by reverse biased p–n junctions. However, the junction isolation is not always the best approach for integrated circuits since these junctions introduce additional capacitances and reduce the density of the transistors in the circuits. At high ambient temperatures, the leakage currents diminish the isolation among the various circuit components.

Silicon-on-Insulator (SOI) wafers have been used commercially for decades as substrates in discrete and integrated circuits. The initial applications of SOI were mainly in extreme operating temperature for military and space applications. The key advantages of the SOI wafers are low junction capacitance, low leakage current, high breakdown voltage, resistance to ionization radiation, and robust voltage isolation in integrated circuits. In 1970s and 1980s, the radiation hardness of SOI circuits was the primary motivator for choosing these substrates as the thin, active Si films minimized the impact of ionizing radiation on device performance. Currently, the performance enhancement needs to motivate many integrated circuit companies to use SOI wafers. For the same supply voltage, digital logic circuits, such as microprocessors, run faster in SOI than in the bulk-Si. It is also possible to reduce power consumption of the SOI circuits by lowering the operating voltages, while still keeping the clock rate and their performance the same as in more power-hungry bulk-Si circuits. Since their introduction, commercial applications of SOI have grown exponentially, and entered the mainstream of ultra large-scale integration (ULSI) electronic circuits. Figure 2.5 illustrates the growth of market share of SOI technology in the twenty-first century.

SOI technology enables high-speed operation because of the inherently low capacitance. In addition to its advantages of speed and power, SOI technology provides good radiation hardness, ability to withstand high temperatures, ability to handle high voltage, a steep subthreshold characteristics, and improved short-channel effects compared to its bulk-Si counterpart[8]. In addition, the SOI devices are virtually free from latch-up and can be implemented with a smaller layout area as compared to the Bulk-Si devices.



Fig. 2.5 History and forecast of market share of SOI

The SOI technology opens up the possibility of having more than one gate for each transistor due to the presence of two oxide layers. Double Gate MOSFET (DGMOSFET) has been realized in SOI technology, which utilizes the two oxide layers as independent gates to control conduction. This offers more control over the channel and completely or partially eliminates the drawbacks of the bulk-Si technology. However, the maximum number of gates in a transistor is not limited to just two [8]. The number of gates can be extended to four for SOI technology includes two junction gates in addition to the two oxide gates. The transistor with four gates is called a Four Gate Field Effect Transistor (G⁴FET) [9]. The G⁴FET offers all features of the SOI technology. The independent action of the four gates broadens the horizons for mixed-signal applications, quantum wire effects, and quaternary logic schemes.

2.3 Silicon-on-Insulator Structures

In its simplest form, SOI structure uses a layered silicon–insulator–silicon substrate in place of the conventional silicon substrates in semiconductor manufacturing to reduce parasitic device capacitance and thereby improves performance [10]. SOI-based devices differ from the conventional bulk-Si devices in that the silicon junctions are formed in the active layer and a buried oxide (BOX) layer is sandwiched in between the active layer and the substrate, which is also known as handle or base wafer. Figure 2.6 shows the SOI wafer and the cross-section of SOI structure. As a result, the conduction is confined in a thin layer of Si, thereby reducing the loss due to bulk conduction.

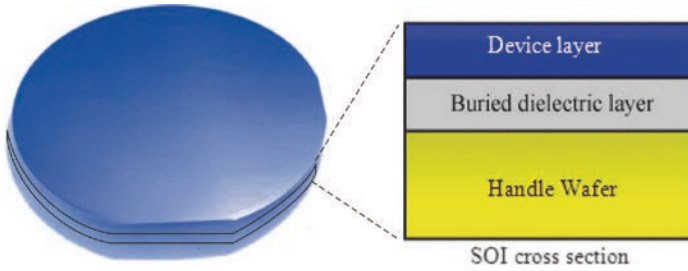


Fig. 2.6 SOI wafer and the cross-section of SOI structure

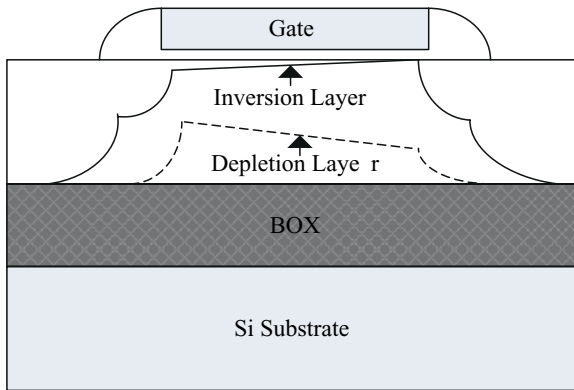


Fig. 2.7 Cross-section of a MOSFET on SOI

Because of isolation from the bulk Si, the SOI technology provides a lower parasitic capacitance compared to the conventional bulk-Si process. This improves power consumption at matched performance and provides resistance to latch-up because of the complete isolation of the n- and p- well structures.

From a manufacturing perspective, the SOI-based process may be implemented without special equipment or significant retooling of an existing factory. However, one of the challenges associated with SOI is stringent metrology requirements to account for the buried oxide layer and concerns about differential stress in the topmost silicon layer. The primary barrier to the commercialization of SOI is the higher substrate cost, which contributes an estimated 10–15% increase to total manufacturing costs [11].

The physics of SOI devices is highly dependent on the thickness and doping concentration of the silicon film on which they are constructed. Figure 2.7 shows the cross-section of a MOSFET realized in SOI. Depending on the thickness of the depletion charge in the top silicon epi-layer, the SOI devices can be classified as fully depleted (FD) and partially depleted (PD) SOI.

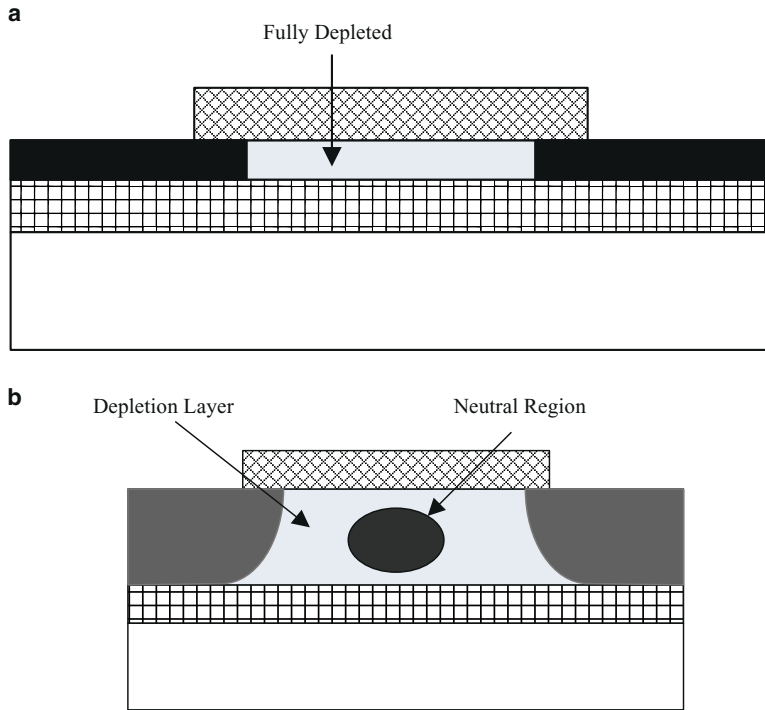


Fig. 2.8 Cross-section, showing depletion of channel, of (a) FDSOI and (b) PDSOI

Figure 2.8 shows the cross-section of (a) FDSOI and (b) PDSOI wafers. It is clear from the figure that the active silicon layer of FDSOI is thinner than that of the PDSOI. It also shows that the channel of the FDSOI is fully depleted, whereas the channel of the PDSOI is partially depleted. Moreover, a PDSOI can be converted to an FDSOI with appropriate bias gate conditions.

The local substrate terminal of the SOI MOSFET floats electrically, and thus the substrate-source voltage is not fixed. This has an adverse effect on the device performance as the change in the substrate-source bias changes the threshold voltage. The floating body effect is minimized by the use of fully depleted SOI. The thickness and doping density of the Si film of the FDSOI is less than that of the PDSOI, which facilitates easy depletion of the Si epi-layer in FDSOI compared to the PDSOI at thermal equilibrium. Initially, FDSOI demonstrated improved short-channel effects [12]. However, as the SOI devices scale down, FDSOI begins to exhibit increased short-channel effects compared to PDSOI unless silicon epi thickness becomes much smaller than the depletion width [13]. On the other hand, in PDSOI, short-channel effects decrease even in comparison with bulk-Si technology with identical doping [14]. Moreover, it is difficult to design a device in FDSOI with reasonable off-state current.

Table 2.4 Comparison between FDSOI and PDSOI [14]

	Partially depleted	Fully depleted
Manufacturability	+	
Design point (high V_t)	+	
Multiple V_t	+	
Breakdown voltage	+	
Short channel effect	+	
Kink effect	+	
Body contact	+	
Passgate leakage	+	
History dependence		+

Table 2.4 summarizes the comparison between the FDSOI and the PDSOI. In order to take full advantages of SOI technology, it is preferable to have a device with a PDSOI.

2.4 High-k Dielectric and Metal Gate Technology

Traditional MOSFETs are formed with an insulating layer of silicon dioxide and a polysilicon gate. The rapid scaling of the devices in accordance with Moore’s law has shrunk the gate oxide layer to merely five atoms in thickness. The reduction of the thickness of the gate dielectric is necessary for increased gate capacitance. Leakage current due to tunneling increases dramatically as the thickness of the gate dielectric scales down below 2 nm, which leads to reduced reliability and increased power dissipation.

If the standard silicon dioxide gate dielectric is replaced with a material with higher dielectric constant than that of the silicon dioxide, it will provide the required high gate capacitance value with larger thickness of the gate oxide, thus leaving room for further scaling. Oxides and silicates of hafnium (Hf) and zirconium (Zr) as well as aluminum oxides (Al_2O_3), titanium dioxide (TiO_2), tantalum pentoxide (Ta_2O_5), and lanthanum oxide (La_2O_3) have received a lot of attention as a possible replacement of silicon dioxide. The dielectric constant of silicon dioxide is about 3.9. The dielectric constant for pure hafnium silicates has been observed in a range between 15 and 25, while that of pure hafnium oxides has been observed at 40. However, for the sake of structural integrity, the manufacturing process used “impure” compounds of HfO_2 , which demonstrates a dielectric constant of over 16. CMOS fabrication industry has settled with hafnium oxide (HfO_2) as the high-k dielectric material due to its ease of integration with the standard CMOS manufacturing process. Figure 2.9 illustrates how the oxide layer thickness and the choice of materials affect the transistor’s gate leakage power [15]. The gate leakage current due to tunneling through the oxide layer has increased 100-fold in last three generations of transistors. The replacement of the gate dielectric by a high-k material has reversed the trend.

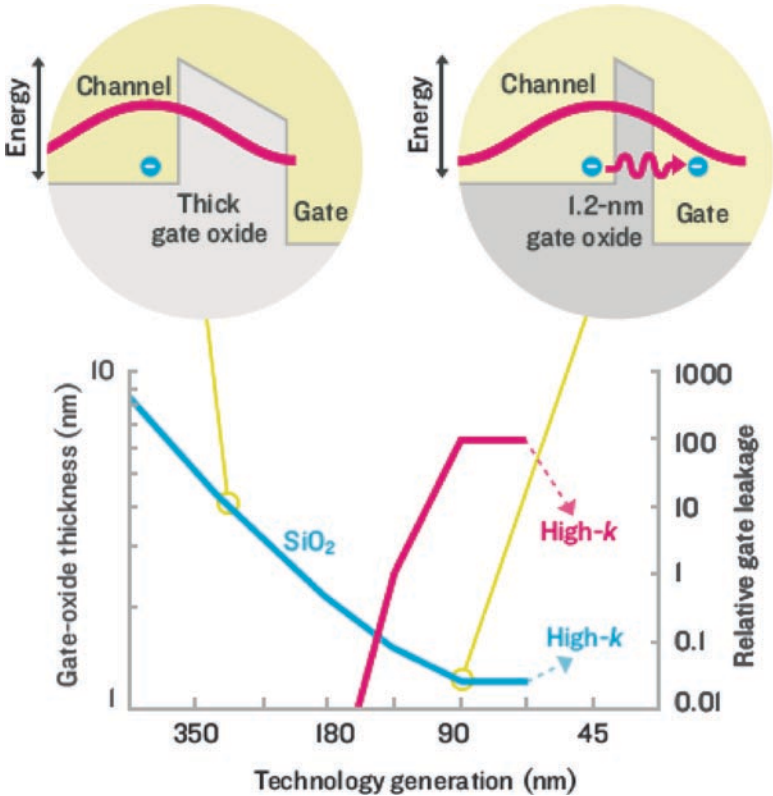


Fig. 2.9 Effect of gate oxide thickness and material on the leakage power of transistors as a function of the technology generation [15]

In the earlier days of MOS transistors, metal has been used as gate electrode materials. But the manufacturing process necessitated the use of polysilicon as a gate material replacing the metals. For the new generation of CMOS process using high-k gate dielectric, polysilicon has been initially used, but the device performance was poor compared to traditional low-k dielectric devices. This was due to the reduced mobility in the channel caused by phonon scattering. The particular density of electrons in the polysilicon gate allows inherent vibrations or phonons which move into the transistor channel, thereby disrupting the flow of current. On the other hand, higher density of electrons in the metal screens out vibrations allowing a smooth flow of current.

In addition, the combination of high-k dielectric and polysilicon gate increased the threshold voltage because of Fermi-level pinning caused by defects in the polysilicon high-k interface. As a result, the process engineers resorted to metal gate electrodes, which solved the issue of phonon scattering as well as Fermi-level pinning.

2.5 Summary

The rapid scaling of the CMOS process along with the development of silicon-on-insulator technology has facilitated the circuit designers to develop low-power circuits for sensor electronics. The recent development of CMOS processes incorporating high-k dielectric has led to further development of the highly complex integrated circuits with significantly reduced power dissipation. Combining the CMOS process enhancement with low-power circuit design strategies has launched a revolution in low-power sensor technologies and proliferation of various sensors in our everyday lives.

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