

Preface

To the observer, it would appear that New York city has a special place in the hearts of integrated circuit (IC) designers. Manhattan geometries, which mimic the blocks and streets of the eponymous borough, are routinely used in physical design: under this paradigm, all shapes can be decomposed into rectangles, and each wire is either parallel and perpendicular to any other. The advent of 3D circuits extends the analogy to another prominent feature of Manhattan – namely, its skyscrapers – as ICs are being built upward, with stacks of active devices placed on top of each other. More precisely, unlike conventional 2D IC technologies that employ a single tier with one layer of active devices and several layers of interconnect above this layer, 3D ICs stack multiple tiers above each other. This enables the enhanced use of silicon real estate and the use of efficient communication structures (analogous to elevators in a skyscraper) within a stack.

Going from the prevalent 2D paradigm to 3D is certainly not a small step: in more ways than one, this change adds a new dimension to IC design. Three-dimensional design requires novel process and manufacturing technologies to reliably, scalably, and economically stack multiple tiers of circuitry, design methods from the circuit level to the architectural level to exploit the promise of 3D, and computer-aided design (CAD) techniques that facilitate circuit analysis and optimization at all stages of design. In the past few years, as process technologies for 3D have neared maturity and 3D circuits have become a reality, this field has seen a flurry of research effort. The objective of this book is to capture the current state of the art and to provide the readers with a comprehensive introduction to the underlying manufacturing technology, design methods, and computer-aided design (CAD) techniques. This collection consists of contributions from some of the most prominent research groups in this area, providing detailed insights into the challenges and opportunities of designing 3D circuits.

The history of 3D circuits goes back many years, and some of its roots can be traced to a major government-funded program in Japan from a couple of decades ago. It is only in the past few years that the idea of 3D has gained major traction, so that it is considered a realistic option today. Today, most major players in the semiconductor industry have dedicated significant resources and effort to this area. As a result, 3D technology is at a stage where it is poised to make a major leap. The context and motivation for this technology are provided in Chapter 1.

The domain of 3D circuits is diverse, and various 3D technologies available today provide a wide range of tradeoffs between cost and performance. These include silicon-carrier-like technologies with multiple dies mounted on a substrate, wafer stacking with intertier spacings of the order of hundreds of microns, and thinned die/wafer stacks with intertier distances of the order of ten microns. The former two have the advantage of providing compact packaging and higher levels of integration but often involve significant performance overheads in communications from one tier to another. The last, with small intertier distances, not only provides increased levels of integration but also facilitates new architectures that can actually improve significantly upon an equivalent 2D implementation. Such advanced technologies are the primary focus of this book, and a cutting-edge example within this class is described in detail in Chapter 2.

In building 3D structures, there are significant issues that must be addressed by CAD tools and design techniques. The change from 2D to 3D is fundamentally topological, and therefore it is important to build floorplanning, placement, and routing tools for 3D chips. Moreover, 3D chips see a higher amount of current per unit footprint than their 2D counterparts, resulting in severe thermal and power delivery bottlenecks. Any physical design system for 3D must incorporate thermal considerations and must pay careful attention to constructing power delivery networks. All of these issues are addressed in Chapters 3–6.

At the system level, 3D architectures can be used to build new architectures. For sensor chips, sensors may be placed in the top tier, with analog amplifier circuits in the next layer, and digital signal processing circuitry in the layers below: such ideas have been demonstrated at the concept or implementation level for image sensors and antenna arrays. For processor design, 3D architectures allow memories to be stacked above processors, allowing for fast communication between the two and thereby removing one of the most significant performance bottlenecks in such systems. Several system design examples are discussed in Chapters 7–9. Finally, Chapter 10 presents a methodology for cost analysis of 3D circuits.

It is our hope that the book will provide the readers with a comprehensive view of the current state of 3D IC design and insights into the future of this technology.

Sachin Sapatnekar

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Xie, Y.; Cong, J.J.; Sapatnekar, S. (Eds.)

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