

# Preface

Power consumption has already become a critical issue that must be taken into consideration when developing and implementing modern integrated circuits and systems. In many application markets enabled by portable devices, the limited energy supply, which is available in-field by means of either energy scavenging or rechargeable batteries, is defining key product features, such as the form factor or the “talk time” for mobile phones. For example, the power budget for today’s smartphones is in the range of 2–4 W. When excluding the power required for operating the user display and radios, there is approximately 1 W available for almost 100 billion operations per second needed by the digital workload. The continuous user demand to further expand the functionality of portable devices, without affecting the key product features, imposes tight constraints on the design technology with power optimization as its focal point. Besides, power impacts the cost of fabrication, packaging and cooling, as well as the system’s reliability and its maintenance cost. With the proliferation of cloud computing and data centers, the power requirements for this elaborate computing infrastructure may exceed 100 MW in the foreseeable future. Therefore, even a modest 10% reduction in the average power consumed by each circuit in a server farm can visibly reduce the operational expenses.

Given the above trends, in the past two decades, we have witnessed extensive research and development in the area of low-power circuits and systems. A large pool of circuit techniques, design methodologies and tool flows have been invented by exploiting redundancies in the implementation space and manipulating design parameters, such as scaling the supply voltage, dynamically adjusting the operating frequency at runtime, gating clocks to match the circuit activity to the application workload; or modifying the software and/or the processor architecture, only to mention a few well-established solutions. In addition to the above, according to Moore’s Law, there was a steady shift to finer semiconductor process geometries, which also enables a power reduction for each device, if the same level of functionality is preserved. Nonetheless, as the number of transistors integrated onto a silicon die has increased, and because the number of pins available for screening the devices for fabrication defects is not scaling at the same rate, the cost of manufacturing test is on the rise. This problem has been exacerbated by both the new types of defect mechanisms that have been found in advanced process technologies and the test constraints unique to low-power devices.

This book provides a comprehensive coverage of the established interrelationships between low-power design and manufacturing test of integrated circuits. It deals with both power-aware testing that addresses excessive, and potentially damaging, power surges that occur only during test, and the unique test challenges posed by the power-management techniques. The material takes the reader from the fundamental principles to the advanced concepts in the field and all the known directions of work are explored, ranging from low-power automatic test pattern generation and power-aware design-for-test to the core test strategies for low-power devices.

Chapter 1 provides the background material on manufacturing test of very large-scale integrated (VLSI) circuits. Fundamental concepts such as defects, fault models and coverage, manufacturing yield, defect level, logic testing and memory testing are introduced. The basic algorithms and methods developed to make VLSI test tractable, such as automatic test pattern generation (ATPG), design-for-test (DFT), built-in self-test (BIST) and test data compression, are also described in this chapter.

Sudden changes in power consumption affect supply voltage levels, while variations in chip temperature, caused by excessive power, can affect both reliability and timing. These are only two power-related issues that affect the testing process. Chapter 2 elaborates this relationship between power consumption and VLSI test in detail and it presents basic concepts such as power droop, power delivery and on-chip thermal gradients. How power impacts test throughput and yield loss, both of which influence test economics, is also discussed.

ATPG algorithms have been researched for over four decades and they have become ubiquitous in test tools. However, the unique challenges posed by power consumption during test introduce a new dimension to the ATPG problem. The key advantage of using an ATPG-based approach to reduce test power lies in its algorithmic nature, where the added effort is placed during test preparation and there is no area or performance overhead on-chip. Chapter 3 details the recent developments in low-power ATPG, including also advanced concepts such as low-power test compaction, low-power filling of don't care values in test patterns, low-power test vector ordering during scan testing and low-power algorithms for memory testing.

Chapter 4 discusses low-power DFT techniques. Employing scan chains to improve the controllability and observability of state elements is the most common DFT technique. However, the power consumed during the shift cycle in the combinational logic blocks brings no value to the testing process. Hence, gating the outputs of scan cells during shift can be employed to eliminate the useless circuit activity. DFT techniques for low-power test facilitate or can be combined with other test power reduction techniques such as test planning and low-power ATPG. Therefore, more advanced DFT techniques for test-power reduction, such as test clock gating, low-power scan cell design, scan chain partitioning and ordering of scan cells, among others, are discussed in this chapter.

Due to the steady growth in the design complexity and the variety of fabrication defects in modern process technologies, both the number of bits per test pattern and the number of test patterns are increasing, thus causing a test data volume problem. BIST and test data compression are the two main approaches employed to deal with

the excessive test data volume. Chapter 5 describes several low-power BIST and test data compression techniques, by pointing out their advantages and disadvantages in terms of area, performance and power. The discussion is focused on both entropy coding techniques, as well as compression based on linear-feedback shift registers, which are commonly used as pseudorandom sequence generators in BIST.

A modular approach based on the design reuse philosophy has been widely adopted for system-on-chip (SOC) designs. Testing SOC's can also be done in a modular fashion. An important advantage of using a modular test strategy is the ability to develop test plans that are power-aware. Chapter 6 contains an introduction to core-based testing, followed by a discussion on test power modeling and test plan scheduling. The advantages of a modular approach are also highlighted for SOC's with multiple clock domains and when monitoring the steady-state current.

In the previous chapters, the focus has been placed on algorithms and techniques for low-power testing, with the main objective on avoiding overstressing and overheating the devices. In the second part of the book, the focus shifts toward low-power devices and the unique test challenges posed by the power-management structures. Chapter 7 provides an overview of the adopted design techniques for the static and dynamic power reduction. For a better understanding of the following chapters, it discusses the impact of low-power design techniques on test and it covers the test implications of the post-silicon adaptation approaches for power reduction.

Using multiple supply voltages (also called multi-voltage or multi-V<sub>dd</sub>) enables dynamic voltage scaling, which is often employed in practice to match the circuit speed and power at runtime to the application workload. Chapter 8 discusses testing strategies for multi-voltage designs. There are fabrication defects which have V<sub>dd</sub> dependency and hence they can be activated at some but not at all the power supply settings. Due to cost considerations, the aim is to screen the fabrication defects by avoiding repetitive tests at several V<sub>dd</sub> settings. To adequately address this unique test challenge, new techniques for defect modeling, test generation and DFT have been investigated in recent years. Some of these techniques, such as test point insertion, elevated V<sub>dd</sub> testing and low-cost scan for multi-voltage design, are presented in depth in this chapter.

Another widely adopted low-power technique is to gate off clocks to logic blocks that are not doing any useful computations in the present state. Chapter 9 discusses DFT approaches that deal with gated clocks, such that the ATPG algorithms can be reused and correctly interpret the operation of gated clocks to avoid any loss in test coverage. Besides, as elaborated in this chapter, clock-gating logic, which is inserted for lowering power during the functional operation, can also be leveraged to reduce the switching activity during both test application and test data loading/offloading through scan.

Power management techniques used in low-power circuits commonly rely on special low-power cells such as level shifters, state-retention registers and isolation cells. To ensure that the defect level is not affected by not screening these cells adequately for fabrication defects, in addition to testing logic and memory blocks,

the power-management structures also need to be tested in a structured way. Chapter 10 discusses different methods for testing low-power cells and for validating the integrity of power distribution networks in low-power devices.

Unlike the previous chapters, the last one is focused neither on techniques for reducing power during test nor on testing the power-management structures present in low-power devices. Rather its focus is on explaining the unique challenges posed by integrating these techniques in electronic design automation (EDA) tool flows. For example, on the one hand, DFT insertion tools must be power-aware so that scan is robustly implemented across different clock and voltage domains. On the other hand, the power overhead of the DFT logic must be minimal. Hence, as elaborated in Chapter 11, EDA tool users must be provided with the choice to reach trade-offs, since DFT and low power can present conflicting constraints and implementation costs.

Low-power design and manufacturing test are well-researched and published topics in the broad field of VLSI circuits and systems. However, given the technology trends from the past decade and the stronger interrelation between power and test, this book provides the first comprehensive reference material on power-aware testing and testing low-power devices. It covers the fundamentals, the established techniques that have been adopted in practice and the latest research in the field. It is hoped that this book will have a two-pronged effect: to provide the reader with the fundamental material to be used as a reference and to motivate further innovation in the field. Therefore, it can become a valuable asset for a diverse group of readers: VLSI design and test professionals, EDA tool developers, academics that are planning to develop or to bring their course material up to date and, most importantly, students who are entering in the VLSI and EDA fields.

Montpellier, France  
Hamilton, Canada  
Iizuka, Japan

*Patrick Girard*  
*Nicola Nicolici*  
*Xiaoqing Wen*

Power-Aware Testing and Test Strategies for Low Power  
Devices

Girard, P.; Nicolici, N.; Wen, X. (Eds.)

2010, XXI, 363 p., Hardcover

ISBN: 978-1-4419-0927-5