

Chapter 2
Development of a DVI-Compatible VGA Projector Engine Based on Flexible Reflective Analog Modulators

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Abstract The development of a Digital Video Interface (DVI) – compatible VGA projector engine based on Flexible Reflective Analog Modulator (FRAM) is reported. The FRAM technology development began a few years ago in response to a need for a new projection technology allowing the achievement of ultrahigh resolution for high fidelity simulations. This technology relies on simple micromirrors produced using typical Micro Opto Electro Mechanical System (MOEMS) manufacturing processes. It has the advantages of offering a simple fabrication process (three masking layers), a quick response time (5 μs) and to be wavelength insensitive over large spectral ranges. Additionally, the light modulation with these microdevices does not require the achievement of a very high quality optically flat state of the micromirrors which is typically difficult to obtain yet necessary for other MOEMS modulation technologies.

Testing and FRAM array selection for packaging: One challenge of the projector engine development was the packaging of the FRAM dies presenting a high number of input signals (480). For the packaging of such dies, the die-on-board approach was selected. 480 × 1 FRAM arrays appropriate for this packaging approach have been designed, fabricated and tested. Very large arrays (4000 × 1) were also produced within the fabrication run therefore confirming the feasibility of such arrays. Testing in itself represented a challenge. Actually, it was critical to select a 480 × 1 FRAM array with a pixel functionality percentage as high as possible to minimize the presence of dead rows in the projected image. Reaching this goal implied that the fabricated FRAM arrays should be carefully inspected and tested. In practice, testing all FRAMs of many 480 × 1 arrays before packaging is not straightforward. The

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difficulty here is that the time and cost required for such testing must remain reasonable. This requires many FRAMs to be activated and tested at once. Activation of many FRAMs (60) was achieved with a customized probe card combined to a probe station. The response of the activated FRAMs was observed with an optical test bench integrated to the probe station. This test bench was a small and slightly modified version of the optical system used in a projector. A line of light illuminated a number of FRAMs and the light reflected by the FRAMs passed through Schlieren optics to produce pixels in the image plane located at the exit of an optical relay. A camera and a CRT produced a magnified image of the pixels. This provided a convenient method for assessing the functionality of thousands of FRAMs relatively quickly by observing the pixels intensity changes as the voltage applied to the FRAMs was varied.

FRAM array packaging: One 480×1 FRAM array has been selected for final packaging using this method combined with complementary interferometric microscope measurements. A flex board/metallic package assembly has been used to implement the selected die-on-board packaging approach. Within the assembly, each FRAM is electrically connected to the flexible PCB using wire bonding. A housing placed over the FRAM array and clamped to the board provides an hermetic enclosure allowing operation of the FRAM array in an inert atmosphere of dry nitrogen. It also provides mechanical protection to the array. It is equipped with an optical window. Small closable inlet and outlet openings allow regeneration of the inert atmosphere if necessary.

Control electronics, software and final assembly: The link between the die-on-board packaging assembly and the control electronics is insured by standard high pin count connectors. This customized control electronics and the associated control software have been developed to allow the transfer of image data to the modulator array. The control electronics includes a DAC board, a FPGA board and a power supply board. The designed electronics and the associated software are compatible with the Digital Video Interface standard. This allows the projection of a variety of images including still images and animated sequences. With the resulting projector engine, images with VGA resolution can be displayed at a frame rate of 60 Hz. Part of the control electronics and the package assembly are mounted on positioning supports. These supports allow a precise optical alignment of the FRAM array. Full functionality of the engine has been verified by integrating it into an existing optical test bench and projecting still images and animations.

Sommaire Le développement d'un engin de projection de format VGA basé sur les Modulateurs Analogues Réflectifs Flexibles (FRAM) et compatible avec le standard DVI est rapporté. La technologie FRAM a été développée il y a quelques années. Cette technologie repose sur des micro-miroirs simples produits en utilisant des procédés typiques pour la fabrication des MOEMS. Elle a l'avantage d'offrir un procédé de production simple (3 niveaux de masquage), un temps de réponse rapide (moins de $5\,\mu s$) et d'être insensible à la longueur d'onde d'opération sur de grandes plages spectrales. De plus, la modulation de la lumière avec ces micro-dispositifs

ne demande pas de réaliser des micro-miroirs présentant un état plan de très haute qualité optique difficile à obtenir mais nécessaire pour d'autres technologies de modulation basées sur les MOEMS.

Tests et sélection de barrettes de FRAM pour la mise en boîtier: Un défi du développement de l'engin de projection était la mise en boîtier de puces FRAM présentant un grand nombre de signaux d'entrée (480). Pour la mise en boîtier de telles puces, l'approche puce-sur-carte a été sélectionnée. Des barrettes de FRAM 480×1 appropriées pour cette approche de mise en boîtier ont été conçues, fabriquées et testées. De très grandes barrettes (4000×1) ont aussi été produites durant la période de fabrication ce qui a confirmé la faisabilité de telles barrettes. Les tests en eux-mêmes représentaient un défi. En effet, il était critique de sélectionner une barrette de FRAM 480×1 avec un pourcentage de fonctionnement des pixels aussi haut que possible. Atteindre ce but impliquait que les barrettes de FRAM fabriquées devaient être inspectées et testées avec soin. En pratique, tester tous les FRAM de plusieurs barrettes 480×1 avant la mise en boîtier n'est pas simple. La difficulté ici est que le temps et le coût requis pour ces tests doivent demeurer raisonnables. Ceci requiert que plusieurs FRAM soient activés et testés en même temps. L'activation de plusieurs FRAM (60) a été réalisée avec une carte à pointes conçue sur mesure combinée à une station de test. La réponse des FRAM activés était observée à l'aide d'un banc de test optique intégré à la station de test. Ce banc de test était une version réduite et légèrement modifiée du système optique utilisé dans un projecteur. Une ligne de lumière illuminait plusieurs FRAM et la lumière réfléchie par les FRAM passait à travers une optique Schlieren pour produire des pixels dans le plan image localisé à la sortie d'un relai optique. Une caméra et un moniteur produisaient une image agrandie des pixels. Ceci fournissait une façon commode pour vérifier le fonctionnement de milliers de FRAM relativement vite en observant les changements d'intensité des pixels quand le voltage appliqué aux FRAM était varié.

Mise en boîtier d'une barrette de FRAM: Une barrette de FRAM 480×1 a été sélectionnée pour la mise en boîtier finale en utilisant cette méthode combinée à des mesures complémentaires réalisées avec un microscope interférométrique. Un assemblage carte flexible/boîtier métallique a été utilisé pour implémenter l'approche de mise en boîtier puce-sur-carte sélectionnée. A l'intérieur de l'assemblage, chaque FRAM est connecté électriquement à la carte de circuit imprimé flexible par microcâblage. Un boîtier placé par-dessus la barrette de FRAM et serré sur la carte fournit une enceinte hermétique permettant l'opération de la barrette de FRAM dans une atmosphère inerte d'azote sec. Il procure aussi une protection mécanique à la barrette. Il est équipé d'une fenêtre optique. De petites ouvertures d'entrée et sortie refermables permettent la régénération de l'atmosphère inerte si nécessaire.

Electronique, logiciel de contrôle et assemblage final: Le lien entre l'assemblage puce-sur-carte et l'électronique de contrôle est assuré par des connecteurs standards présentant un nombre élevé de broches de raccordement. Cette électronique de contrôle sur mesure et le logiciel de contrôle associé ont été développés pour permettre le transfert des données des images vers la barrette de modulateurs.

L'électronique de contrôle comprend une carte DAC, une carte FPGA et une carte d'alimentation. L'électronique conçue et le logiciel associé sont compatibles avec le standard Digital Vidéo Interface (DVI). Cela permet la projection d'une variété d'images incluant des images fixes et des séquences d'animation. Avec l'engin de projection résultant, des images de définition VGA peuvent être affichées à une cadence de 60 Hz. Une partie de l'électronique de contrôle et le boîtier sont montés sur des supports de positionnement. Ces supports permettent un alignement optique précis de la barrette de FRAM. Le plein fonctionnement de l'engin a été vérifié en l'intégrant à un banc de test existant et en projetant des images fixes et des animations.

Nowadays, simulations play a role of increasing importance as training tools. No doubt that this is due to the benefits achievable with this training method which are approaching those of field training yet at a lower cost and often at a lower risk for trainees. This situation is causing some pressure on the required simulation quality due to the trainers' and users' expectations. Flight simulators which are amongst the most complex training tools, in particular those developed for jet fighter pilots, do not escape these trends. Therefore, it is no surprise to observe important ongoing efforts for the improvement of all aspects of these simulators. As a crucial component of the flight simulators, spatial light modulators have received a special attention over the past few years resulting in impressive achievements in terms of resolution, contrast and overall image quality. This paper reports efforts in this field related to the Flexible Reflective Analog Modulator (FRAM) technology. In particular, the development of a Digital Video interface (DVI)-compatible VGA projector engine based on this technology will be described.

A FRAM based projector engine consists of a linear array of $25\,\mu m \times 25\,\mu m$ microbridges which act as flexible micromirrors. Electrostatic actuation allows the control on the curvature of each micromirror independently. When such array is illuminated with a laser and combined with Schlieren optics (van Raalte 1970; see Fig. 2.1), the micromirror curvature variations perform an analog modulation of light intensity. This produces a line of image pixels at the output of an optical relay, each pixel corresponding to one flexible micromirror. This approach allows pixel intensity modulation with switching times in the range of $5\,\mu s$. A complete 2-D image is obtained by using a scanning mechanism that displays each image line sequentially. Additionally, projection optics is used to tailor the final image.

The FRAM arrays are produced using simple fabrication processes typical of Micro Opto Electro Mechanical System (MOEMS) manufacturing. Only three photolithographic masks are required to perform the surface micromachining process developed for the FRAM fabrication. Materials common in the microelectronics industry are used in this process: silicon wafers as substrates, aluminum for the actuation electrodes, silicon nitride for electrical insulation, and polyimide for the sacrificial layer which, when removed, will produce the gap between the micromirror and the substrate and finally aluminum alloy for the micromirrors themselves.

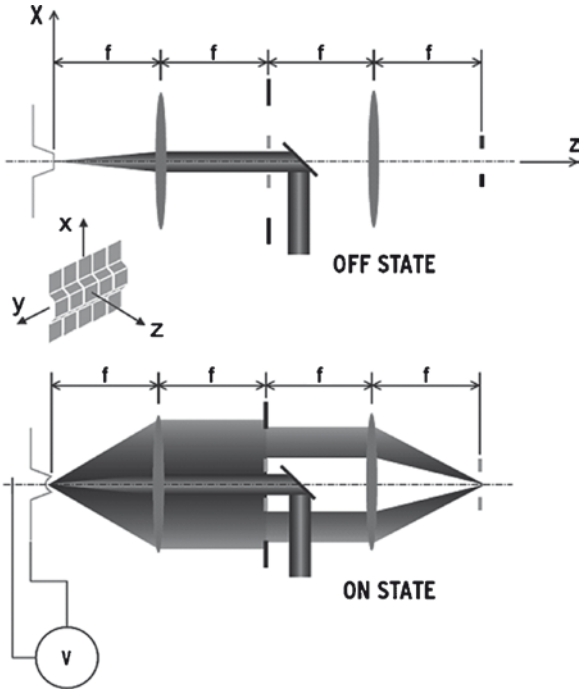


Fig. 2.1 Light modulation approach using a flexible reflective analog modulator (FRAM) array. The few FRAM shown between the OFF and ON state schematic representations indicate the array orientation in the optical setup

The FRAM are typically designed to achieve a maximum curvature corresponding to an f-number of 2. For 25 μm micromirrors, this means producing micromirror sag of about 0.8 μm. Such sag is typically obtained for a voltage of less than 230 V for a micromirror thickness of 150 nm. As mentioned above, response times of the order of 5 μs or less are possible with these micromirrors. Additionally, the FRAM are characterized by a high optical damage threshold of more than 8 kW/cm^2 continuous wave (CW) at 532 nm due to the high reflectivity of these micromirrors (higher than 88% at 532 nm) and to their strong thermal coupling with the substrate. This last feature allows the use of the FRAM arrays with high power laser sources which is not the case for all MEMS based optical modulators.

The development of the FRAM technology began in the year 2000 and since then has progressed to the current state. Following simulations and design, the first FRAM fabrication run was completed and characterized in 2002 (Picard et al. 2002). Projection display using the FRAM technology was demonstrated shortly after (Picard et al. 2003). These achievements have been followed by further studies aimed at improving the micromirror structure (for faster response time, inter alia) and allowing more flexible ways to operate the FRAM arrays for light modulation.

Results of these studies were reported in 2004 (Picard et al. 2004) and 2005 (Doucet et al. 2005). The most recent FRAM technology advances are reported here. They relate the development of a FRAM based DVI-compatible VGA projector engine.

2.1 FRAM Fabrication for VGA Projection Display

The development of a VGA projector engine (640 columns × 480 lines displayed) involved the fabrication of 480 × 1 FRAM arrays with individually addressable micromirrors. The high input count of these arrays led to the selection of a slightly modified chip-on-board approach for the packaging. The requirements related to this packaging approach were also important elements affecting the design of the 480 × 1 micromirror arrays.

As mentioned above the FRAM array fabrication is based on a surface micromachining process involving a polyimide sacrificial layer. The first fabrication step consists of the deposition and patterning of an aluminum thin film on a silicon substrate covered with an electrically insulating silicon nitride layer. This step produces the common electrode located underneath all micromirrors. Second, the polyimide sacrificial layer is deposited and patterned. Of particular importance is the angle of the resulting polyimide structure walls which is a critical parameter affecting the operation of the FRAM. Third, an aluminum alloy film is deposited and patterned to produce the micromirrors. Finally, the sacrificial layer is removed using a plasma ashing step.

Three photomasks were needed for the fabrication of the required FRAM array. They were designed to be used with 6-in. silicon substrates. The mask layout included 288 linear arrays of 480 FRAM, a linear array of 4,000 FRAM, test structures and alignment marks. For the 480 × 1 FRAM arrays, all micromirrors are individually addressable. For the 4,000 × 1 FRAM array, 2,000 micromirrors are individually addressable and 2,000 micromirrors are connected in groups of five mirrors. This last array was included on the masks to investigate the feasibility of such large FRAM arrays.

The required 480 × 1 FRAM arrays have been successfully fabricated using the process described above. Some of the micromirrors from one of the 480 × 1 FRAM arrays are shown at the top of Fig. 2.2. 4,000 × 1 FRAM arrays have also been produced (see Fig. 2.2) within this fabrication run. Static characterization of a few micromirrors from the 4,000 × 1 FRAM arrays has been performed. Typical Deflection vs. Voltage curves (Picard et al. 2003) were generally observed. The voltage for the required maximum deflection (0.8 μm) varied from 171 to 199 V. This demonstrates some pixel-to-pixel non uniformity. Non uniformity was even more evident in some cases. For these FRAM, atypical asymmetric deformations were observed. Such pixel-to-pixel non uniformity was not unexpected in the context of the first fabrication run involving these very large arrays.

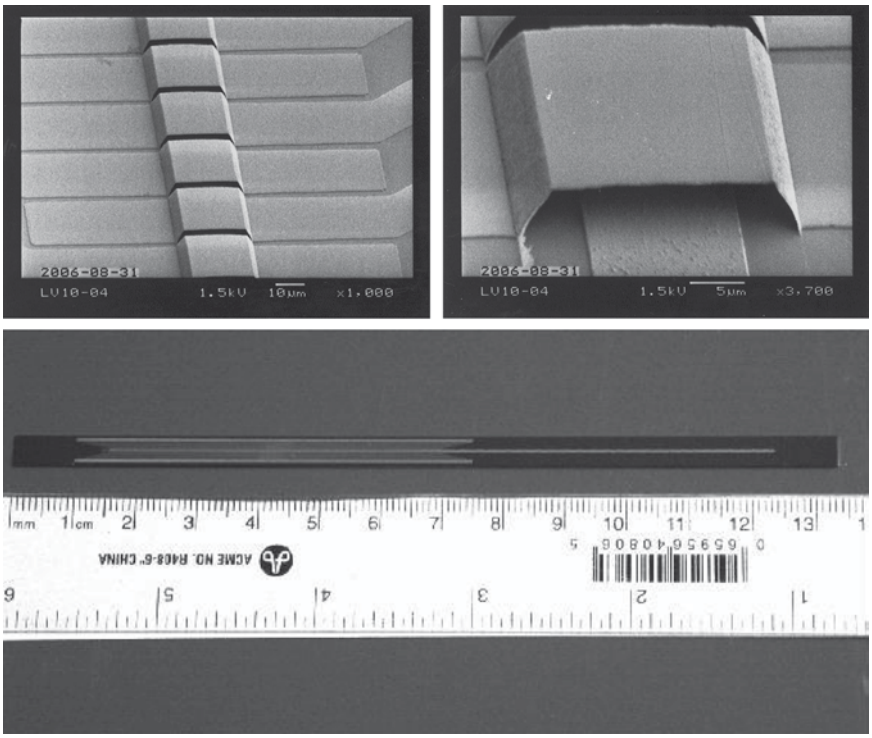


Fig. 2.2 *Top* FRAM arrays with a membrane thickness of 300 nm. *Bottom* 4,000×1 FRAM array

2.2 FRAM Array Testing and Selection

For the planned 640×480 pixel projector engine, it was critical to select a 480×1 FRAM array with a pixel functionality percentage as high as possible. This was required to minimize the presence of dead lines in the projected image. Reaching this goal implies that the fabricated FRAM arrays must be carefully inspected and tested. In practice, testing all FRAM of many 480×1 arrays before packaging is not straightforward. The difficulty here is that the time and cost required for such testing must remain reasonable.

2.2.1 Test Setup

The requirement of testing thousands of FRAM implies in practice that many micromirrors from an array must be actuated and tested at once. This required a setup especially designed for massive evaluation of FRAM functionality. Parallel actuation of 60 FRAM has been achieved by using a customized probe card combined

with a probe station (Cascade Microtech, REL-4800). The response of the activated FRAM was observed with an optical test bench integrated to the probe station. This test bench is a small and slightly modified version of the optical system used for light modulation in a FRAM-based projector. A line of light illuminates about 100 FRAM. The light reflected by the FRAM passes through Schlieren optics to produce pixels in the image plane located at the exit of an optical relay. A CCD camera connected to a computer produces a magnified image of the pixels. The operator of the test setup verifies visually that the pixel intensity profile changes normally as the voltage applied to the FRAM is varied. Once a set of 60 FRAM is checked, the optical setup is removed, the probe card is positioned to actuate the next 60 FRAM and the optical setup is put back in place to validate the response of this new group of micromirrors. The process is repeated until a full array has been tested. This approach provides a convenient way to observe thousands of FRAM relatively quickly and assess qualitatively their functionality.

2.2.2 FRAM Array Screening Procedure

The screening process for the FRAM arrays comprised an initial selection based on a visual inspection with a microscope. Then, the retained arrays went through a partial testing where the Deflection vs. Voltage curve was measured for a few FRAMs on each selected array. The Deflection vs. Voltage curve was obtained using an interferometric microscope. This step allowed further screening of the arrays. The remaining arrays were finally tested on the probe station with the setup described above (Sect. 3.1) to assess, at least qualitatively, the percentage of functional FRAM for a given array.

The developed procedure allowed the testing of FRAM arrays to an extent never approached before. This provided new insights about FRAM behaviour, in particular about their failure mechanism. For standard FRAM (that is, fabricated with the same membrane thickness as previously, i.e. 150 nm) it was relatively easy to find, by visual inspection, arrays with no defective mirror. The same arrays showed a typical Deflection vs. Voltage mirror response when characterized with the interferometric microscope. Ten mirrors were characterized with the interferometric microscope for each array. The maximum voltage to be applied to all mirrors with the probe station setup was based on these measurements. Relatively large variations of the voltage required to reach maximum deflection (0.8 μm) were observed among the characterized mirrors (a few tens of volts). The maximum voltage to apply to the array was set as the minimum voltage observed for maximum deflection within the ten measurements performed minus 15 V to account for the possibility of mirrors with even lower actuation voltages. When this voltage was applied to the whole array (60 micromirrors at once), FRAM were sometimes observed to collapse just beside mirrors which withstood the applied voltage.

The failure in these cases is not due to the sacrificial layer thickness non-uniformity or to the aluminum alloy film thickness non-uniformity. As was observed in previous

fabrication runs, the side walls of the polyimide sacrificial layer are not smooth but present a network of fibre-like structures generally oriented perpendicularly to the FRAM array. This pattern is replicated in the aluminum alloy deposited as the structural layer for the FRAM. These fibre-like structures are somewhat different from one micromirror to another. They are most probably due to the interaction of the oxygen with the silane groups within the polyimide during the RIE etching which produces silicon oxide residues. The resulting wall pattern is unique to each mirror and produces a unique stress distribution within the walls. This unique wall structure can explain either a shift of the Deflection vs. Voltage curve toward low voltages or defective walls with a reduced overall structural strength. Therefore, the stress concentration within the walls can lead to the destruction of one mirror upon actuation while the adjacent mirror withstands the same actuation voltage. Either the pull-in phenomena typical of electrostatic microdevices (Hung and Senturia 1999) or simple structural breakdown can be at the origin of the failure.

This does not necessarily exclude the use of such mirrors for projection display. If the failure mechanism is related to the pull-in phenomena, implementing a pixel-to-pixel non-uniformity correction procedure would solve the problem. If the failure mechanism is rather a structural breakdown occurring before the pull-in voltage is reached then it would be difficult to find arrays offering 100% functionality. In either case, pre-packaging testing with the probe station is not easily applicable and would most probably lead to the destruction of some FRAM within the tested array.

FRAM with thicker walls (300 nm), such as those shown in Fig. 2.2, were also fabricated. These micromirror arrays showed a better mirror-to-mirror Deflection vs. Voltage response uniformity. As expected, the actuation voltage was higher (around 260 V) than for the standard FRAM discussed above. However, the influence of the fibre-like structures in the walls was much lower, as demonstrated by the improved FRAM uniformity. For these arrays, it was possible to select an actuation voltage corresponding to a deflection close to the required maximum for most FRAM. One of these arrays was selected for final packaging after which testing with the probe station setup confirmed a functionality of 100% for this array.

As mentioned above, these arrays show a higher actuation voltage than the standard FRAM. However, they still offer a large useful deflection range but require a higher bias on the common electrode of the array for proper operation. This is compatible with the electronic driver designed for the DVI-compatible VGA projector engine and described in the following section.

2.3 Projector Engine Control

Control software has been developed for the image data transfer from a computer to the projector engine electronics. This Microsoft Windows application allows the loading and transfer of fixed images (.bmp format) and animations (.tmi format).

The image data are transferred to the projector engine through a DVI link. A built-in look-up table (LUT) defined by the user allows individual modification of the Pixel Intensity vs. Grey Level Input relation for each FRAM. This feature allows correction of the pixel-to-pixel non-uniformity when relevant data are available. Alternatively, this LUT can be replaced by a 14-bit linear LUT for which the voltage applied to the FRAM is proportional to the grey level data for all FRAM of the array. Additionally, contrast, brightness and gamma correction can be performed globally on the images before the user-defined LUT (or the 14-bit linear LUT) is applied to the image data. Other features of this software application allow the user to manually adjust frame synchronization and the number of displayed columns.

A built-in tool has also been added to the control software. This tool allows the quick and easy generation of user-defined test images. The tool can be opened as a new window from the main software window. In this window, the user can compose a program of simple instructions. When this program is run, the corresponding image is generated and displayed in the same window. This image can subsequently be saved or saved and loaded directly into the main software application. The programming script is relatively simple but still supports typical features such as basic arithmetical operations, loops, logical operations and conditions.

The Windows application is run on a host PC that feeds the control electronics with a monochrome video stream of size 640×480 pixels at the rate of 60 frames/s. The Windows application requires that a standard DVI interface board be installed in the host PC in order to send the video stream to the electronics through a DVI cable. The control electronics acts as a slave with respect to the host PC. It receives the video stream and forwards the image flow to the 480 micromirrors of the FRAM array. No information is transferred back from the electronics to the host PC. These control electronics consist of an FPGA board, a high-voltage digital-to-analog converter (HV DAC) board and a high-voltage DC power supply board.

The main components located on the FPGA board are a DVI input port for the video stream received from the host PC, a double-buffer of random access memory (RAM), and a CameraLink port for output of the video stream to the HV DAC board. These components are controlled by a VHDL application programmed in a Xilinx Virtex-2 Pro FPGA.

Image data are received as 640×480 pixels/frame, 60 frames/s. The pixel data are 14-bit binary words that are forwarded to the DAC board. Images are received in the standard 640×480 VGA format from the DVI port installed on the host PC. Since the FRAM arrays comprise 480 micromirrors, images must first be stored line-wise as 640×480 in a buffer memory, and then read column-wise as 480×640 during the display process. Such procedure requires a double-buffer structure. A steady video stream between input and output is achieved by writing the first incoming frame to a first buffer, then writing the second incoming frame to a second buffer while the preceding frame is being read simultaneously from the first buffer and so on. This procedure avoids interruptions in the data flow toward the DAC board and the FRAM array.

As its main functions, the VHDL application installed in the FPGA locks to the incoming video stream, manages the proper line-wise/column-wise addressing scheme for read/write accesses in the double-buffer memory structure and issues

frame synchronization to the DAC board. Images are sent from the FPGA board to the DAC board through a CameraLink port. Sending a full image frame nominally takes 1/60 of a second. This period is partitioned as 13 2/3 ms for writing the frame in the digital-to-analog converters and 3 ms to allow an eventual scanning device to return to its initial position before it can display a new frame. All micromirrors are driven as blanked lines (0 V applied) during this return interval.

The CameraLink port provides 24 independent data channels and each channel is used as a serial data link to access the serial input port of each of 24 multi-DAC chips installed on the DAC board. Each multi-DAC chip contains 32 individual 14-bit DACs, but the application timings permit using only 20 of the 32 available DACs on each chip. Since the VHDL application in the FPGA accesses the 24 channels in parallel, writing a single 480-pixel column requires 20 consecutive write operations to the 24-bit Camera Link port and this procedure must be repeated 640 times for a complete 480×640 frame to be written in the DAC. The number of 480-pixel columns that are written into the DAC is defined by the user and can vary from 480 to 640. If desired, this allows the adjustment of the time available for the HV DAC outputs to reach the required voltage values and stabilize.

The Digital-to-Analog Converter Board comprises 480 individuals 14-bits DAC grouped into 24 AD5535 Analog Devices chips assembled on the printed circuit board. A common voltage reference signal is connected to each AD5535 chip. This signal allows the setting of the maximum output voltage from 50 to 200 V. The so called FRAM PC board further discussed below and comprising the packaged FRAM array is connected directly to the DAC board. Since images are displayed column-by-column, the DAC board also provides a signal available to drive a galvanometer which is the scanning device typically used to produce a 2-D image. This driving signal is a periodic triangular waveform that can be synchronized with the frame rate of the incoming video stream. In addition, the rising time, falling time and amplitude of the triangular waveform can be set with potentiometers as part of the galvanometer driver circuit.

2.4 480×1 FRAM Array Packaging

The packaging of microdevices exhibiting hundreds of I/O pads is generally a challenge. Typically no off-the-shelf packages are available to fulfill all requirements for such packaging tasks. The FRAM arrays used to produce the VGA projector engine, with their 481 bonding pads to be connected, are no exception. Therefore, a custom package and packaging procedure have been developed to link all micromirrors to the control electronics. The selected packaging approach is a modified die-on-board packaging method. In this approach, the FRAM array silicon die is glued to a metallic package base plate with a low outgas rate epoxy. This assembly is then secured to the FRAM PC board with screws. The FRAM PC board is a high density two-layer printed circuit. Its central region is rigid and comprises all bonding pads for the FRAM connection. The resolution of the metal traces in this region is very high, close to the current limit of the technology.

A hole in the center of this region allows the positioning of the FRAM die in close proximity with the PC board bonding pads by passing it through the board, the base plate of the package remaining at the back of the FRAM PC board. Both external sides of the FRAM PC board are also rigid. This is where high pin count standard connectors are mounted. These connectors provide the link between the FRAM PC board and the DAC board. Finally, the part of the FRAM PC board linking the connectors to the central region is flexible and exhibits a high density connection routing. A large hole and slits in this flexible part of the board increase the compliance of the mechanical link between the connectors and the FRAM array. At this point of the packaging process, the package base plate being attached to the FRAM PC board, wire bonding is performed between the FRAM array bonding pads and the FRAM PC board pads.

In the next step of the packaging procedure, a fused silica window with AR coatings is placed in a groove machined in the package cover and secured with a window holder and screws. Silicone is then injected in a groove surrounding the window through holes in the window holder. This assembly provides a hermetic joint between the window and the package cover and can be reworked if required. This is an important advantage for such an experimental packaging approach.

The package cover is then attached to the package base plate. In this process, both package parts are pressed against the central portion of the FRAM PC board which is in between. Silicone o-rings placed in grooves machined in the cover and the base plate ensure a hermetic assembly. At this point, the package enclosure must be purged with dry nitrogen. This step allows the operation of the FRAM array in an inert atmosphere which is generally required for Micro-electrical Mechanical Systems (MEMS) devices. Two holes in the package base plate allow this purge. A small tube is inserted in one of these holes and a low flow of dry nitrogen is circulated in the package for 24 h. After this period, the two holes are plugged with flat headed screws equipped with small o-rings which hermetically close the package cavity. All the purging operations described above are performed in a glove box purged with dry nitrogen to insure that no contamination of the package atmosphere occurs during the final closure of the purge holes. The purging manipulation can be repeated to regenerate the package atmosphere after a given operation period, if required. Four holes located at the outer margin of the package allow its attachment to positioning stages or supports, if needed. The assembly obtained with the packaging procedure described above is shown in Fig. 2.3.

2.5 Projector Engine Integration

All components of the projector engine have been assembled within an existing test bench. This test bench provides the required optical setup to produce images with the fabricated projector engine. In its current state, this test bench can illuminate up to 250 pixels which translates to 640 columns × 250 lines images on the screen. The resulting projection device is shown in Fig. 2.4. Part of the positioning stages is

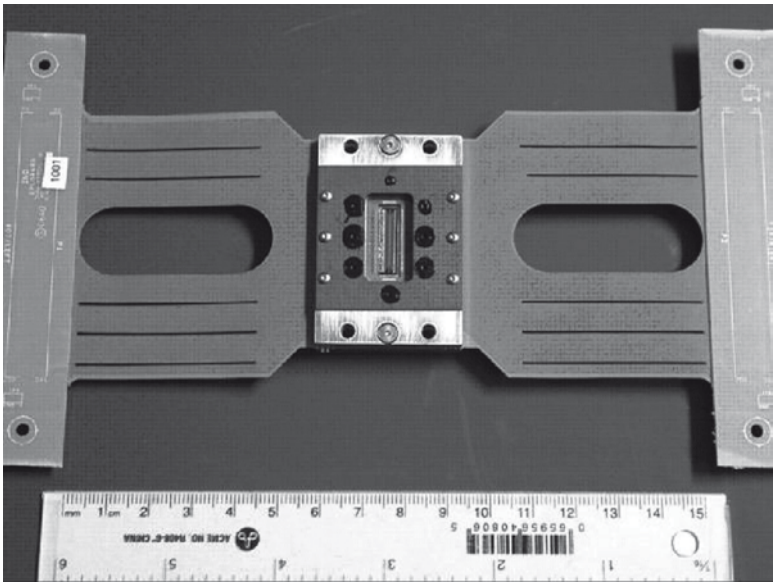


Fig. 2.3 Packaged 480×1 FRAM array

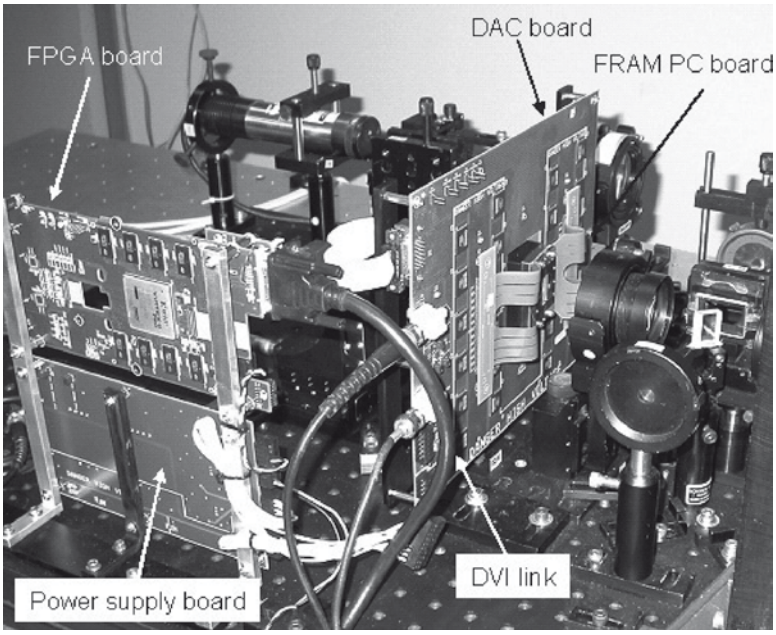


Fig. 2.4 The projector engine and part of the optical test bench

attached to the DAC board and allows coarse positioning of the DAC board/ FRAM PC board assembly. Part of the positioning stages is attached directly to the FRAM array package through a hole in the DAC board. This configuration is advantageous since it allows fine alignment of the micromirror array by moving only the small mass of the FRAM array package. The flexible links between the FRAM array package and the DAC board make this arrangement possible.

Final tests confirmed that the projection engine allows the projection of VGA still images or animations at a frame rate of 60 Hz. All features of the control software and of the control electronics are functional.

2.6 Conclusion

The goal of the work was the demonstration of a projector engine based on the FRAM technology and capable of displaying 640×480 pixels at a frame rate of 60 Hz. To meet this objective, a new data/FRAM interface for a 480×1 FRAM array has been designed and fabricated. Customized control software allows the transfer of image data to the interface. The control electronics includes a DAC board, a FPGA board and a power supply board. The designed electronics and the associated software are compatible with the Digital Video Interface (DVI) standard. This allows the projection of a variety of images including still images and animation sequences. In addition, 480×1 FRAM arrays appropriate for the selected packaging approach (modified chip-on-board) have been designed, fabricated and tested. Full testing of 480×1 arrays before packaging has been successfully achieved by combining a specialized optical setup with a probe station. Very large arrays (4,000×1) were also produced within this fabrication run therefore confirming the feasibility of such arrays.

One 480×1 FRAM array has been selected and packaged using a PC board/ metallic package assembly. This assembly has been connected to the data/FRAM interface. Integration of the projector engine into an existing test bench has been performed. Tests confirmed that the projector engine allows the projection of VGA format still images or animations at 60 Hz. All features of the control software and of the control electronics are functional.



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