Chapter 2
HiSIM-HV: A Scalable, Surface-Potential-Based Compact Model for High-Voltage MOSFETs

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Abstract The main features of the industry standard compact model HiSIM-HV for high-voltage MOSFETs are described. The basis of HiSIM-HV is a consistent physically correct potential determination in the MOSFET core and the surrounding drift regions, providing the high-voltage capabilities. Consequently, HiSIM-HV can accurately calculate the physical potential distribution in the entire asymmetric LDMOS structure or the symmetric HVMOS structure and determine all electrical and thermal high-voltage MOSFET properties without relying on any form of macro modeling or sub-circuit formulation. Furthermore, HiSIM-HV's consistent potential-based approach enables the reproduction of all structure-dependent scaling properties of high-voltage MOSFET features with a single global parameter set. The full scaling properties of HiSIM-HV with respect to the MOSFET-core geometry parameters of gate length and gate width as well as the drift-region parameters of drift-region length and drift-region doping are unique among the available compact high-voltage MOSFET models. Continuous development of HiSIM-HV is carried out in cooperation with the international semiconductor industry and improved versions of HiSIM-HV are released 2 times per year through the Compact Modeling Council (CMC).

Keywords High-voltage MOSFET · LDMOS · HVMOS · Surface potential · Consistent potential distribution · Drift region · Global parameter set · Scaling properties · Self-heating · Industry standard · Compact Modeling Council

1 Introduction

In recent years the success of cellular wireless networks, consumer appliances like digital televisions or digital cameras, mobile computers as well as automotive elec-

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tronics, has resulted in a significant increase of the practical usage of high-voltage MOSFET devices. Furthermore, advances in one-chip process technologies have allowed the integration of high-voltage devices in substantial numbers to produce complex high-voltage circuits on a single chip. Consequently, to enable a more efficient design of such integrated high-voltage circuits, the requirement for accurate compact modeling of high-voltage MOSFETs is increasing.

There are two major types of high-voltage MOSFET structures commonly used by the semiconductor industry, which have to be covered in the compact modeling. The first type is a laterally-diffused asymmetrical structure called commonly LDMOS structure. The second type is a symmetrical structure with extended drift regions at both source and drain, which we distinguish by referring to it as HVMOS because it represents the more generalized case. HiSIM-HV is valid for modeling both structure types, and has been developed as an extension of the surface-potential-based HiSIM (Hiroshima-university STARC IGFET Model) model for conventional bulk MOSFETs [1, 2].

The described practical needs for accurate compact high-voltage MOSFET modeling have also led to an international industrial effort to standardize a compact high-voltage MOSFET model for high-voltage circuit simulation, which is conducted by the Compact Model Council (CMC) [3] and recently resulted in the selection of HiSIM-HV as the international standard compact model for high-voltage MOSFETs. Several versions of the HiSIM-HV standard have been already released by the CMC and this chapter mainly describes the HiSIM-HV102 standard version. An important reason for the selection of HiSIM-HV as the industry-standard model has been the fact that it is the only existing model, which can accurately reproduce the full spectrum of high-voltage-MOSFET behavior, including the effects due to the scaling of device dimensions, with a single global parameter set and without relying on a macro-model concept by adding sub-circuits.

2 Modeling Concepts of HiSIM-HV

The high-voltage MOSFET model HiSIM-HV, reported and described in this chapter, uses a modular concept for its construction. The properties of the MOSFET core in the high-voltage structure are captured by using the advanced bulk-MOSFET model HiSIM (Hiroshima-university STARC IGFET Model), which is the first complete surface-potential-based MOSFET model for circuit simulation, and which avoids introducing any explicit-equation approximations for solving the implicit surface-potential equation of the drift–diffusion theory. The HiSIM core model is then extended and enhanced by various modular additions to construct the HiSIM-HV model. These additional modules mainly have the purpose to capture the specific properties of drift regions added to the MOSFET core for obtaining the high-voltage capabilities and to include the self-heating effect which becomes indispensable due to the increased power dissipation of a high-voltage MOSFET device during its operation.

2.1 Surface-Potential-Based Bulk-MOSFET Core Model

The HiSIM core model implements the drift–diffusion theory, which was originally developed by Pao and Sah [4], and makes this theory available in the form of a compact model for circuit simulation. The most important advantage of the surface-potential-based modeling is a unified description of the device characteristics for all bias conditions with a single although non-explicit equation. The physical reliability of the drift–diffusion theory has been proved by 2D device simulations with channel lengths down to well below 0.1 μm [5], so that it remains valid for the most advanced technologies. To obtain analytical solutions for describing device performances, the charge sheet approximation for the inversion layer with zero thickness has been introduced (for example [6]). Together with the gradual-channel approximation all device characteristics are then described analytically by the channel-surface potentials at the source side (ϕ_{S0}) and at the drain side (ϕ_{SL}) (see Fig. 2.1).

These surface potentials are functions of applied voltages on the four terminals; the gate voltage V_g, the drain voltage V_d, the bulk voltage V_b and the reference potential at the source V_s. The resistance in the contact region causes potential drops and therefore also affects the surface potential values. Since the surface potentials are implicit functions of the applied voltages, model-internal iteration procedures are introduced, but only for calculating the surface potential ϕ_{S0} at the source end and ϕ_{SL} at the end of the inversion channel. These model internal iterations are executed in addition to the global iteration of the circuit simulator. The potential $\phi_S(\Delta L)$, which appears under the saturation condition at the drain end due to the so-called channel-length modulation effect and which represents the potential drop in the pinch-off region (see Fig. 2.3), is calculated from ϕ_{S0}, ϕ_{SL} and V_{ds} involving also a fitting parameter in the respective equation.

The above described modeling concept constitutes the long-channel basis of the HiSIM model, and extensions of the model approximations are then done to capture the properties of advanced MOSFET technologies. All newly appearing phenomena

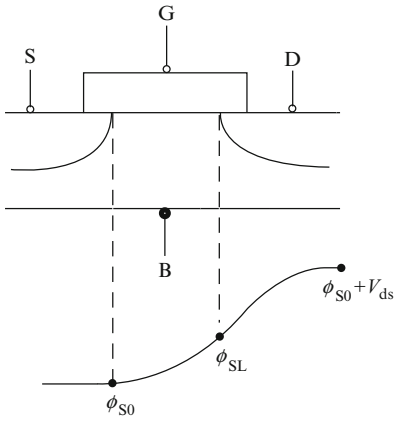

Fig. 2.1 Schematic of the surface potential distribution in the channel

such as short-channel or reverse-short-channel effects are included in the surface potential calculations and cause modifications resulting from the specific features of these advanced technologies [1].

By choosing the iterative solution in the HiSIM core, we preserve the MOSFET physics, which is built into the set of implicit equations resulting from the rigorous application of the drift–diffusion theory. Since an iterative solution is commonly believed to result in an execution-time penalty for the compact model, specific attention is directed towards calculating the surface potentials with enough accuracy under the boundary condition of a small CPU run-time. The number of HiSIM-internal iteration steps could in particular be reduced to an average of two steps in typical circuit-simulation tasks. Furthermore, with advancing scaled-down fabrication technologies, the necessity of including higher-order phenomena like noise effects, non-quasi-static (NQS) effects, or non-homogeneous channel doping into the compact models turned out to be less a burden for HiSIM with its iterative approach than for other non-iterative approaches. Up to now the validity of HiSIM has been tested for channel lengths down to 45 nm with CMOS fabrication technologies using the pocket-implant technology. All theoretical descriptions and equations in the following sections of this chapter are given for the n-channel MOSFET, but they are of course also valid for the p-channel case with the appropriate modifications to account for the exchange of p- and n-doped regions.

2.2 High-Voltage LDMOS Structure

The most important features of LDMOS and HVMOS devices, different from the conventional MOSFET, are originating from the drift region introduced to achieve the sustainability of high voltages. By varying the length and the dopant concentration of this drift region as well as the length of the gate-overlap region, various device types with a variety of operating bias conditions are realized as shown in Fig. 2.2 for the LDMOS structure, which features a drift region only at its drain side. In any of these modified cases, the drift region represent a dynamically varying resistance for the current flow and also induces additional charges, which cause the

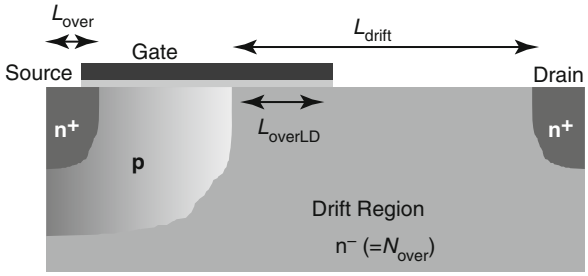

Fig. 2.2 Schematic of the typical LDMOS device structure and the respective structure parameters

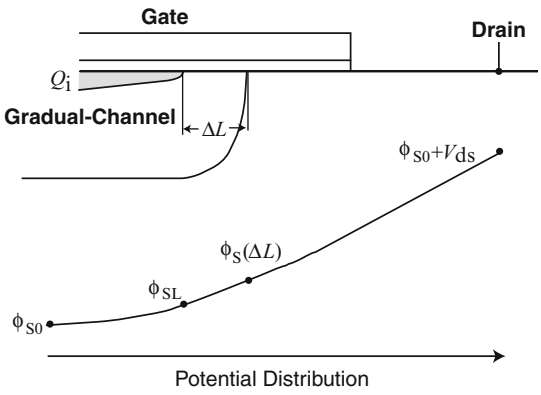

Fig. 2.3 Schematic of the surface potential distribution in the channel at the drain side of the LDMOS device structure

especially unique features of the LDMOS and HVMOS capacitances. Thus accurate modeling of the drift region is the main task for the construction of the HiSIM-HV compact model.

A fortunate feature of the HiSIM compact model, which simplifies the physically consistent capturing of the drift-region properties, is the fact that HiSIM determines the complete potential distribution along the gate from source to drain contact, namely the surface potential at the source side ϕ_{S0}, the surface potential at the pinch-off point ϕ_{SL}, the potential at the channel/drain junction, $\phi_S(\Delta L)$, and the final potential value at the drain contact $\phi_{S0} + V_{ds}$ as shown in simplified from in Fig. 2.3.

For the LDMOS devices it turns out, that the iterative solution for obtaining accurate potentials is the only possible solution to model the specific features of these devices accurately and in a physically consistent way. In particular, if one aims at obtaining a scalable compact high-voltage MOSFET model with respect to gate length, gate width and drift-region length, an iterative solution is unavoidable. The main reason for this comes from the subtle dependence of the potential at the beginning of the drift region, and therefore of the resistance effect in the drift region, on the bias conditions as well as on the detailed geometrical LDMOS structure. The basic modeling method of HiSIM is already suitable for this purpose and can thus be taken over from the HiSIM2 model for advanced MOSFETs [7]. Further equations for capturing the drift-region effects are then included within the framework of HiSIM's modeling method. Since the overlap length is, in comparison to the bulk MOSFET, relatively long for LDMOS devices, accurate surface-potential calculation for this overlap region as a function of applied voltages is also necessary for accurate prediction of the capacitances of the high-voltage LDMOS device.

2.3 General High-Voltage MOSFET Structure

To make the structural definition flexible, the Flag **COSYM** is introduced in HiSIM-HV, as shown in Fig. 2.4. **COSYM** $= 0$ refers to the asymmetrical LDMOS case, where drain-side and source-side parameters are different because the source side

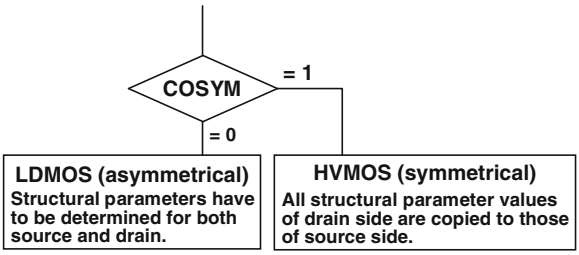

Fig. 2.4 Selection of LDMOS or HVMOS compact-model cases, including respective model parameters, in HiSIM-HV by setting the flag COSYM

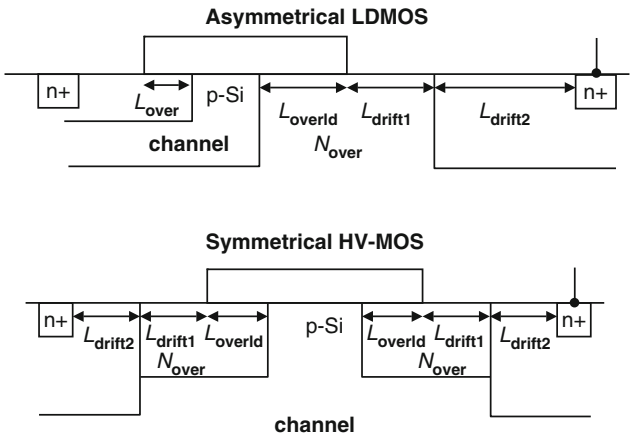

Fig. 2.5 Structure parameters asymmetrical and symmetrical structures selectable in HiSIM-HV

does not include a drift region. **COSYM** = 1 refers to the symmetrical HVMOS case, and all parameter types of the drain side, especially those related to the drift region, have to be determined also for the source side.

HiSIM-HV considers the length of the drift region L_{drift}, the overlap length L_{over}, and the impurity concentration of the drift region N_{over} explicitly. Schematics of the general structures for LDMOS and HVMOS are shown in Fig. 2.5 for the n-channel case. For the LDMOS device, independent structures at the source side and the drain side can be distinguished, due to the fact that the L_{drift} region is not present at the source side. In the HVMOS case, the drift-region-related parameter values for the source side have to be determined, and are copied from the drain-side parameters, automatically. If the drift-region related parameters are not determined, default values are taken.

One most significant feature of the LDMOS/HVMOS devices is that the drain current continues to increase quite steeply even under the saturation condition, which is referred to as the quasi saturation. Other peculiar features are observed in the capacitances, showing strong sharp peaks, which significantly change depending on the structure as well as doping levels. All these phenomena are caused by

Table 2.1 HiSIM-HV model parameters introduced in Section 2 of this chapter

LOVER	Overlap length at source side
LOVERLD	Overlap length at drain, and at source, if **COSYM** = 1
LDRIFT1	Length of lightly doped drift region at drain, and at source, if **COSYM** = 1
LDRIFT2	Length of heavily doped drift region at drain, and at source, if **COSYM** = 1
NOVER	Impurity concentration of **LOVERLD** at drain, and at source, if **COSYM** = 1
VBSMIN	Minimum V_{bs} voltage applied

the highly resistive drift region, enabling the high-voltage application of MOSFETs. The structural parameters of the LDMOS/HVMOS devices are explicitly considered in the resistance modeling, and the resistance effect is considered as a potential drop, which is determined iteratively within HiSIM-HV.

Consequently, the basic modeling concept of LDMOS/HVMOS devices is kept the same as in the HiSIM2 model for the conventional MOSFET. HiSIM-HV also determines the potential distribution between source and drain contacts by solving the Poisson equation iteratively, but includes the resistance effect in the drift region and considers the bias dependence of this resistance.

HiSIM-HV limits the minimum value of the applied bulk voltage V_{bs} to -10.5V. However, this limitation can be changed by adjusting the model parameter **VBSMIN**.

The HiSIM-HV model parameters introduced in Section 2 are summarized in Table 2.1.

3 Implementation of the HiSIM-HV Modeling Concept

As explained in the previous section HiSIM-HV has been developed by building on the bulk-MOSFET model HiSIM2, which is used as the core part. The specific effects of a high-voltage MOSFET, due to the added drift regions for providing the high-voltage blocking and switching capability, are the added in a modular way by either modifying affected modules for certain phenomena already considered in HiSIM2 or by adding new modules.

In this section, the main changes of HiSIM2, which were implemented to develop HiSIM-HV, and which affect the capacitance model, the resistance model, the non-quasi-static (NQS) model, as well as the implementation of the self-heating effect, are described in this section in more detail.

3.1 Capacitances

The capacitance model of HiSIM-HV remains conceptually very similar to that of the bulk-MOSFET model HiSIM2 and mainly covers in addition the increased overlap capacitances including their surface-potential dependence.

3.1.1 Intrinsic Capacitances

The intrinsic capacitances are derivatives of the node charges determined as

$$C_{jk} = \delta \frac{\partial Q_j}{\partial V_k}$$
$$\delta = -1 \quad \text{for} \quad j \neq k$$
$$\delta = 1 \quad \text{for} \quad j = k \tag{2.1}$$

HiSIM-HV uses analytical solutions for all nine independent intrinsic capacitances, derived from the equations for the respective terminal charges [7] as explicit functions of the surface potentials. Therefore, there are no extra model parameters required for the intrinsic capacitances.

The lateral electric field along the channel induces a capacitance C_{Q_y} which significantly affects the gate capacitance in saturation [8]. This induced charge associated with C_{Q_y} is described with the surface potential values as

$$Q_y = \epsilon_{\mathrm{Si}} W_{\mathrm{eff}} \cdot \mathbf{NF} W_{\mathrm{d}} \left(\frac{\phi_{\mathrm{S0}} + V_{\mathrm{ds}} - \phi_{\mathrm{S}}(\Delta L)}{\mathbf{XQY}} \right) + \frac{\mathbf{XQY1}}{L_{\mathrm{gate}}^{\mathbf{XQY2}}} V_{\mathrm{bs}} \tag{2.2}$$

introducing **XQY**, a parameter determining the maximum field at the channel/drain junction independent of L_{gate}. For $\mathbf{XQY} = 0$ the charge Q_{y} is fixed to zero. To compensate the enhanced short-channel effect, determined by the current characteristics, two model parameters **XQY1** and **XQY2** are introduced. Under the saturation condition, C_{Q_y} together with the overlap capacitance dominates the gate-drain capacitance C_{gd}. This effect is more visibly observed as the gate-length reduces. Therefore, in the C_{gd} modeling, C_{Q_y} is added to the conventional components as depicted in Fig. 2.6 and replaces the so-called inner-fringing field effects which are conventionally applied [9]. To activate Q_{y} the model parameter **CLM1** must be smaller than unity.

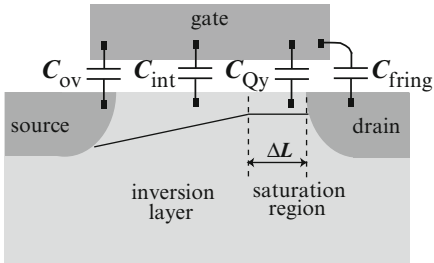

Fig. 2.6 Modeling of the gate-drain capacitance with C_{Q_y} added to the conventional capacitance components

3.1.2 Overlap Capacitances

The overlap charge at the drain side is written as

$$\frac{Q_{\text{god}}}{W_{\text{eff}} \cdot \mathbf{NF} \cdot C_{\text{ox}}} = \int_0^{\mathbf{LOVERLD}} (V_{\text{gs}} - \phi_{\text{S}}) dy \tag{2.3}$$

Thus the surface-potential distribution along the overlap region determines the charge and the capacitance. The potential increase of $\phi_{\text{S}}(y)$ from $\phi_{\text{S}}(\Delta L)$ to $\phi_{\text{S0}} + V_{\text{ds}}$ is modeled by considering the lateral impurity-profile gradient of the drain contact [10]. However, the influence of the gradient is often negligible, and only the surface-potential change as a function of the applied voltage is considered here.

The overlap capacitance includes three model options as summarized in Fig. 2.7. Besides the constant overlap-capacitance option, two bias dependent models are provided: One considers the surface potential change as a function of V_{gs} and the other calculates the overlap capacitance with a simplified V_{gs} dependence.

(i) Surface-Potential-Based Model

The surface-potential-based concept for the overlap capacitance is described here for the drain side. For the source side the same calculation is performed with $V_{\text{ds}} = 0$. The calculation of the surface potential in the drain contact region is done for all possible conditions, from the inversion condition to the accumulation condition. The surface potential ϕ_{S} is calculated in the same manner as in the channel region, and only the polarity is inverted in comparison to the channel. The final overlap charge equation is written with the calculated ϕ_{S}

(a) under the depletion and the accumulation conditions

$$Q_{\text{over}} = W_{\text{eff}} \cdot \mathbf{NF} \cdot \mathbf{LOVERLD} \cdot \left(\sqrt{\frac{2\epsilon_{\text{Si}} q \mathbf{NOVER}}{\beta}} \sqrt{\beta(\phi_{\text{S}} + V_{\text{ds}}) - 1} \right) \tag{2.4}$$

(b) under the inversion condition

$$Q_{\text{over}} = W_{\text{eff}} \cdot \mathbf{NF} \cdot \mathbf{LOVERLD} \cdot C_{\text{ox}} \left[(V_{\text{gs}} - \mathbf{VFBOVER} - \phi_{\text{S}}) \right] \tag{2.5}$$

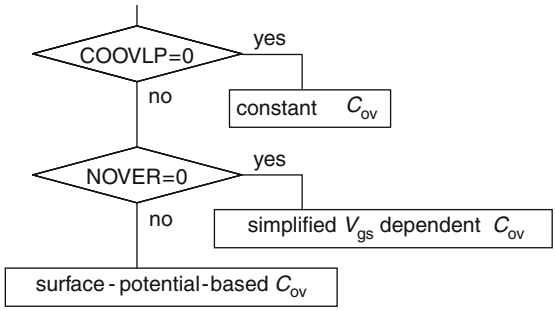

Fig. 2.7 Summary of the HiSIM-HV model options for the overlap capacitance

where **LOVERLD** is the length of the overlap region of the gate over the drain, **NOVER** is the impurity concentration in the drain contact region, and **VFBOVER** is the flat-band voltage in the overlap region. This model is selected, if **NOVER** is not equal to 0.

A smoothing function is introduced with a model parameter **QOVSM** to achieve a smooth transition between the depletion region and the inversion region of the overlap charge.

(ii) Simplified Bias-Dependent Model

If **LOVER** > 0 and the flag **COOVLP** $= 1$, the overlap gate charge at the source side is modeled as

$$\begin{aligned}\frac{Q_{\mathrm{gos}}}{W_{\mathrm{eff}} \cdot \mathbf{NF} \cdot C_{\mathrm{ox}}} &= V_{\mathrm{gs}} \cdot \mathbf{LOVER} \\ &\quad - \mathbf{OVSLP} \cdot (1.2 - (\phi_{\mathrm{S0}} - V_{\mathrm{bs}})) \\ &\quad \cdot (\mathbf{OVMAG} + V_{\mathrm{gs}})\end{aligned} \tag{2.6}$$

If **NOVER** is equal to 0, the overlap charge at the drain is also calculated with the same type of simplified equation as

$$\begin{aligned}\frac{Q_{\mathrm{god}}}{W_{\mathrm{eff}} \cdot \mathbf{NF} \cdot C_{\mathrm{ox}}} &= (V_{\mathrm{gs}} - V_{\mathrm{ds}}) \cdot \mathbf{LOVERLD} \\ &\quad - \mathbf{OVSLP} \cdot (1.2 - (\phi_{\mathrm{SL}} - V_{\mathrm{bs}})) \\ &\quad \times (\mathbf{OVMAG} + V_{\mathrm{gs}})\end{aligned} \tag{2.7}$$

The overlap capacitance at the source side is calculated by differentiating Q_{gos}. Whereas the overlap capacitances at the drain side is calculated by differentiating either Q_{god} or Q_{over} of the overlap charge equations.

In summary these bias-dependent overlap-capacitance models can be selected using the model flag **COOVLP** $= 1$, and require **OVSLP** and **OVMAG** or **NOVER** and **VFBOVER** in addition as model parameters. For further model adjustments **LOVER** (overlap length) is used.

The default overlap capacitance flag (**COOVLP** $=$ 0) calculates bias-independent drain and source overlap capacitances. User-defined values can be specified using the input parameters **CGDO** and **CGSO**. If these values are not specified, the overlap capacitances are calculated using

$$C_{\mathrm{ov}} = -\frac{\epsilon_{\mathrm{ox}}}{\mathbf{TOX}} \mathbf{LOVER} \cdot W_{\mathrm{eff}} \cdot \mathbf{NF} \tag{2.8}$$

The gate-to-bulk overlap capacitance $C_{\mathrm{gbo\_loc}}$ is calculated only with a user-defined value **CGBO** using

$$C_{\mathrm{gbo\_loc}} = -\mathbf{CGBO} \cdot L_{\mathrm{gate}} \tag{2.9}$$

independent of the model flag **COOVLP**.

Table 2.2 HiSIM-HV model parameters introduced in subsection 3.1 of this chapter

XQY	Distance from drain junction to maximum electric field point
***XQY1**	V_{bs} dependence of Q_y
***XQY2**	L_{gate} dependence of Q_y
VFBOVER	Flat-band voltage in overlap region
***QOVSM**	Smoothing Q_{over} at depletion/inversion transition
OVSLP	Coefficient for overlap capacitance
OVMAG	Coefficient for overlap capacitance
CGSO	Gate-to-source overlap capacitance
CGDO	Gate-to-drain overlap capacitance
CGBO	Gate-to-bulk overlap capacitance
TPOLY	Height of the gate poly-Si

3.1.3 Extrinsic Capacitances

The outer fringing capacitance is modeled as [11]

$$C_f = \frac{\epsilon_{ox}}{\pi/2} W_{gate} \cdot \mathbf{NF} \cdot \ln\left(1 + \frac{\mathbf{TPOLY}}{T_{ox}}\right) \tag{2.10}$$

where **TPOLY** is the gate-poly thickness. This outer fringing capacitance is bias independent.

The HiSIM-HV model parameters introduced in Section 3.1 are summarized in Table 2.2.

3.2 Resistances of the High-Voltage MOSFET

This section describes the equations of the resistance model for the LDMOS case. In the symmetrical HVMOS case, the resistance at the source side is modeled with the same equations as for the drain side in the LDMOS case, but without the V_{ds} dependence.

The source and the drain resistances R_s and R_d are considered by voltage drops across each of the resistances as:

$$V_{gs,eff} = V_{gs} - I_{ds} \cdot R_s \tag{2.11}$$

$$V_{ds,eff} = V_{ds} - I_{ds} \cdot (R_s + R_{drift}) \tag{2.12}$$

$$V_{bs,eff} = V_{bs} - I_{ds} \cdot R_s \tag{2.13}$$

where

$$R_s = \frac{\mathbf{RS}}{W_{eff}} + \mathbf{NRS} \cdot \mathbf{RSH} \tag{2.14}$$

$$R_{\mathrm{drift}} = (R_{\mathrm{d}} + V_{\mathrm{ds}} \cdot R_{\mathrm{DVD}}) \left(1 + \mathbf{RDVG11} - \frac{\mathbf{RDVG11}}{\mathbf{RDVG12}} \cdot V_{\mathrm{gs}}\right) \times (1 - V_{\mathrm{bs}} \cdot \mathbf{RDVB}) \tag{2.15}$$

and

$$R_{\mathrm{d}} = \frac{R_{\mathrm{d0}}}{W_{\mathrm{eff}}} \left(1 + \frac{\mathbf{RDS}}{(W_{\mathrm{gate}} \cdot 10^4 \times L_{\mathrm{gate}} \cdot 10^4)^{\mathbf{RDSP}}}\right) + \mathbf{RSH} \cdot \mathbf{NRD} \tag{2.16}$$

$$R_{\mathrm{d0}} = \left(\mathbf{RD} + R_{\mathrm{d0,temp}}\right) f_1 \cdot f_2 \tag{2.17}$$

$$R_{\mathrm{DVD}} = \frac{\mathbf{RDVD} + R_{\mathrm{dvd,temp}}}{W_{\mathrm{eff}}} \cdot \exp\left(-\mathbf{RDVDL} \times (L_{\mathrm{gate}} \cdot 10^4)^{\mathbf{RDVDLP}}\right) \cdot \left(1 + \frac{\mathbf{RDVDS}}{(W_{\mathrm{gate}} \cdot 10^4 \times L_{\mathrm{gate}} \cdot 10^4)^{\mathbf{RDVDSP}}}\right) \cdot f_1 \cdot f_3 \tag{2.18}$$

$$f_1(L_{\mathrm{drift1}}) = \frac{\mathbf{LDRIFT1}}{1\mu\mathrm{m}} \cdot \mathbf{RDSLP1} + \mathbf{RDICT1} \tag{2.19}$$

$$f_2(L_{\mathrm{drift2}}) = \frac{\mathbf{LDRIFT2}}{1\mu\mathrm{m}} \cdot \mathbf{RDSLP2} + \mathbf{RDICT2} \tag{2.20}$$

$$f_3(L_{\mathrm{over}}) = 1 + \mathbf{RDOV11} - \frac{\mathbf{RDOV11}}{\mathbf{RDOV12}} \cdot \frac{\mathbf{LOVERLD}}{1\mu\mathrm{m}} \tag{2.21}$$

NRS and **NRD** are instance parameters describing the number of squares resulting from the geometrical layout of the source and the drain diffusions, while **RSH** is the sheet resistance of one square of diffusion area. In each of the Eqs. 2.14 and 2.16, the first term of the right hand side considers the resistance of the LDD region and the drift region, and the second term takes account of the diffusion region, which is layout dependent. **LDRIFT1** and **LDRIFT2** are model parameters denoting the length of different parts of the drift region (see Fig. 2.5). The source resistance in the LDMOS case, for which the above equations are valid, does not include a drift region and has therefore no drift length parameters.

The voltage drops at the source and the drain resistances are calculated iteratively within HiSIM-HV for given terminal voltages to keep consistency among all device performances. However, R_{s} and R_{drift} can also be treated as extrinsic resistances, and can be included in an equivalent circuit applied externally. Consequently, the parasitic source and drain resistances, R_{s} and R_{drift}, can be taken account of in HiSIM-HV by two optional approaches. The first approach is to include them as external resistances, so that the circuit simulator generates nodes and finds the solution with the source/drain resistances iteratively (Flag: **CORSRD** $= -1$). The

second approach is to include them as internal resistances of HiSIM-HV, so that HiSIM-HV solves iteratively for the now internal nodes (Flag: **CORSRD** $= 1$). The Flag **CORSRD** is provided for the selection of one of the altogether four possible approaches, namely **CORSRD** $= 0, 1, 2, -1$ meaning "no resistance", "internal", "analytical", and "external" source/drain resistances, respectively. The selection procedure of the different options by the Flag **CORSRD** is summarized in the flow-diagram of Fig. 2.8.

A further flag option **CORSRD** $= 2$ was originally introduced to avoid simulation time penalties by providing the possibility of an analytical description of the resistance effect as

$$I_{\mathrm{ds}} = \frac{I_{\mathrm{ds0}}}{1 + I_{\mathrm{ds0}} \frac{R_{\mathrm{d}}}{V_{\mathrm{ds}}}} \tag{2.22}$$

where I_{ds0} is the drain current without the resistance effect and where R'_{d} takes account of the resistance effect in the following simplified form.

$$R_{\mathrm{d}} = \frac{1}{W_{\mathrm{eff}}} \left(R'_{\mathrm{d}} \cdot V_{\mathrm{ds}}^{\mathbf{RD21}} + V_{\mathrm{bs}} \cdot \mathbf{RD22} \right) \tag{2.23}$$

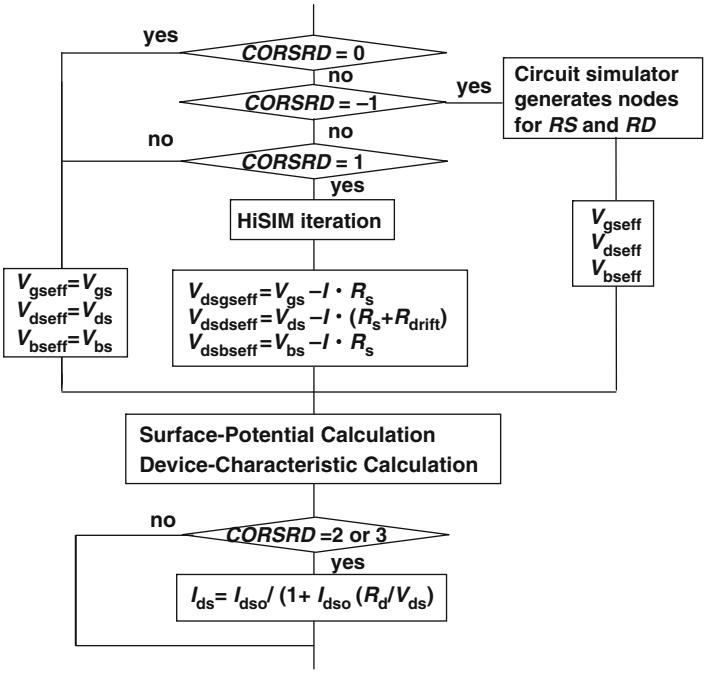

Fig. 2.8 Model options provided in HiSIM-HV for the resistance models at source and drain side, and their selection by the Flag **CORSRD**

The magnitude determination of the resistance R'_{d} includes equations with parameters introduced to consider the resistance reduction due to the current flow in the drift region. Further model parameters have the purpose to include the size dependences of the resistance as

$$R'_{\mathrm{d}} = RD23' \tag{2.24}$$

where

$$RD23' = \mathbf{RD23} \cdot \exp\left(-\mathbf{RD23L} \times (L_{\mathrm{gate}} \cdot 10^4)^{\mathbf{RD23LP}}\right) \cdot \left(1 + \frac{\mathbf{RD23S}}{(W_{\mathrm{gate}} \cdot 10^4 \times L_{\mathrm{gate}} \cdot 10^4)^{\mathbf{RD23SP}}}\right) \tag{2.25}$$

For large V_{gs}, it happens that the resistance effect becomes too strong with the global parameter set fitted to the whole V_{gs} regime. For covering also this effect for large V_{gs} in the global parameter set, the V_{gs} dependence has to be included by the introduction of further model parameters. In HiSIM-HV the equation for R'_{d} is therefore modified to the form

$$R'_{\mathrm{d}} = \mathbf{RD24}\left(V_{\mathrm{gs}} - \mathbf{RD25}\right) \tag{2.26}$$

where the modification of R'_{d} itself is restricted with two boundaries, namely with a lower boundary defined to be $RD23'$ and with an upper boundary given by $RD23'$ multiplied with $(1 + \mathbf{RD20})$ as

$$RD23' \leq R'_{\mathrm{d}} \leq RD23'(1 + \mathbf{RD20}) \tag{2.27}$$

If $\mathbf{RD20} = 0$, R'_{d} reduces to $RD23'$, meaning that the R'_{d} modification is deselected. For the LDMOS case **RD21** (see Eq. 2.23) is normally fixed to be unity. Here it should to be noticed that the described resistance affects only the drain current, and that the LDMOS capacitances are not influenced.

The accurate approach to consider the resistance effect is to treat it with an internal node by selecting ($\mathbf{CORSRD} = 1$). However, in cases where it is necessary, both types of resistance models (internal-node approach and analytical approach) can be applied with $\mathbf{CORSRD} = 3$ simultaneously.

The approach with external source/drain resistances ($\mathbf{CORSRD} = -1$) leads to shorter simulation times for circuits with small to medium transistor numbers, while the approach with internal source/drain resistances leads to shorter simulation times for circuits with very large transistor numbers. The transistor number, for which both approaches result in approximately equal simulation times (the switching point for the choice between the two approximations) is normally between 10,000 and 50,000 transistors.

The gate resistance becomes larger when the gate width increases, and therefore the gate-resistance effect has to be included in the compact model for correctly simulating the circuit properties at sufficiently high operating frequencies, a condition

which applies for the practical operation frequencies of many RF circuits. The approach for the gate-resistance calculation applied in HiSIM-HV is similar to that used in BSIM4 [12] and is described by the equation

$$R_{\mathrm{g}} = \frac{\mathbf{RSHG} \cdot \left(\mathbf{XGW} + \frac{W_{\mathrm{eff}}}{3 \cdot \mathbf{NGCON}}\right)}{\mathbf{NGCON} \cdot (L_{\mathrm{drawn}} - \mathbf{XGL}) \cdot \mathbf{NF}} \tag{2.28}$$

where the parameter **RSHG** is the gate's sheet resistance, while the other parameters are instance parameters dependent on the layout. The flag **CORG** is provided for selecting the inclusion of the gate resistance. The flag settings **CORG** $= 0, 1$ mean "no", "external" gate resistance, respectively.

Model parameters for the same substrate resistance network as applied in BSIM4 (**RBPB**, **RBPD**, **RBPS**, **RBDB**, **RBSB**) are additionally included in the model parameter list, and these parameters are also treated as instance parameters.

The HiSIM-HV model parameters introduced in Section 3.2 are summarized in Table 2.3.

3.3 Non-Quasi-Static (NQS) Model

Carriers in the channel and the drift region take time to build-up as opposed to the quasi-static (QS) approximation. In HiSIM-HV, the carrier formation within the device is modeled by considering the carrier-delay mechanisms as described in the following subsections.

3.3.1 Carrier Formation

To consider the non-quasi-static (NQS) phenomenon of carrier delay in HiSIM-HV, the carrier formation is modeled as [13–15]

$$q(t_{\mathrm{i}}) = \frac{q(t_{\mathrm{i}-1}) + \frac{\Delta t}{\tau} Q(t_{\mathrm{i}})}{1 + \frac{\Delta t}{\tau}} \tag{2.29}$$

where $q(t_{\mathrm{i}})$ and $Q(t_{\mathrm{i}})$ represent the non-quasi-static (NQS) and the quasi-static (QS) carrier density at time t_{i}, respectively, while $\Delta t = t_{\mathrm{i}} - t_{\mathrm{i}-1}$ is the time interval parameter between two sequential time points in the circuit simulation. Equation 2.29 implies that the formation of carriers under the NQS approximation is always delayed in comparison to the QS approximation, and therefore captures the basic physical origin of the NQS effect. The delay in changes of the charge density is determined by the carrier transit delay τ and the time interval Δt used in the circuit simulation.

Table 2.3 HiSIM-HV model parameters introduced in Section 3.2 of this chapter

RS	Source-contact resistance of LDD region
RD	Drain-contact resistance of LDD region
RSH	Source/drain sheet resistance of diffusion region
RSHG	Gate sheet resistance
RBPB	Substrate resistance network
RBPD	Substrate resistance network
RBPS	Substrate resistance network
RBDB	Substrate resistance network
RBSB	Substrate resistance network
#NRS	Number of source squares
#NRD	Number of drain squares
#XGW	Distance from the gate contact to the channel edge
#XGL	Offset of the gate length
#NF	Number of fingers
#NGCON	Number of gate contacts
***RDVG11**	V_{gs} dependence of **RD** for **CORSRD** $= 1, 3$
***RDVG12**	V_{gs} dependence of **RD** for **CORSRD** $= 1, 3$
RDVD	V_{ds} dependence of **RD** for **CORSRD** $= 1, 3$
RDVB	V_{bs} dependence of **RD** for **CORSRD** $= 1, 3$
***RDS**	Small size dependence of **RD** for **CORSRD** $= 1, 3$
***RDSP**	Small size dependence of **RD** for **CORSRD** $= 1, 3$
***RDVDL**	L_{gate} dependence of **RD** for **CORSRD** $= 1, 3$
***RDVDLP**	L_{gate} dependence of **RD** for **CORSRD** $= 1, 3$
***RDVDS**	Small size dependence of **RD** for **CORSRD** $= 1, 3$
***RDVDSP**	Small size dependence of **RD** for **CORSRD** $= 1, 3$
RDOV11	L_{over} dependence of resistance for **CORSRD** $= 1, 3$
RDOV12	L_{over} dependence of resistance for **CORSRD** $= 1, 3$
RDSLP1	L_{drift1} dependence of resistances for **CORSRD** $= 1, 3$
RDICT1	L_{drift1} dependence of resistances for **CORSRD** $= 1, 3$
RDSLP2	L_{drift2} dependence of resistances for **CORSRD** $= 1, 3$
RDICT2	L_{drift2} dependence of resistances for **CORSRD** $= 1, 3$
RD20	**RD23** boundary for **CORSRD** $= 2, 3$
RD21	V_{ds} dependence of **RD** for **CORSRD** $= 2, 3$
RD22	V_{bs} dependence of **RD** for **CORSRD** $= 2, 3$
RD23	Modification of **RD** for **CORSRD** $= 2, 3$
***RD23L**	L_{gate} dependence of **RD21** boundary for **CORSRD** $= 2, 3$
***RD23LP**	L_{gate} dependence of **RD21** boundary for **CORSRD** $= 2, 3$
***RD23S**	Small size dependence of **RD21** for **CORSRD** $= 2, 3$
***RD23SP**	Small size dependence of **RD21** for **CORSRD** $= 2, 3$
***RD24**	V_{gs} dependence of **RD** for **CORSRD** $= 2, 3$
***RD25**	V_{gs} dependence of **RD** for **CORSRD** $= 2, 3$

#indicates instance parameters and * indicates minor parameters

3.3.2 Delay Mechanisms

Up to the weak inversion regime, the carriers diffuse into the channel and the transit delay can be approximated by

$$\tau_{\mathrm{diff}} = \mathbf{DLY1} \tag{2.30}$$

In the strong inversion regime, there is already conduction due to field-driven carriers which dominates the carrier movement. The transit delay due to this flow of conductive carriers is

$$\tau_{\mathrm{cond}} = \mathbf{DLY2} \cdot \frac{Q_{\mathrm{i}}}{I_{\mathrm{ds}}} \tag{2.31}$$

where **DLY2** is a constant coefficient. These two delay mechanisms (diffusion and conduction) are combined in HiSIM-HV by using the Matthiessen rule

$$\frac{1}{\tau} = \frac{1}{\tau_{\mathrm{diff}}} + \frac{1}{\tau_{\mathrm{cond}}} \tag{2.32}$$

Carrier delay mechanisms in a switch-on operation of the MOSFET part with a gate-voltage rise time t_{r} of 20ps are illustrated in Fig. 2.9.

Applying the same approach of a carrier transit delay also for the formation of bulk carriers, leads to the approximation of the bulk carrier delay as an RC delay in the form

$$\tau_{\mathrm{B}} = \mathbf{DLY3} \cdot C_{\mathrm{ox}} \tag{2.33}$$

where **DLY3** is a constant coefficient and C_{ox} is the oxide capacitance of the gate.

3.3.3 Time-Domain Analysis

The total drain/source/bulk terminal currents in the MOSFET part are derived from the superposition of the transport current and the charging current. The transport

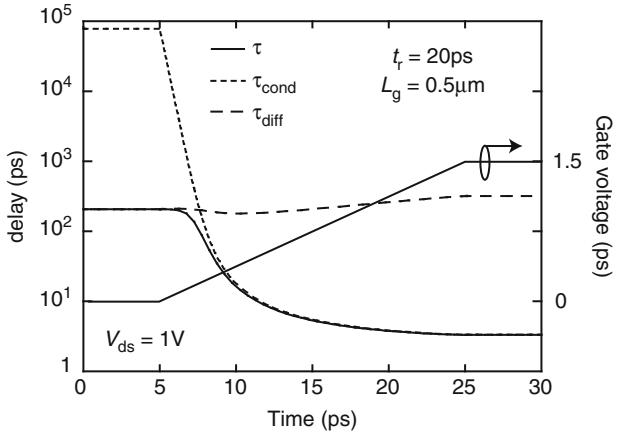

Fig. 2.9 Example of the dynamically calculated transit delay times, as incorporated in the NQS model for the MOSFET part of HiSIM-HV, in a switch-on simulation

current is a function of the instantaneous terminal voltages and is approximated by the steady-state solution. The source/drain/bulk charging currents are the time derivatives of the associated non-quasi-static (NQS) charges, q_S, q_D, and q_B, respectively.

For high-voltage LDMOS/HVMOS devices, the carrier transit delay τ in the drift regions becomes additionally very important, because the considerable length of these drift regions contributes a strong NQS effect during their charging and discharging. The compact modeling of the NQS effect due to the drift region is done in a similar way as for the channel region using the following equation.

$$\tau_{LD} = \frac{(\mathbf{LOVERLD} + \mathbf{LDRIFT1} + \mathbf{LDRIFT2})^2}{\mathbf{DLYDFT} \cdot (V_{ds} - \phi_{SL} + \phi_{S0})} \tag{2.34}$$

The formation delay of the equilibrium charge density for the accumulation condition is also modeled in HiSIM-HV as

$$\tau_{LD} = \mathbf{DLYOV} \cdot C_{ox0} \tag{2.35}$$

The HiSIM-HV model parameters described in Section 3.3 are summarized in Table 2.4.

3.4 Modeling of the Self-Heating Effect

The self-heating effect is modeled in HiSIM-HV according to a conventional approach with the thermal network shown in Fig. 2.10. The self-heating extension is completely integrated in the HiSIM-HV model equations and does therefore not require a subcircuit approach. The flag **COSELFHEAT** must be set equal to 1 and **RTH0** must not be set equal to 0 to activate the self-heating model. The temperature node is automatically generated in the circuit simulator for each device as it is also done with other bias nodes. First, the model core (HiSIM.eval) is called to evaluate device characteristics without heating. Then, the temperature is updated considering the self-heating effect by creating the temperature node. The model core is then

Table 2.4 HiSIM-HV model parameters introduced in Section 3.3 of this chapter

DLY1	Coefficient for delay due to diffusion of carriers
DLY2	Coefficient for delay due to conduction of carriers
DLY3	Coefficient for RC delay of bulk carriers
LOVERLD	Length of the gate-overlap part of the drift region
LDRIFT1	Length of the first lower-doped part of the drift region
LDRIFT2	Length of the second higher-doped part of the drift region
DLYDFT	Coefficient for carrier transit delay
DLYOV	Coefficient for RC delay of carriers for the accumulation condition

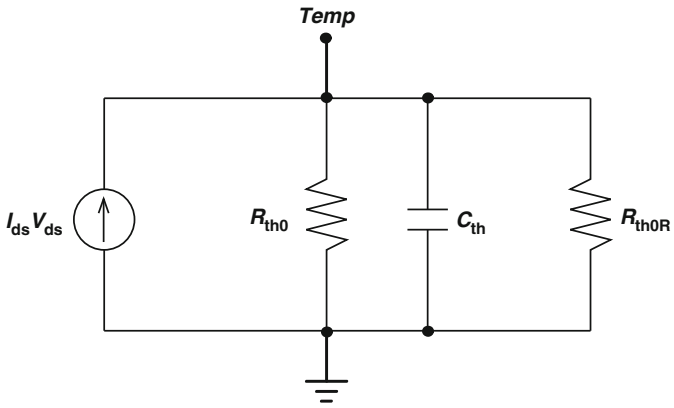

Fig. 2.10 Thermal Network applied for the self-heating effect

called again to update the device characteristics with the calculated temperature T. Under the DC condition the temperature increase is calculated analytically as

$$T = T + R_{\mathrm{TH}} \cdot I_{\mathrm{ds}} \cdot V_{\mathrm{ds}} \tag{2.36}$$

The model parameter **RTH0** is thermal-resistance related and is fitted to measured DC data, while the model parameter **CTH0** is thermal-capacitance related and is introduced for fitting the thermal behavior under AC operation. Furthermore, as the self-heating strongly depends on the width of the LDMOS/HVMOS device and on the number of used fingers **NF** in the layout, these effects have to be included in the compact modeling and result in the formulation of the HiSIM-HV equations for thermal resistance and thermal capacitance as

$$R_{\mathrm{th}} = \frac{\mathbf{RTH0}}{W_{\mathrm{eff}}} \cdot \left(\frac{1}{\mathbf{NF}^{\mathbf{RTH0NF}}} \right) \left(1 + \frac{\mathbf{RTH0W}}{(W_{\mathrm{gate}} \cdot 10^4)^{\mathbf{RTH0WP}}} \right) \tag{2.37}$$

$$C_{\mathrm{th}} = \mathbf{CTH0} \cdot W_{\mathrm{eff}} \tag{2.38}$$

An additional model parameter **RTH0R** is introduced as

$$R_{\mathrm{TH0W}} = \frac{\mathbf{RTH0R}}{\mathbf{TEMP}^3} \tag{2.39}$$

to improve the modeling of the thermal dissipation.

The HiSIM-HV model parameters introduced in Section 3.4 are summarized in Table 2.5.

Table 2.5 HiSIM-HV model parameters introduced in Section 3.4 of this chapter

RTH0	Thermal resistance
CTH0	Thermal capacitance
RTH0W	Width dependence of thermal resistance
RTH0WP	Width dependence of thermal resistance
RTH0NF	Number of finger dependence of thermal resistance
RTH0R	Thermal dissipation

4 Overview of the Parameter-Extraction Procedure

The parameter extraction has to cover the parameters specific for the MOSFET part, which is analogous to the bulk-MOSFET model HiSIM2, and the parameters specific for the high-voltage part of the LDMOS/HVMOS device. Model parameters categorized as group (1), i.e. conventional MOSFET related parameters, are extracted first and parameters characterized as group (2), i.e. LDMOS/HVMOS specific parameters, are extracted afterwards. In this section we discuss the main points of the HiSIM-HV parameter extraction and point out the differences in comparison to the normal MOSFET-parameter extraction.

4.1 Conventional MOSFET Part

In the bulk-MOSFET model HiSIM, device characteristics are strongly dependent on the basic device parameter values, such as the impurity concentration or the oxide thickness. Therefore, the parameter-value extraction has to be repeated with measured characteristics of different devices in a specific sequence until extracted parameter values reproduce all device characteristics consistently and reliably. To achieve reliable extraction results, it is recommended to start with initial parameter values according to the recommendations listed in the Table 2.6. Since some of the model parameters such as T_{ox} are difficult to extract unambiguously with the correct physical values, their determination is recommended directly by dedicated measurements of the MOSFET-device part. Threshold voltage measurements as a function of gate length allow the derivation of a rough extraction for the model parameters referred to as “basic device parameters”. The parameters identified with the symbol “*” in the model-parameter table are initially fixed to zero and only adjusted in the final stage of the extraction, if necessary.

The sequence of the MOSFET-channel-size selection for the parameter-extraction procedure is recommended in four steps:

1. Long-Channel Devices
2. Short-Channel Devices
3. Long-Narrow Devices
4. Short-Narrow Devices

Table 2.6 Recommendation for initial parameter settings at the beginning of the extraction procedure

Determined by dedicated measurements (not changed during extraction procedure)	Default values used (see [7]) initially for parameter groups listed below
TOX	Basic device parameters (not listed on left side)
	Gate leakage
	GIDL
	Source/bulk and drain/bulk diodes
	Noise
	Subthreshold swing
	Non-quasi-static model
	Overlap capacitances

Prior to the detailed extraction, a rough extraction with measured $V_{\text{th}} - L_{\text{gate}}$ characteristics is recommended to get a rough idea about the basic-parameter values. These basic parameters are usually important because they give a strong influence on the accuracy and physical correctness of the total parameter extraction. The parameter extraction procedure of the conventional MOSFET part is summarized in the following Table 2.7.

4.2 LDMOS/HVMOS Specific Part

The LDMOS/HVMOS specific model parameters (group (2) parameters) are extracted, as already mentioned, after the extraction of the intrinsic MOSFET-part parameters (group (1) parameters) of the high-voltage device. According to this recommended extraction procedure, namely to perform first group (1) and then group (2) parameters, the parameter extraction is done in the following sequence:

1. Rough extraction of the MOSFET parameters with measured $V_{\text{th}} - L_{\text{gate}}$
2. Fine extraction with measured subthreshold data for $I_{\text{ds}} - V_{\text{gs}}$
3. Extraction of mobility parameters with $I_{\text{ds}} - V_{\text{gs}}$ and $I_{\text{ds}} - V_{\text{ds}}$
4. Extraction of resistance parameters with $I_{\text{ds}} - V_{\text{gs}}$ and $I_{\text{ds}} - V_{\text{ds}}$
5. Fine extraction of resistance parameters with channel-conductance and transconductance
6. Capacitance extraction

Agreement of the extraction results with measurements after the 3rd step is normally not sufficient, especially in the high V_{gs} region and in the low V_{ds} region. The 4th step for resistance extraction is therefore focused on the measurement regions where the quasi-saturation effect of the LDMOS/HVMOS device becomes obvious. It is recommended to repeat the extraction steps from 3 to 5 because this repetition leads to better fitting results in most practical cases. The initial extraction steps 1 to 3 are basically the same as in the conventional extraction procedure for the bulk MOSFET.

Table 2.7 Summary of the seven steps of the parameter-extraction procedure for the bulk-MOSFET model HiSIM

Step 1: Initial preparation and rough extraction		
1-1.	Initialize all parameters to their default values	
1-2.	Use the measured gate-oxide thickness for TOX	TOX
1-3.	Rough extraction with $V_{\rm th}$-dependence on $L_{\rm gate}$ $[V_{\rm th} - V_{\rm gs}]$	**NSUBC**, **VFB**, **SC1**, **SC2** **SC3**, **NSUBP**, **LP**, **SCP1** **SCP2**, **SCP3** **NPEXT**, **LPEXT**
1-4.	Quantum and poly-depletion effects $[C_{\rm gg} - V_{\rm gs}]$	**QME1**, **QME2**, **QME3** **PGD1**, **PGD2**
Step 2: Extraction with long and wide transistors		
2-1.	Fitting of sub-threshold characteristics $[I_{\rm ds} - V_{\rm gs}]$	**NSUBC**, **VFB**, **MUECB0** **MUECB1**
2-2.	Determination of mobility parameters for low $V_{\rm ds}$ $[I_{\rm ds} - V_{\rm gs}]$	**MUEPH0**, **MUEPH1** **MUESR0**, **MUESR1**
2-3.	Determination of mobility parameters for high $V_{\rm ds}$ $[I_{\rm ds} - V_{\rm gs}]$	**NINVPH**, **NINVSR** **NDEP**
Step 3: Extraction with medium/short length and large width transistors		
3-1.	Pocket-parameter extraction with medium length transistors $[I_{\rm ds} - V_{\rm gs}]$	**NSUBP**, **LP** **SCP1**, **SCP2**, **SCP3** **NPEXT**, **LPEXT**
3-2.	Short-channel-parameter extraction with short-length transistors $[V_{\rm th} - L_{\rm gate}]$	**SC1**, **SC2**, **SC3** **PARL2**, **XLD**
3-3.	Mobility-parameter refinement for low $V_{\rm d}$ $[I_{\rm ds} - V_{\rm gs}]$	**MUEPHL**, **MUEPLP** **MUESRL**, **MUESLP**
3-4.	Velocity parameter extraction for high $V_{\rm d}$ $[I_{\rm ds} - V_{\rm gs}]$	**VMAX**, **VOVER**, **VOVERP**
3-5.	Parameters for channel-length modulation $[I_{\rm ds} - V_{\rm ds}]$	**CLM1**, **CLM2**, **CLM3**
3-6.	Source/drain resistances $[I_{\rm ds} - V_{\rm ds}]$	**RS**, **RD**, **RSH**, **NRS**, **NRD**
Step 4: Extraction of the width dependencies for long transistors		
4-1.	Fitting of sub-threshold width dependencies $[I_{\rm ds} - V_{\rm gs}]$	**NSUBC**, **NSUBCW**, **NSUBCWP** **WFC**, **XWD**, **WVTH0**
4-2.	Fitting of mobility width dependencies $[I_{\rm ds} - V_{\rm gs}]$	**MUEPHW**, **MUEPWP** **MUESRW**, **MUESWP**
Step 5: Extraction of the width dependencies for short transistors		
5-1.	Fitting of sub-threshold dependencies $[I_{\rm ds} - V_{\rm gs}]$	**NSUBP0**, **NSUBWP**
Step 6: Extraction of small-geometry effects		
6-1.	Effective channel-length corrections	**WL2**, **WL2P**
6-2.	Mobility and velocity $[I_{\rm ds} - V_{\rm ds}]$	**MUEPHS**, **MUEPSP** **VOVERS**, **VOVERSP**
Step 7: Extraction of temperature dependence with long-channel transistors		
7-1.	Sub-threshold dependencies $[I_{\rm ds} - V_{\rm gs}]$	**BGTMP1**, **BGTMP2** **EG0**
7-2.	Mobility and maximum carrier-velocity dependencies $[I_{\rm ds} - V_{\rm gs}]$	**MUETMP**, **VTMP**

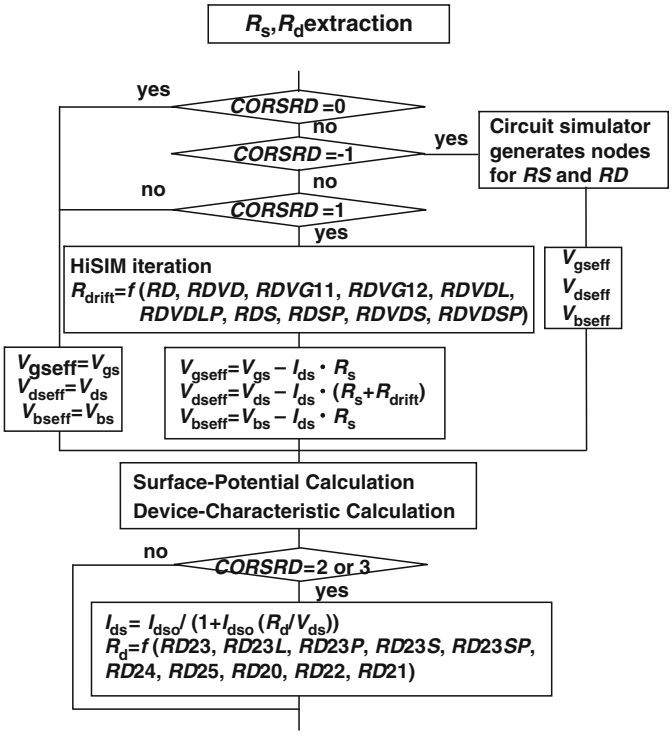

Fig. 2.11 Parameter extraction flow for resistance parameters of HiSIM-HV, which changes according to the resistance-model selection

The extraction of the resistance parameters is done according the selection of the resistance model as summarized in Fig. 2.11.

If the self-heating effect is activated, all device characteristics will normally change drastically. Retuning of model parameters is therefore required. The main affected model parameters, which need this retuning step, are related to the mobility and the resistance models. The temperature-dependent parameters are normally extracted without the self-heating effect from temperature-dependent measurements. It is usually not necessary to modify these initially extracted values of the temperature-dependent parameters after activating the self-heating effect.

5 Reproduction of High-Voltage MOSFET Characteristics

In this section the basic modeling capabilities of HiSIM-HV are demonstrated for the device characteristics, which newly appear in high-voltage MOSFETs and which are known to be difficult to capture by a compact model. Particularly, the anomalies in the capacitances of high-voltage MOSFETs, the quasi-saturation behavior in

the I-V characteristics, the scaling properties with drift-region doping and the scaling properties with drift-region length will be analyzed. Two-dimensional device-simulation results are used to analyze the newly occurring effects and to compare them to the compact-model results, thus verifying the correct modeling of these main high-voltage-MOSFET characteristics with HiSIM-HV.

5.1 Capacitances

The wide range of switching operations from a few volts to several hundred volts is realized in the high-voltage MOSFETs, as mentioned before, with a drift region of low-impurity concentration, which provides the required high-voltage-blocking capability. This has been observed to lead to anomalous characteristics for the capacitances of high-voltage MOSFETs, which become more pronounced with lower impurity concentrations of the drift regions. In particular, capacitance peaks appear in the C_{gg} capacitances as a function of V_{gs}. The effect is demonstrated by the 2-dimensional device simulations of Fig. 2.12 for the LDMOS structure, where the properties of C_{gg} change completely when the drift-region doping is reduced from 10^{17} to 10^{16}cm^{-3}. The experimentally often observed anomalous, V_{gs} -dependent capacitance peaks are seen to appear for the lower impurity concentration.

This anomalous capacitance effect has been modeled in previous approaches either by introducing an internal node at the channel/drift junction [16] or a resistance added as a sub-circuit in a macro model [17]. The former model solves the node potential iteratively until channel current and the current in the drift region at the node becomes equal. However, it is difficult to extract model parameters for both

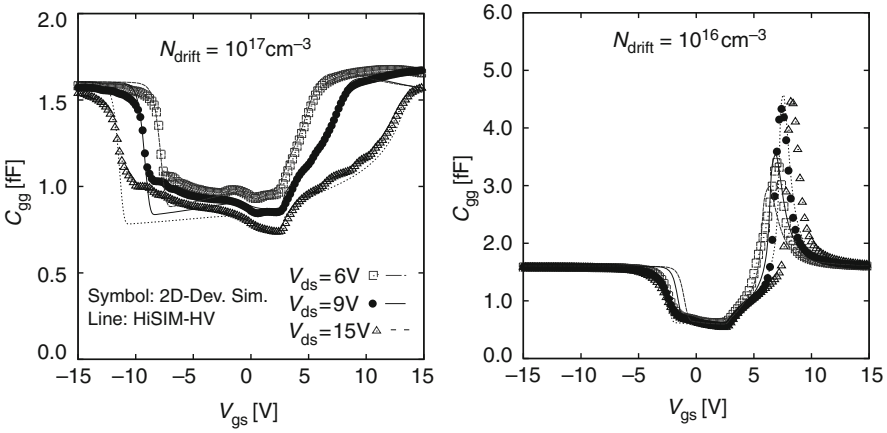

Fig. 2.12 Capacitance comparison between 2D-device simulation (*symbols*) and HiSIM-HV (*lines*) results for the LDMOS structure with different drift-region dopings of 10^{17}cm^{-3} (*left*) and 10^{16}cm^{-3} (*right*)

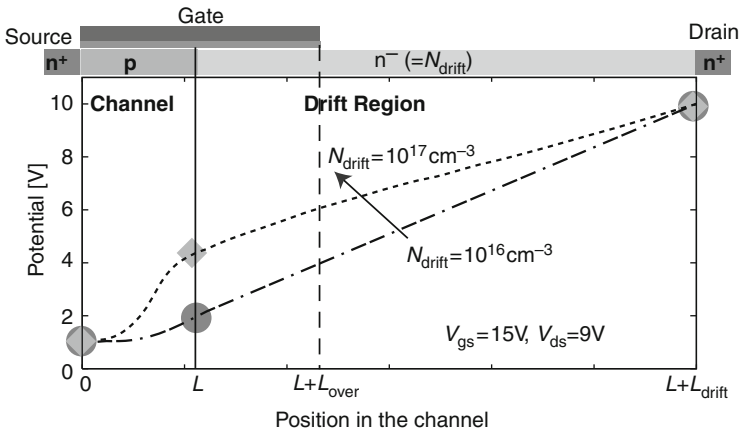

Fig. 2.13 Calculated potential distribution along the channel and the drift region of the LDMOS device with the developed HiSIM-HV model (shown with symbols) for two drift-region concentrations of 10^{17}cm^{-3} and 10^{16}cm^{-3}. Lines are 2-dimensional device simulation results

channel and drift regions with a single set of measured drain currents. The macro model description used in [17], is not valid for a sufficiently accurate modeling in the LDMOS case, because the internal node potential, which is determined by a balance between channel conductivity and the resistivity in the drift region, and which is responsible for all device features, cannot be correctly calculated.

On the other hand, HiSIM-HV consistently calculates the potential distribution along the channel and the drift region from the source to the drain contact. The changes in the potential distribution for different impurity concentrations in the drift region can therefore be accurately calculated, as demonstrated with the LDMOS structure in Fig. 2.13 for the drift-region-doping cases of 10^{17}cm^{-3} and 10^{16}cm^{-3}. Consequently, due to this accurate potential-distribution determination, HiSIM-HV is able to capture the scaling properties of the high-voltage MOSFET capacitances with respect to drift-region doping accurately, as verified by the lines in Fig. 2.12.

5.2 I-V Characteristics and Derivatives

Figure 2.14a,b,c shows a comparisons of $I - V$ and g_m characteristics for the LDMOS device structure and the two impurity concentrations 10^{17}cm^{-3} and 10^{16}cm^{-3} in the drift region, while keeping the length of the drift region and the other device parameters the same. Good agreement between the 2-dimensional device-simulation and HiSIM-HV results is again verified. Furthermore, the quasi-saturation effect can be clearly seen, in particular for the lower doping concentration, and is reproduced quantitatively.

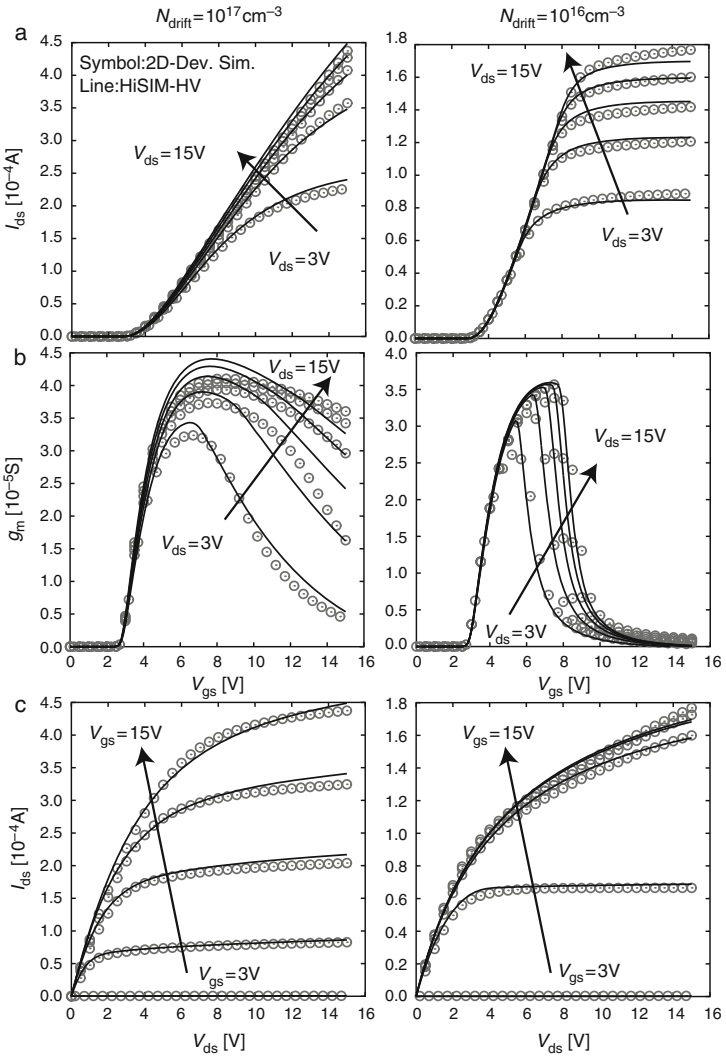

Fig. 2.14 Comparison of $I - V$ and g_m characteristics between 2-dimensional device simulator (*symbols*) and HiSIM-HV (*lines*) results for the LDMOS structure with different drift-region dopings of 10^{17} cm^{-3} (*left*) and 10^{16} cm^{-3} (*right*)

The corresponding C_{gg} characteristics has been compared in Fig. 2.12 of the previous section with for the two different drift-region doping values. As discussed, the anomalies observed as peaks in the V_{gs} dependence of C_{gg} for reduced drift-region doping are caused by the increased resistance effect in the drift region due to this lower impurity concentration. Figure 2.14b verifies that the drastic reduction of g_m as a function of V_{gs} coincides very well with these capacitance peaks.

5.3 Symmetric Versus Asymmetric Characteristics

Accurate surface-potential-dependent modeling of the overlap charge, Q_{over}, between the gate oxide and the drift region is already very important for the asymmetrical LDMOS structure. However, since substantial surface-potential-dependent overlap capacitances are located at source end as well as drain end for the symmetrical HVMOS-device structure, their contribution to the operational characteristics of the symmetrical devices becomes even more important.

For providing sufficient accuracy, the bias dependent surface potentials within the overlap regions consequently have to be considered in describing the formation of the accumulation, the depletion as well as the inversion condition underneath the gate overlap region, which now depend in a complicated way dynamically on the bias conditions.

These modeling tasks for the overlap region are achieved by solving the Poisson equation in the same way as in the channel. The overlap charges are determined in HiSIM-HV from the calculated surface-potential distribution under the simplifying approximation that the potential variation along the overlap region (see Section 3.1) is negligible. The surface-potential values are of course a function of the drift-region doping N_{drift}, which determines also the flat-band voltage within the overlap region. Calculated overlap capacitances with HiSIM-HV are shown in Fig. 2.15 as a function of V_{gs}.

Figure 2.16 compares the calculated capacitances for the asymmetrical LDMOS device and the symmetrical HVMOS device as obtained with HiSIM-HV and a 2-dimensional device simulator. It can be seen that the results agree well for both device structures. The shoulders in the overall capacitances originate from the overlap

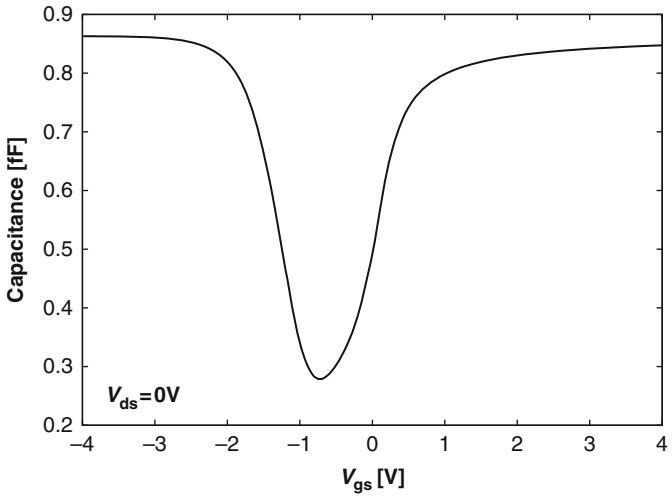

Fig. 2.15 Calculated overlap capacitance at the drain side with HiSIM-HV at $V_{\text{gs}} = 0\text{V}$

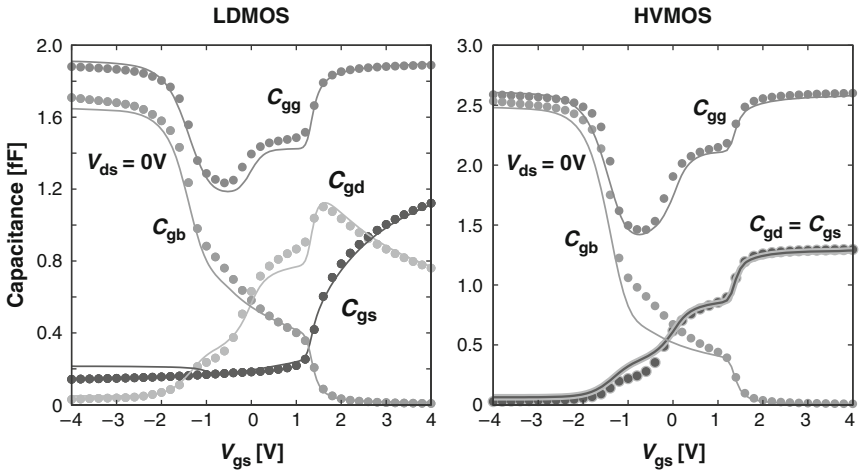

Fig. 2.16 Comparison of capacitances calculated for the asymmetrical LDMOS and symmetrical HVMOS structure with HiSIM-HV (*lines*) and a 2-dimensional device simulator (*symbols*). Again HiSIM-HV is verified to be in good agreement with the device-simulation results

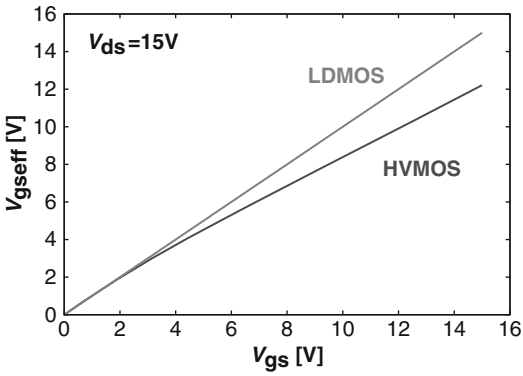

Fig. 2.17 Comparison of the effective gate-source voltage (V_{gseff}) as a function of the applied gate-source voltage (V_{gs}) for the symmetrical HVMOS and the asymmetrical LDMOS device structures

capacitances between the gate and the drift regions, which are non-negligible for high-voltage MOSFETs and have to be modeled under inclusion of their bias dependences.

For modeling of the symmetrical HVMOS device, the resistance model for the drift region, described in Section 3.2, has to be applied to the source side as well. Figure 2.17 shows the calculated potential drop within the drift region at the source end, causing a reduction of the effective gate-source potential of the MOSFET core from V_{gs} to V_{gseff}, which now furthermore depends in a dynamic way on bias conditions. This additional potential drop at the source end results of course also in a bias-dependent reduction of V_{ds} and V_{bs} as well. Therefore, the influence of the source resistance in the symmetric HVMOS device on the device characteristics can be expected to be very drastic.

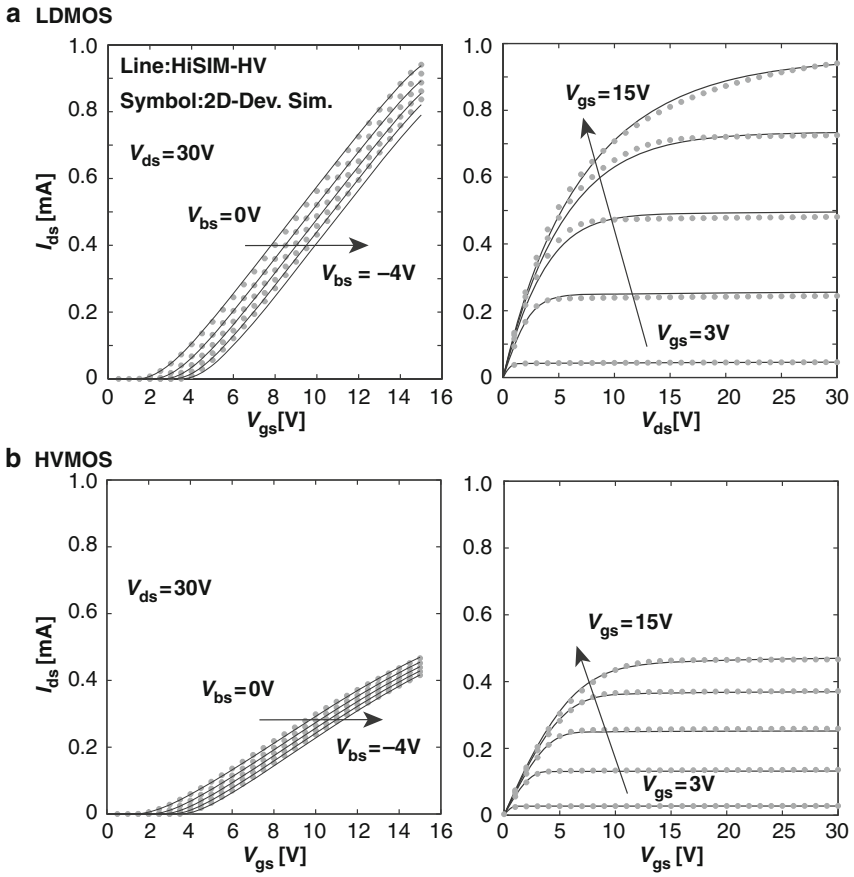

Fig. 2.18 Current comparison, (*left-hand side*) as a function of Vgs and (*right-hand side*) as a function of Vds, between LDMOS and HVMOS structures, respectively. Results from HiSIM-HV (*lines*) and 2-dimensional device simulation (*symbols*) are in very good agreement

Figure 2.18a,b compares the calculated I-V characteristics of HiSIM-HV for the asymmetrical LDMOS and the symmetrical HVMOS with 2-dimensional device-simulation results. The high resistance effect of the drift region causes a reduction of the potential increase in the channel, which also results in a drastic reduction of the drain current. This drain-current reduction is much more enhanced for the symmetrical HVMOS case due to the potential drop in the drift region at the source side. On the other hand the LDMOS device shows a more gradually increasing current due to the dynamic reduction of R_{drift} for an increased carrier concentration in the drift region. Thus, it is verified that all specific features of LDMOS and HVMOS devices can be well reproduced with the single model HiSIM-HV. This is an advantage obtained by the modeling based on the surface potential, which secures the consistency of the overall model description due to the consistent potential determination in the complete high-voltage MOSFET device.

5.4 Scaling Properties

As explained before, HiSIM-HV is constructed as a modular extension of the bulk-MOSFET model HiSIM2, which is fully scalable with respect to gate length L_g and gate width W_g, enabling the provision of a single global parameter set for the complete L_g-W_g space. Due to the modular extension concept, it becomes possible to preserve the L_g- as well as the W_g-scalability in HiSIM-HV and care is taken that this task is achieved. It turns out that the L_g-scalability can be achieved quite easily, without taking special measures in the modeling equations. However, the W_g-scalability is more difficult to achieve because the power dissipation increases drastically with larger W_g, while the thermal resistance and thermal capacitance properties change too. These power-dissipation effects under W_g-scaling are appropriately taken care of in the scaling properties of the self-heating model, so that accurate W_g-scaling of HiSIM-HV model is achieved.

Another desirable scaling property of a high-voltage MOSFET model is the correct scaling with respect to the drift-region parameters, in particular the drift-region doping N_{drift} and the drift-region length L_{drift}. The correct scaling properties of HiSIM-HV with respect to N_{drift} have already been demonstrated in Fig. 2.12 for the capacitances, in Fig. 2.13 for the potential distribution and in Fig. 2.14 for the $I-V$ characteristics.

Figure 2.19 verifies the scalability of HiSIM-HV with the drift-region length L_{drift} for the case of the $I-V$ characteristics as a function of the gate-source voltage V_{gs} with high and also low drain-source voltage V_{ds} biases.

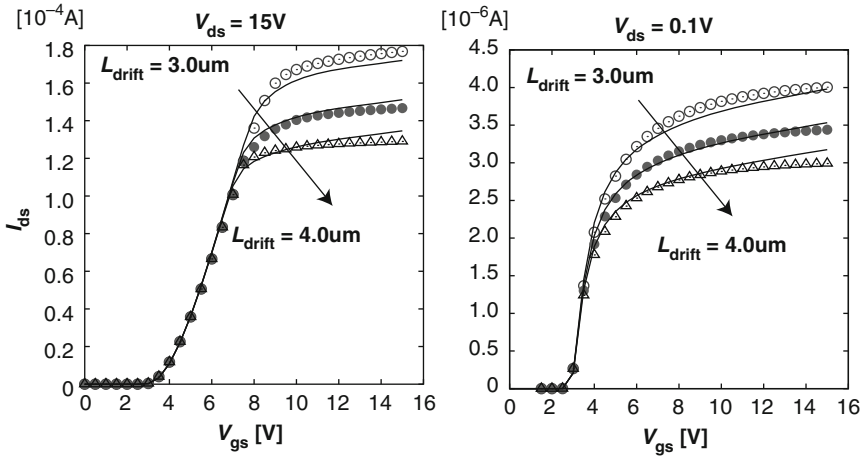

Fig. 2.19 Scalability of HiSIM-HV model with drift-region length L_{drift}. The plots compare the I_{ds}-V_{gs} characteristics at high and low drain bias for 2-dimensional device simulation (*symbols*) and HiSIM-HV (*lines*)

In fact HiSIM-HV is the only available high-voltage MOSFET model, which features the full scalability with MOSFET-core parameters and drift-region parameters, therefore being able to provide single global parameter set for high-voltage MOSFETs fabricated in a given technology.

6 Conclusion

The compact model HiSIM-HV for high-voltage MOSFETs, whose main features are described in this chapter, is based on the determination of the surface-potential distribution in the MOSFET core and the consistent potential extension to the drift region. Consequently, HiSIM-HV can accurately calculate the potential distribution in the entire asymmetric LDMOS structure or the symmetric HVMOS structure and determine all electrical and thermal high-voltage MOSFET properties without relying on any form of macro- or sub-circuit formulation. Furthermore, this consistent potential-based approach enables HiSIM-HV to reproduce all structure-dependent scaling properties of high-voltage MOSFET features with a single global parameter set.

The full scaling properties of HiSIM-HV with respect to the MOSFET-core geometry parameters L_g and W_g as well as the drift-region parameters L_{drift} and N_{drift} is unique among the compact high-voltage MOSFET models available today. As a result, HiSIM-HV has been selected by the Compact Model Council (CMC) [3] as the international compact-model standard for high-voltage-MOSFET devices. Continuously improved versions of the HiSIM-HV standard are released 2 times per year through the CMC.

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